Consumer LSI Devices
Digital ICs

Data Book
Volume II

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Picture-in-picture

Section 1 - Picture-in-picture

PICTURE IN PICTURE GENERATOR

The μPD42272A is a picture in picture generator (PIPG) made up of single chip including field memory, line memory, controller, and oscillator. It uses the C-MOS process, and implements high-speed processing and low power consumption. The μPD42272A include most features necessary for PIP processing; high performance TV and VCR systems can easily be implemented using this generator.

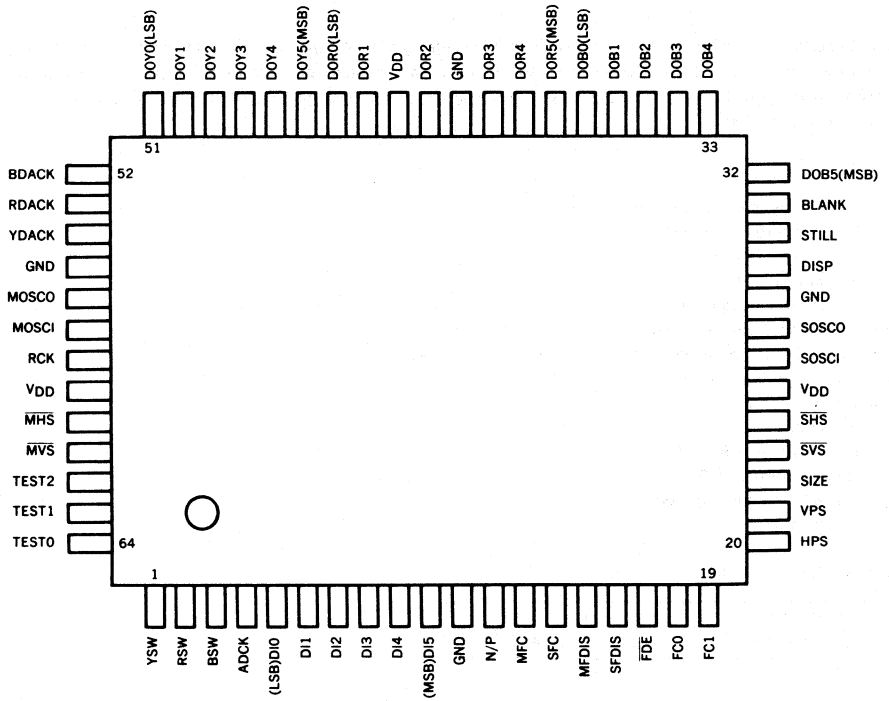
FEATURES

- The PIP features are integrated into single chip.
- Available for both PAL and NTSC
- Built-in vertical filter
- For 6 quantizing bits
- Two screen sizes are selectable.
- Four screen positions are selectable.
- Four frame colors (white, yellow, light blue, green) are selectable.
- For the color difference method (Y, R−Y, B−Y)
- Still picture display
- Tristate output
- Power supply V_{DD} = 5 V ±10 %
- TTL compatible (Full I/O)
- CMOS low power consumption
- 64-pin plastic QFP

ORDERING INFORMATION

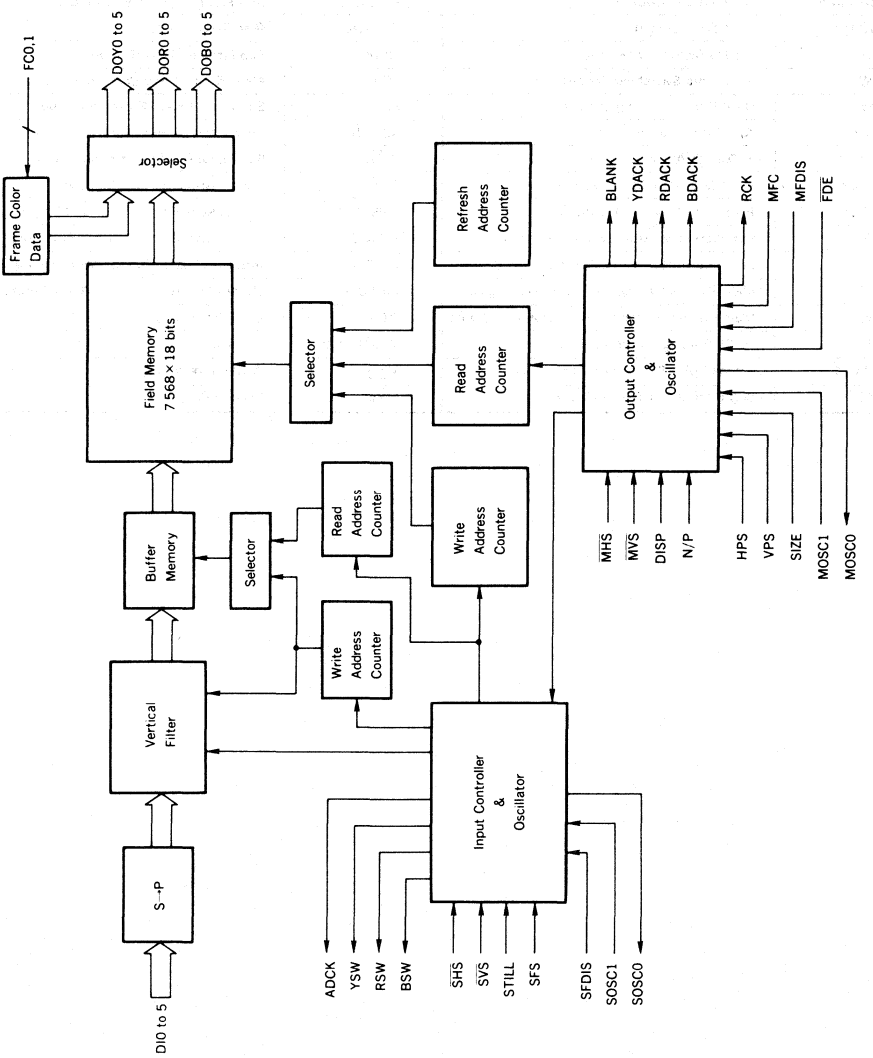
Order product name	Package
μPD42272AGF-3BE	64-pin plastic QFP

PIN CONFIGURATION (Top View)



ABBREVIATION	NAME	ABBREVIATION	NAME
DI0 to 5	Data Input	VPS	Vertical Screen Position Selection Input
DOY0 to 5	Y Data Output	HPS	Horizontal Screen Position Selection Input
DOR0 to 5	R—Y Data Output	STILL	Still Picture Specification Input
DOB0 to 5	B—Y Data Output	BLANK	Blanking Output
YSW	Y Data Switching Output	DISP	Sub Picture ON/OFF Input
RSW	R—Y Data Switching Output	MFC	Main Picture Field Correction Input
BSW	B—Y Data Switching Output	SFC	Sub Picture Field Correction Input
ADCK	A/D Clock Output	MFDIS	Main Picture Field Distinction Input
YDACK	Y Data D/A Clock Output	SFDIS	Sub Picture Field Distinction Input
RDACK	R—Y Data D/A Clock Output	$\overline{FDE}$	Field Distinction Enable Input
BDACK	B—Y Data D/A Clock Output	SOSCI	Input Oscillation Pin for Sub Picture
$\overline{SVS}$	Sub Picture Vertical Synchronizing Signal	SOSCO	Output Oscillation Pin for Sub Picture
$\overline{SHS}$	Sub Picture Horizontal Synchonizing Signal	MOSCI	Input Oscillation Pin for Main Picture
$\overline{MVS}$	Main Picture Vertical Synchronizing Signal	MOSCO	Output Oscillation Pin for Main Picture
$\overline{MHS}$	Main Picture Horizontal Synchronizing Signal	RCK	Lead Clock Output
N/P	NTSC/PAL Selection Input	TEST0 to 2	Test Pin
FC0 to 1	Frame Color Selection Input	V_{DD}	Power Supply Pin
SIZE	Sub Picture Size Selection Input	GND	Ground Pin

μPD42272A BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Pin Voltage	V_T	−0.1 to V_{DD} +0.5	V
Supply Voltage	V_{DD}	−0.1 to +7.0	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATION CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
High Level Input Voltage	V_{IH}	2.4		V_{DD} +0.5	V	
Low Level Input Voltage	V_{IL}	−1.0		+0.8	V	
Input Oscillation Frequency	$f_{OSC\ IN}$		6		MHz	
Output Oscillation Frequency	$f_{OSC\ OUT}$		18		MHz	
Horizontal Synchronizing Pulse Width	t_{HSYNC}		4.8		μs	$\overline{SHS}$ and $\overline{MHS}$ pins
$\overline{MVS}$ Pulse Width	$t_{\overline{MVS}}$	1		40	H	$\overline{MVS}$ Pin; IH = Period of horizontal signal
$\overline{SVS}$ Pulse Width	$t_{\overline{SVS}}$	1		25	H	$\overline{SVS}$ Pin; IH = Period of horizontal signal
Ambient Temperature	T_a	−20		+70	°C	

DC CHARACTERISTICS (In Recommended Operation Conditions)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Current	I_{DD}			75	mA	$f_{OSC\ IN}$ = 6 MHz, $f_{OSC\ OUT}$ = 18 MHz
Input Leak Current	I_I	−10		+10	μA	V_I = 0 to V_{DD}, other input 0 V
Output Leak Current	I_O	−10		+10	μA	V_O = 0 to V_{DD}, high impedance
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 2 mA

I/O CAPACITY (T_a = 25 °C, f = 1 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C_I			5	pF	Except SOSCI, MOSCI
Output Capacity	C_O			7	pF	Except SOCSO, MOSCO
Oscillation Input Capacity 1	C_{SOSCI}		8		pF	at SOSCI
Oscillation Input Capacity 2	C_{MOSCI}		10		pF	at MOSCI
Oscillation Output Capacity 1	C_{SOSCO}		8		pF	at SOSCO
Oscillation Output Capacity 2	C_{MOSCO}		10		pF	at MOSCO

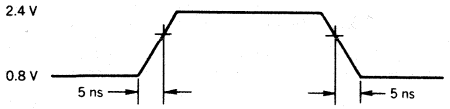
AC CHARACTERISTICS (In Recommended Operation Conditions)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	(Note)
ADCK Low Level Period	t_{ADL}	70		ns	
ADCK High Level Period	t_{ADH}	70		ns	
YDACK Low Level Period	t_{YDAL}	50		ns	
YDACK High Level Period	t_{YDAH}	50		ns	
RDACK Low Level Period	t_{RDAL}	200		ns	7
RDACK High Level Period	t_{RDAH}	200		ns	7
BDACK Low Level Period	t_{BDAL}	200		ns	7
BDACK High Level Period	t_{BDAH}	200		ns	7
RCK Low Level Period	t_{RCKL}	25		ns	
RCK High Level Period	t_{RCKH}	25		ns	
Data Input Setup Time	t_{DS}	25		ns	
Data Input Hold Time	t_{DH}	30		ns	
Y Data Access Time	t_{ACY}		25	ns	
Y Data Hold Time	t_{OHY}	20		ns	
R–Y Data Access Time	t_{ACR}		7RCK + 25	ns	
R–Y Data Hold Time	t_{OHR}	20		ns	
B–Y Data Access Time	t_{ACB}		7RCK + 25	ns	
B–Y Data Hold Time	t_{OHB}	20		ns	
Output Low Impedance Time	t_{LZ}	5	100	ns	4
Output High Impedance Time	t_{HZ}	5	100	ns	4
SW from ADCK High Level Output Time	t_{SW1}	5	30	ns	
SW from ADCK Low Level Output Time	t_{SW2}	5	30	ns	
Input Transition Time (Rise time, Fall time)	t_T	3	35	ns	

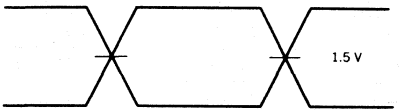
Notes:
1. The reference of any voltage is GND.
2. The above data was obtained in condition of $t_T = 5$ ns.
3. The input voltage reference levels of the timing standard are $V_{IH} = 2.4$ V and $V_{IL} = 0.8$ V.
4. t_{LZ} and t_{HZ} are measured at ±200 mV in the steady state. $t_{LZ} \geqq t_{HZ}$.
5. The I/O signal reference level is 1.5 V.
6. The input oscillation frequency ($f_{OSC\ IN}$) shall be 6 MHz; the output oscillation frequency ($f_{OSC\ OUT}$) shall be 18 MHz.
7. The frame output period is either 0.5 or 1.5 times as large as the standard value.

AC CHARACTERISTIC TEST CONDITIONS

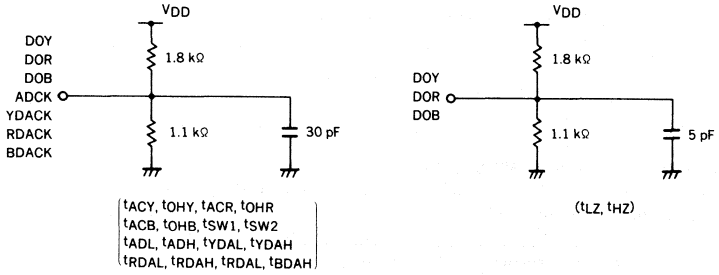
- **Input timing standard**



- **Output timing standard**



- **D_{OUT} load**



1. OVERVIEW OF FUNCTIONS

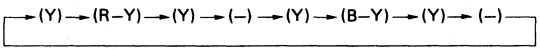
- Field memory capacity: 7 568 words x 18 bits
  (86 x 88)
- Subpicture display area:

Method	Full Screen Display (1/9)	80 % Screen Display (1/12)
NTSC	49.3 μs x 74 lines	41.3 μs x 62 lines
PAL	49.3 μs x 87 lines	41.3 μs x 73 lines

- Sampling rate

Signal	Input	Output
Y	3 MHz	9 MHz
R–Y	0.75 MHz	2.25 MHz
B–Y	0.75 MHz	2.25 MHz

- Sampling method



- Quantization : 6 bits
- Number of frame colors : 4 (White, yellow, light blue, green)
- Screen position : 4 (Top left, bottom left, top right, bottom right)
- Averaging processing that uses the vertical filter:

Line Number	Coefficient
n – 1	1/4
n	1/2
n +1	1/4

n: Line to be sampled

- Field-to-field line offset sampling processing
- Line array correction
- Display ON/OFF switching
- Still picture display

2. PIN FUNCTIONS

(1) DI0 to 5 (Data Input) (Input)

Six-bit data input pins that input digitized subpicture component signals (Y, R–Y, B–Y) sequentially. DI0 is the LSB, and DI5 is the MSB.

(2) DOY0 to 5 (Y Data Output) (Output)

Luminance signal (Y) output pins, which output six-bit Y signals compressed by a factor of three by PIP processing. DOY0 is the LSB, and DOY5 is the MSB. The high impedance state is entered unless the data is being output; the no-signal period level is determined from the external resistor.

(3) DOR0 to 5 (R–Y Data Output) (Output)

Color difference signal (R–Y) output pins, which output six-bit R–Y signals compressed by a factor of three by PIP processing. DOR0 is the LSB, and DOR5 is the MSB. The high impedance state is entered, unless the data is being output; the no-signal period level is determined from the external resistor.

(4) DOB0 to 5 (B–Y Data Output) (Output)

Color difference signal (B–Y) output pins, which output six-bit B–Y signals compressed by a factor of three by PIP processing. DOB0 is the LSB, and DOB5 is the MSB. The high impedance state is entered unless the data is being output; the no-signal period level is determined from the external resistor.

(5) YSW, RSW, BSW (Data Switching Output) (Output)

Output pins for the data switching signals supplied to the six-bit A/D converter (μPC661) with analog switch. Three component signals (Y, R–Y, B–Y) are converted from analog data to digital data while sequentially switching them with YSW/RSW/BSW. When the switching output is at the high level, the corresponding signal is selected. (For example, the Y signal is selected when YSW = H.)

(6) ADCK (A/D Clock Output) (Output)

Output pin for the sampling clocks supplied to the A/D converter (μPC661). While being synchronized to this clock, the component signals selected with the analog switch are converted from analog data to digital data. While being synchronized to this clock, the digitized component signals are sequentially input to the DI pin. The clock frequency is 6 MHz.

(7) YDACK, RDACK, BDACK (D/A Clock Output) (Output)

Output pins for the sampling clocks supplied to the six-bit D/A converter. After being submitted to PIP processing, the component signals are output from the DO pin. It goes from digital data to analog data while being synchronized to this clock. The three clock output pins correspond to the three component signals (YDACK ··· Y output, RDACK ··· R–Y output, BDACK ··· B–Y output). The clock frequency of YDACK is 9 MHz, and that of RDACK and BDACK is 2.25 MHz.

(8) $\overline{\text{SVS}}$ (Sub Picture Vertical Synchronization Signal Input) (Input)

The subpicture vertical synchronization signal input pin, which inputs vertical signals locked to the synchronous separation signal. When $\overline{\text{SVS}}$ falls, the internal Write Address Counter is rest. The frequency of Sub Picture Horizontal Synchronization Signal Input ($\overline{\text{SHS}}$) is then counted to determine the vertical write area of the subpicture. The $\overline{\text{SVS}}$ input is used also as the field distinction data of the subpicture.

(9) $\overline{\text{SHS}}$ (Sub Picture Horizontal Synchronization Signal Input) (Input)

Subpicture horizontal synchronization signal input pin, which inputs horizontal signals locked to the synchronous separation signal. Write Clock is oscillated synchronously with the $\overline{\text{SHS}}$ rising edge. This clock causes Write Address Counter to be incremented, and the horizontal write area is determined. The reference signal for field distinction is generated inside by counting Write Clock. The standard of $\overline{\text{SHS}}$ synchronization pulse width is 4.8 μs.

(10) $\overline{\text{MVS}}$ (Main Picture Vertical Synchronization Signal Input) (Input)

Main Picture vertical synchronization signal input pin, which inputs vertical signals locked to the synchronous separation signal. When $\overline{\text{MVS}}$ falls, the internal Read Address Counter is reset. The frequency of Main Picture Horizontal Synchronization Signal Input ($\overline{\text{MHS}}$) is then counted to determine the vertical display area and display position of the subpicture. The $\overline{\text{MVS}}$ input is used also as the field distinction data of the main picture.

(11) $\overline{MHS}$ (Main Picture Horizontal Synchronization Signal Input) (Input)

Main Picture horizontal synchronization signal input pin, which inputs horizontal signals locked to the synchronous separate signal. Read Clock is oscillated synchronously with the $\overline{MHS}$ rising edge. This clock causes Read Address Counter to be incremented, and the horizontal display area and display position are determined. The reference signal for field distinction is generated inside by counting Read Clock. The standard of $\overline{MHS}$ synchronization pulse width is 4.8 μs.

(12) N/P (NTSC/PAL Selection Input) (Input)

Input pins used to select the NTSC and PAL methods. When the input level is High (H), NTSC is selected. When it is Low (L), PAL is selected. These methods differ in vertical write operation and the display area.

(13) FC0 to 1 (Frame Color Selection Input) (Input)

Input pins used to specify the subpicture frame color. One of four frame colors (white, light blue, yellow, green) can be selected by input level combination.

	White	Light Blue	Yellow	Green
FC0	H	L	H	L
FC1	H	H	L	L

(14) SIZE (Subpicture Size Selection Input) (Input)

Input pin used to specify the subpicture size (display area). When the input level is H, this size is set to one-ninth of the main picture (full screen display). When the level is L, it is set to one-twelfth (80 % display).

(15) VPS, HPS (Position Selection Input) (Input)

Input pins used to specify the sub picture display position. One of the four corners on the main picture can be selected by combining the VPS and HPS input levels. VPS specifies the vertical position; HPS specifies the horizontal position.

	Top Left	Bottom Left	Top Right	Bottom Right
VPS	H	L	H	L
HPS	H	H	L	L

(16) STILL (Still Picture Request Input) (Input)

Input pin used to specify the still picture. When the input level is H, the still picture is selected. When the input level is L, the moving picture is selected.

(17) BLANK (Blanking Output) (Output)

Signal output pin used to blank the main picture. When the output level is H, the subpicture signal is output.

(18) DISP (Subpicture ON/OFF Input) (Input)

Input pin used to turn on/off the blanking signal (BLANK). When the input level is H, the BLANK signal is output. When the input level is L, the signal is turned off (low level). At this time, the subpicture data output signals (DOY, DOR, DOB) are output regardless of the DISP pin input level.

(19) MFC (Main Field Correction Input) (Input)

Input pin used to correct Main Picture Signal field distinction. The μPD42272A distinguishes fields based on the phase relation between the horizontal and vertical synchronization signals to be input. Thus, field distinction may fall into error if the proper phase relation is not obtained. In this case, the distinction result is corrected using the MFC pin. If the input level is H, the field distinction result will be reversed. If it is L, the original result will be used.

(20) SFC (Sub Field Correction Input) (Input)

Input pin used to correct the Subpicture Signal field distinction result. The function is the same as for the MFC pin.

(21) MFDIS (Main Field Distinction Input) (Input)

Input pin for the Main Picture Signal field distinction result. The μPD42272A distinguishes fields based on the phase relation between the horizontal and vertical synchronization signals to be input. In addition, the result from outside field-distinction can be input from the MFDIS pin. The H level indicates an old field; the L level indicates an even field.

(22) SFDIS (Sub Field Distinction Input) (Input)

Input pin for the Subpicture Signal field distinction result. The function is the same as for the MFDIS pin.

(23) $\overline{FDE}$ (Field Distinction Enable Input) (Input)

Input pin used to select whether field distinction is executed inside or the outside distinction result is input (MFDIS, SFDIS). When the input level is H, the inside field distinction is inhibited. In this case, outside field distinction is executed, depending on the signal levels input through the MFDIS and SFDIS pins. When the input level is L, input from the MFDIS and SFDIS pin is inhibited. In this case, the inside field distinction data is effective.

(24) SOSCI, SOSCO (Sub Oscillation Input/Output) (Input, Output)

Oscillation pins for the subpicture Write Clock. The oscillation capacitor and coil must have been installed externally. The oscillation frequency must be 6 MHz. The SOSCI can also be used to input clocks from the outside.

(25) MOSCI, MOSCO (Main Oscillation Input/Output) (Input, Output)

Oscillation pins for the subpicture Read Clock. The oscillation capacitor and coil must have been installed externally. The oscillation frequency must be 18 MHz. The MOSCI pin can also be used to input clocks from the outside.

(26) RCK (Read Clock Output) (Output)

Output pin for the subpicture Read Clock. Used to output the clocks oscillated with the main oscillation circuit. Can be used for synchronization with another IC.

(27) TEST (Test Input) (Input)

Test pin. Must usually be grounded.

(28) V_{DD} (Voltage Supply)

Power supply pin.

(29) GND (Ground)

Ground pin.

3. CONFIGURATION

(1) Serial/parallel Converter (S → P)

Converts into 18-bit parallel signals (Y·R–Y·Y or Y·B–Y·Y) the subpicture signals (Y, R–Y, B–Y) that are serialy input in units of six bits, and outputs them.

(2) Vertical Filter

Consists of two sets of line memory and an arithmetic circuit, and executes averaging processing. If one of the three lines is simply extracted to compress the screen vertically, may become disordered on the screen. To prevent this, averaging processing is executed with the data of the appropriate line and the preceding and succeeding lines by using the vertical filter.

(3) Buffer Memory

If field memory is in read mode, no data can be written into it. The subpicture signals input during the read mode need to be stored in the buffer memory, which has one-line capacity (86 words x 18 bits).

(4) Field Memory

Stores one field (7 568 words x 18 bits) of a subpicture. Data is written into field memory when no subpicture is being displayed.

(5) Line Memory Write Address Counter

Supplies write addresses to the line memory of the vertical filter block and buffer memory. When the address reaches the set value, this counter stops counting. Reading the data from the vertical filter block (1 line/3 lines), use the write address.

(6) Buffer Memory Read Address Counter

Supplies read addresses to buffer memory. This counter is synchronized with field memory Write Address Counter; it remains in the wait state during field memory read. When the address reaches the set value, this counter stops counting.

(7) Buffer Memory Address Selector

Outputs the write and read addresses to buffer memory while switching them.

(8) Field Memory Write Address Counter

Supplies write addresses to field memory. This counter consists of the horizontal and vertical address counters. The horizontal and vertical address counters. The horizontal one is synchronized with Buffer Memory Read Address Counter. It remains in the wait state during memory read. When the address reaches the set value, this counter stops counting.

(9) Field Memory Read Address Counter

Supplies read addresses to field memory. This counter consists of the horizontal and vertical address counters. Data read from field memory always takes priority over write to it. Thus, the counter never enters the wait state during operation. When the address reaches the set value, this counter stops counting.

(10) Refresh Address Counter

Supplies refresh addresses to field memory. When write/read for field memory is at a stop, this counter refreshes the memory according to the Refresh Address Counter's address value. The input clock (6 MHz) is frequency-divided, and supplied to the counter. It remains in the wait state while data is being read from or written into field memory. When the address reaches the set value, this counter stops counting, and the address returns to the start address.

(11) Field Memory Address Selector

Supplies the write, read, and refresh addresses while switching them.

(12) Output Data Selector

Switches the subpicture signal read from field memory and the frame color signal selected with a frame color selection pin (FC0 or FC1), and outputs the signal. In addition, this selector concurrently executes parallel/serial conversion (12 bits → 6 bits) of the subpicture Y signal.

(13) Input Controller & Oscillator

Controls the subpicture signal until it is written into field memory. This circuit oscillates the input clock (6 MHz) synchronously with Subpicture Horizontal Synchronization Signal ($\overline{SHS}$). Using this clock as the reference, the circuit controls vertical filter or buffer memory write/read operation and the field memory write operation. This circuit also generates the ADCK, YSW, RSW, and BSW control signals, transmitted to the six-bit A/D converter (μPC661).

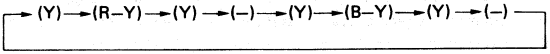
(14) Output Controller & Oscillator

Controls the subpicture signal during the period from read from field memory to output. This circuit oscillates the output clock (18 MHz) synchronously with the Main Picture Horizontal Synchronization Signal ($\overline{MHS}$). Using this clock as the reference, the circuit controls the field memory read operation and the data selector. In addition, it generates the YDACK, RDACK, and BDACK control signals, transmitted to the six-bit D/A converter (μPD6901). The BLANK and RCK signals are also generated by this circuit.

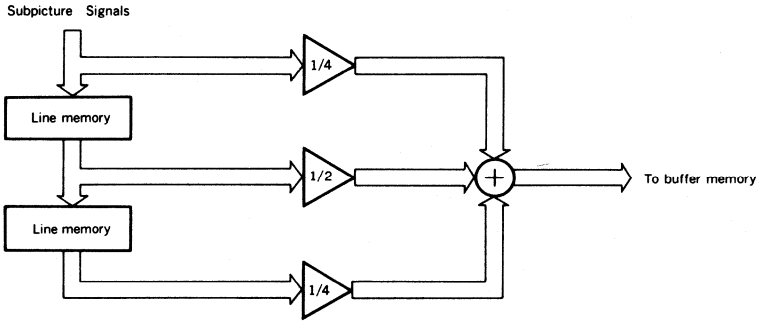
4. OPERATION

4.1 Writing the Subpicture Signals

The subpicture signals are converted, by the six-bit A/D converter (μPC661), into digital data, then input from the Data Input pin (DI). At this time, the subpicture signals are sequentially switched with the YSW, RSW, and BSW data switching signals. They are serially sampled as follows:

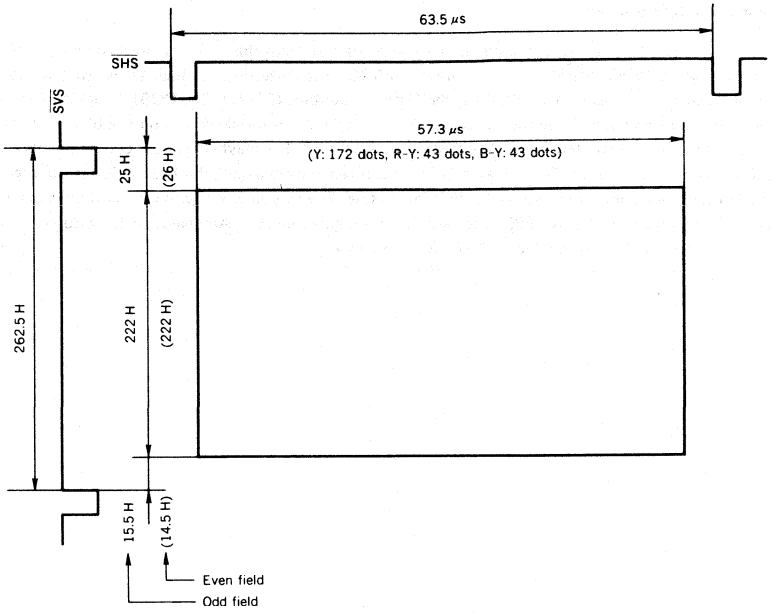


The (–) data is not transferred actually. The subpicture signals are converted, by the serial/parallel converter, into 18-bit data (Y·R–Y·Y or Y·B–Y·Y), then averaged in Vertical Filter. The vertical filter configuration is as follows:

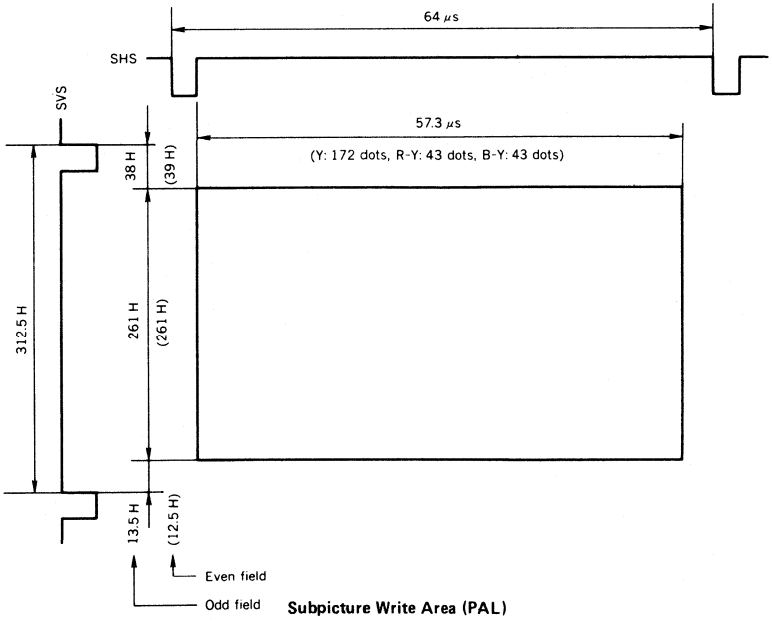


After being averaged in Vertical Filter, the subpicture signals are extracted line by line from the three lines. They are then written into buffer memory. After this, when field memory read is at a stop, the subpicture signals are written from buffer memory into field memory at a rate of 1.5 MHz.

The subpicture signal write area varies with the NTSC/PAL method as shown below. The odd and even fields deviate one line in the vertical write area. This enables field-to-field line offset sampling processing, which improves the vertical resolution.



Subpicture Write Area (NTSC)

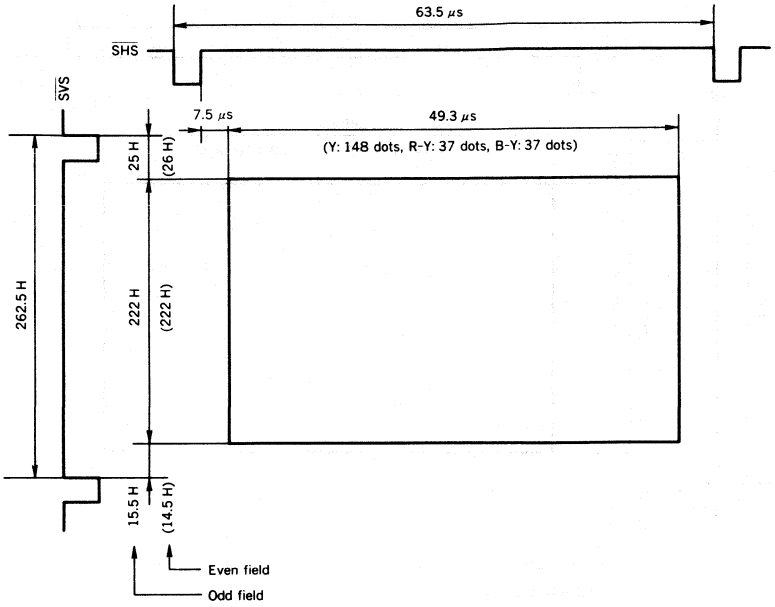


Subpicture Write Area (PAL)

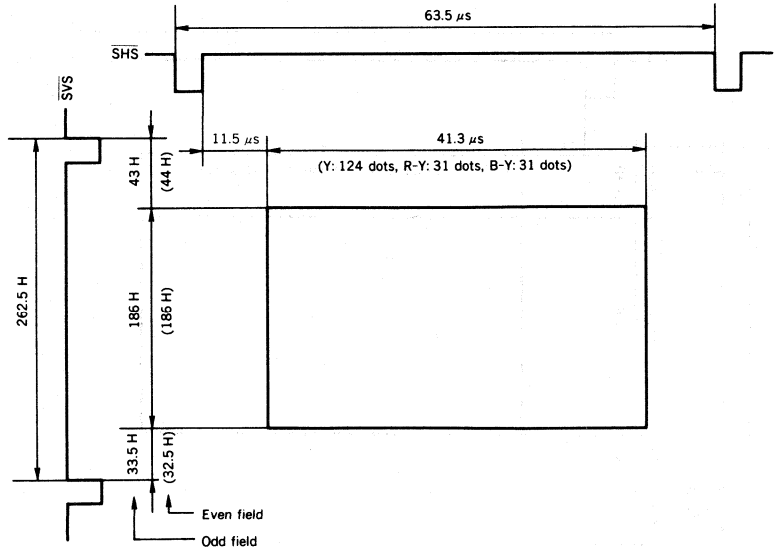
4.2 Reading the Subpicture Signals

After being written in field memory, the subpicture signals are read from this memory synchronously with the Main Picture Synchronization Signals ($\overline{MHS}$, $\overline{MVS}$). The reading rate (4.5 MHz) is three times as high as the writing rate. The subpicture signals then pass Selector, and are output through the Data Output pins (DOY, DOR, DOB). In addition to switching/outputting the subpicture and frame signals, Selector executes the Y signal parallel/serial conversion (12 bits → 6 bits).

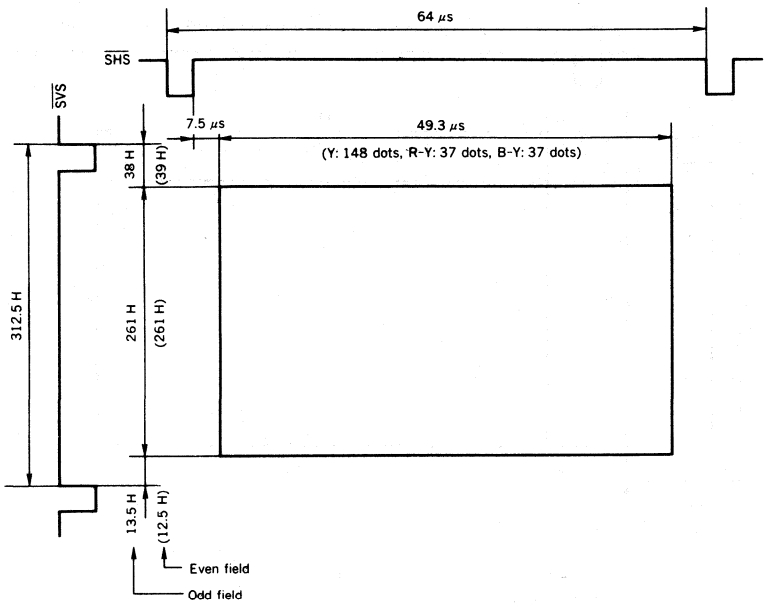
Subpicture signal read is executed for all data that has been written. The playback area is determined by the blanking signal (BLANK), and is not the write area. The display position is controlled by changing the Read Address Counter timing according to the Screen Position Selection Input Pin (HPS, VPS) input state. The playback area and display position vary with the NTSC/PAL method and screen size (full screen/80 % screen) (see the figures below). Any value in the display position includes the frame signal, which has a 220 ns (horizontal) x 1 line (vertical) area.



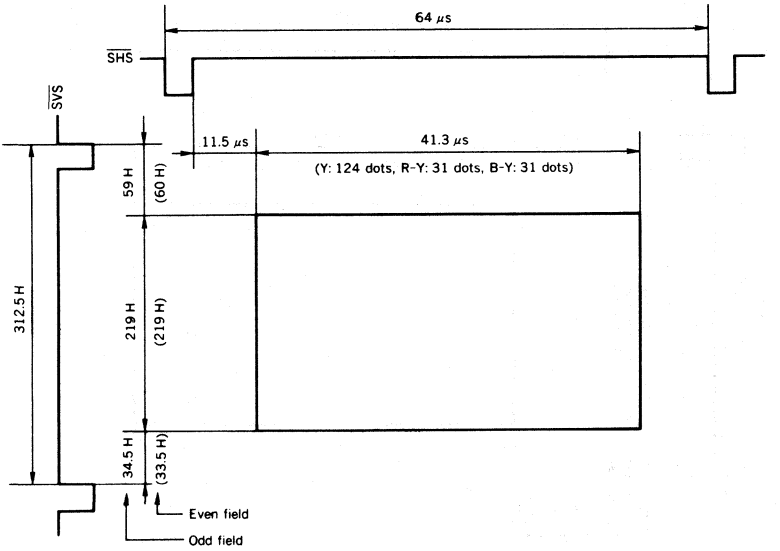
Subpicture Playback Area (NTSC, full screen display)



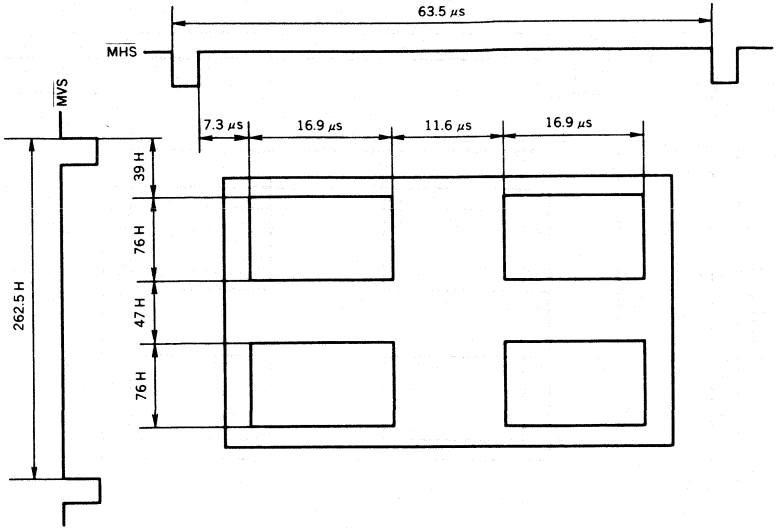
Subpicture Playback Area (NTSC, 80 % screen display)



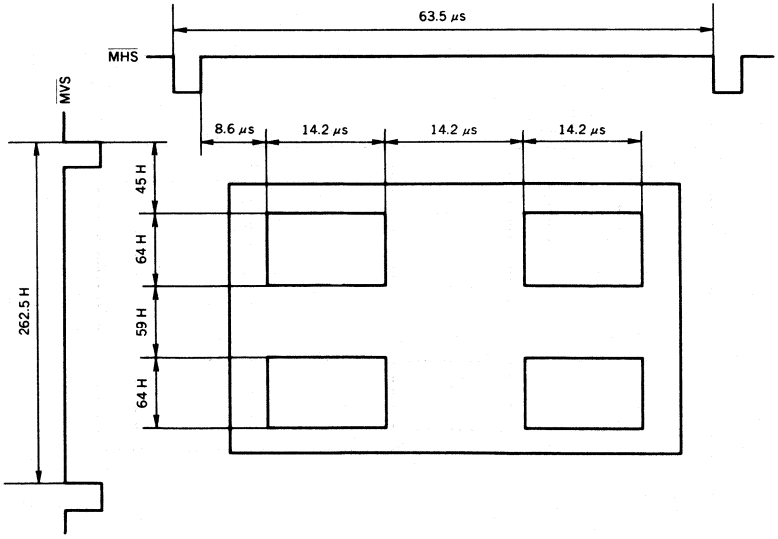
Subpicture Playback Area (PAL, full screen display)



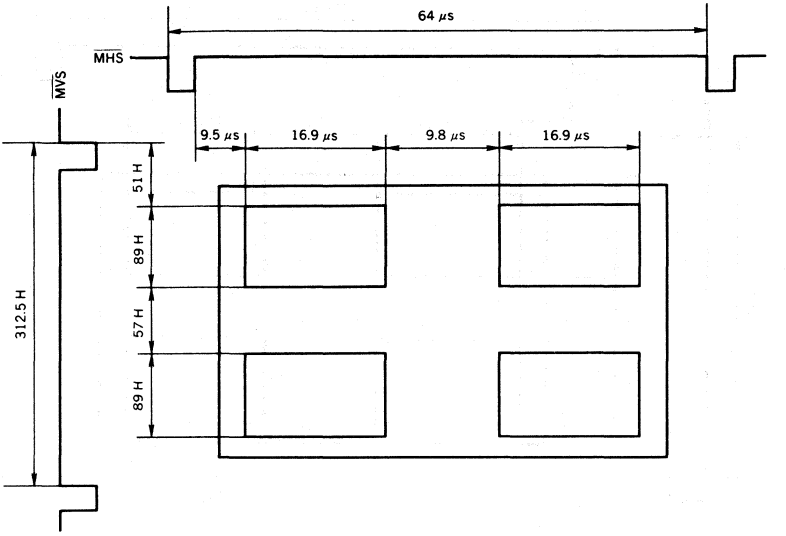
Subpicture Playback Area (PAL, 80 % screen display)



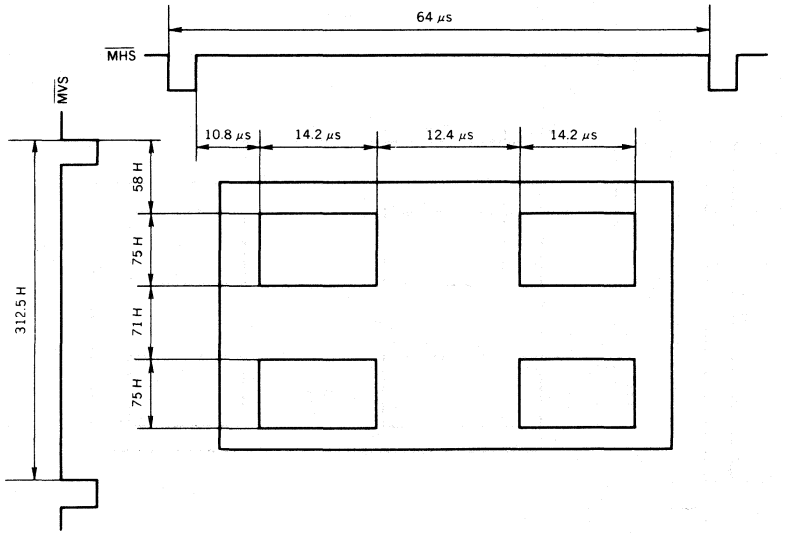
Subpicture Display Position (NTSC, full screen display)



Subpicture Display Position (NTSC, 80 % screen display)



Subpicture Display Position (PAL, full screen display)



Subpicture Display Position (PAL, 80 % screen display)

4.3 LINE Array Correction

Subpicture processing executes screen compression; the field memory read rate is three times as high as the write rate. The read operation thus outruns the write operation half way on the screen. After this, old fields are read. As a result, a field joint is produced halfway on the screen. When the data under the joint, that is, old fields are read in this case, the screen reverses because of interlace scanning. The line array correction resolves this reverse.

Line array is corrected by advancing the vertical address counter to the ordinary value plus 1, during old-field read. The correction operation varies with combination of the main picture and subpicture fields (odd/even). The following tables summarizes this:

When the main picture and subpicture have the same fields prior to outrunning

Main Picture \ Subpicture	Odd	Even
Odd	– (Before outrunning) →	– (After outrunning)
Even	+1 (After outrunning) ←	– (Before outrunning)

When the main picture and subpicture have different fields prior to outrunning

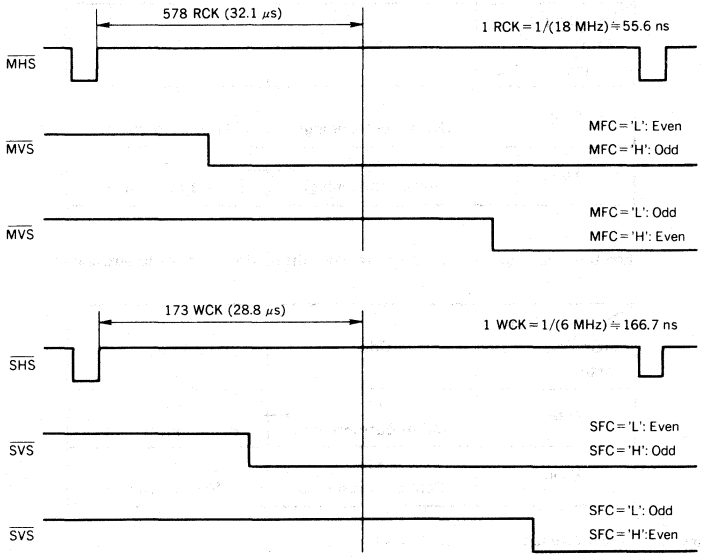
Main Picture \ Subpicture	Odd	Even
Odd	+1 (After outrunning) ←	– (Before outrunning)
Even	+1 (Before outrunning) →	+1* (After outrunning)

+1: The address counter is incremented to the normal value plus 1.
– : No operation.
* : Indicates that the address counter holds the incremented status. (The address counter is not incremented actually.)

4.4 Field Distinction

As mentioned in Sections 4.1 and 4.3, the μPD42272A executes line offset sampling and line array correction. Line offset sampling is to offset write lines between fields by one line. Line array correction is to advance the vertical Read Address Counter to the ordinary value plus 1 by combining the main picture and subpicture signal fields. This is required to prevent screen reverse caused by the outrunning in field memory read.

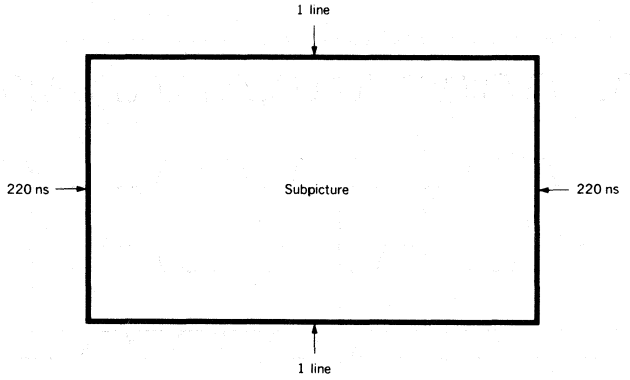
To execute the above processes, the μPD42272A executes field distinction to distinguish the main picture and subpicture signal field status (odd/even). The field distinction result is determined as follows according to (i) the phase difference between the input horizontal synchronization signals ($\overline{MHS}$, $\overline{SHS}$) and vertical synchronization signals ($\overline{MVS}$, $\overline{SVS}$) and (ii) the state of the field correction input pins (MFC, SFC).



At this time, the falling edges of the horizontal signal ($\overline{MHS}$, $\overline{SHS}$ = 'L') and falling edges of the vertical signals ($\overline{MVS}$, $\overline{SVS}$) must not overlap.

4.5 Frame Signal Generation

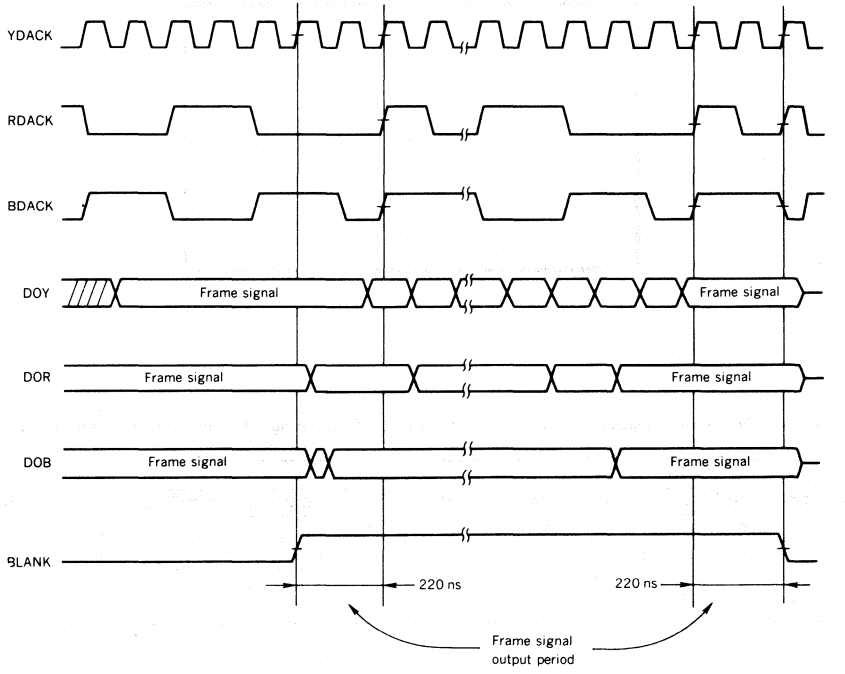
The μPD42272A contains the data for four colors (white, yellow, light blue, green) that are used for frame signals. Frame Color Selection Input (FC0, FC1) selects a color. Data Selector switches the subpicture to the frame signal, and outputs it. The vertical width of the frame signal is 1 line; the horizontal width is 220 ns. The horizontal width is determined according to the D/A clock (YDACK, RDACK, BDACK) and blanking signal (BLANK).



The four colors of the frame signal are represented individually by six bits assigned to the Y, R−Y, and B−Y signals.

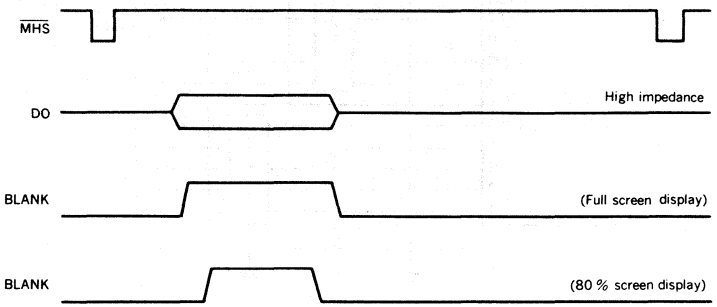
Signal / Color	Y						R−Y						B−Y					
	DO5	DO4	DO3	DO2	DO1	DO0	DO5	DO4	DO3	DO2	DO1	DO0	DO5	DO4	DO3	DO2	DO1	DO0
White	1	0	1	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0
Yellow	1	0	0	1	1	0	1	0	0	0	1	1	0	0	1	1	0	1
Light Blue	0	1	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1	1
Green	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	1

As mentioned previously, the μPD42272A writes the subpicture signals (Y, R−Y, B−Y) serially using the μPC661, which is a six-bit A/D converter with analog switch. For this reason, the R−Y and B−Y signal sampling phases are reversed. For the output signals, there is 180 ° phase difference between the R−Y and B−Y signals. If frame signals containing phase differences are similarly output, gradation is generated because the frame signals deviate at the edges. To prevent this, the μPD42272A adjusts the color signal D/A clock (RDACK, BDACK) phases during the frame signal output period to align the frame signal edges.



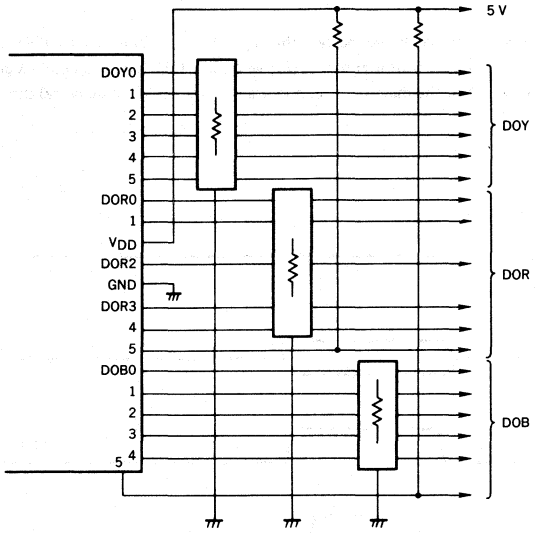
4.6 Data Output

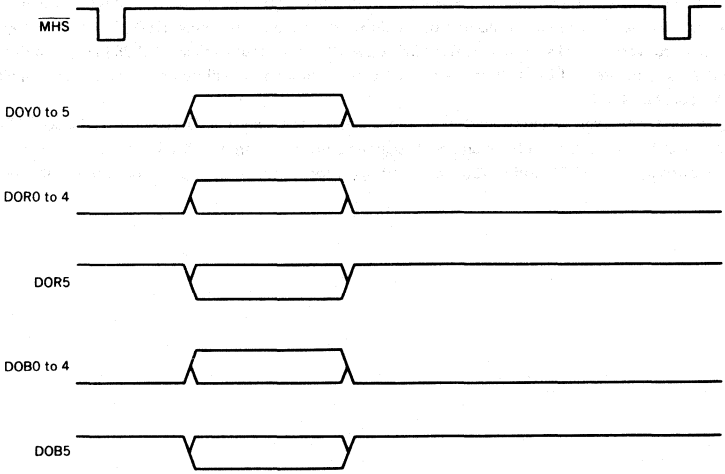
After compressed, the subpicture signals are output through the Data Output pins (DOY, DOR, DOB). The subpicture signals are compressed to the scale of 1/9 (horizontal: 1/3; vertical: 1/3). The subpicture signal output period is about one-ninth of one field period (16.7 ms) of the main picture; no data is output (high impedance) during the remaining period (eight-ninth) of the period.



The signal level of the above no-signal (high impedance) period must meet the pedestal level (level of the initial input signal). To do this, the signal level is determined by pulling up or down the Data Output pins (DOY, DOR, DOB) by resistors. In the μPD42272A, the D/A converter clocks (YDACK, RDACK, BDACK) are output cyclically (2.25 MHz) also during the no-signal period. The six-bit D/A converter (μPD6901) converts the data determined by pull-up or -down into analog data. This enables the signal to be at a constant level.

The input signal pedestal level is determined at clamp levels of the six-bit A/D converter (μPC661). For the μPC661, the Y signal clamp level is the 0LSB; the R–Y and B–Y signal clamp signals are the 32LSB. All Y output is thus pulled down. For R–Y and B–Y output, only DOR5 and DOB5 are pulled up, respectively, and the other output is pulled down.


5 V
DOY0
1
2
3
4
5
DOR0
1
VDD
DOR2
GND
DOR3
4
5
DOB0
1
2
3
4
5
DOY
DOR
DOB


MHS
DOY0 to 5
DOR0 to 4
DOR5
DOB0 to 4
DOB5

1

4.7 Outside Control

4.7.1 Specified frame color

μPD42272A can generate one of four frame colors (white, light blue, yellow, green) at inside. Frame color selection is used by Frame color Selection Input ($FC_{0\ to\ 1}$). One of four frame colors can be selected by input level combination.

	White	Light Blue	Yellow	Green
FC0	H	L	H	L
FC1	H	H	L	L

4.7.2 Specified subpicture size

μPD42272A can select one of two subpictures size (display area) by Subpicture Size Selection Input (SIZE). When the input level is H, this size is set to one-ninth of the main picture (full screen display). When the level is L, it is set to one-twelfth (80 % screen display).

4.7.3 Specified subpicture position

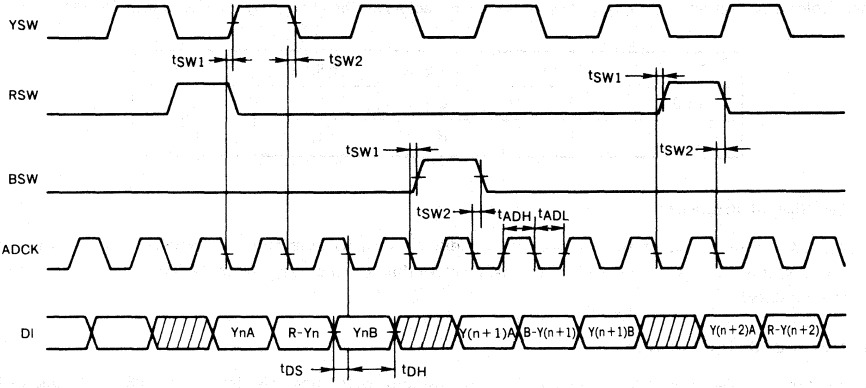
μPD42272A can select one of four subpicture display positions by Position Selection Input (VPS, HPS). One of the four corners on the main picture can be selected by combining the VPS and HPS input level.

	Top Left	Bottom Left	Top Right	Bottom Right
VPS	H	L	H	L
HPS	H	H	L	L

4.7.4 Specified still picture

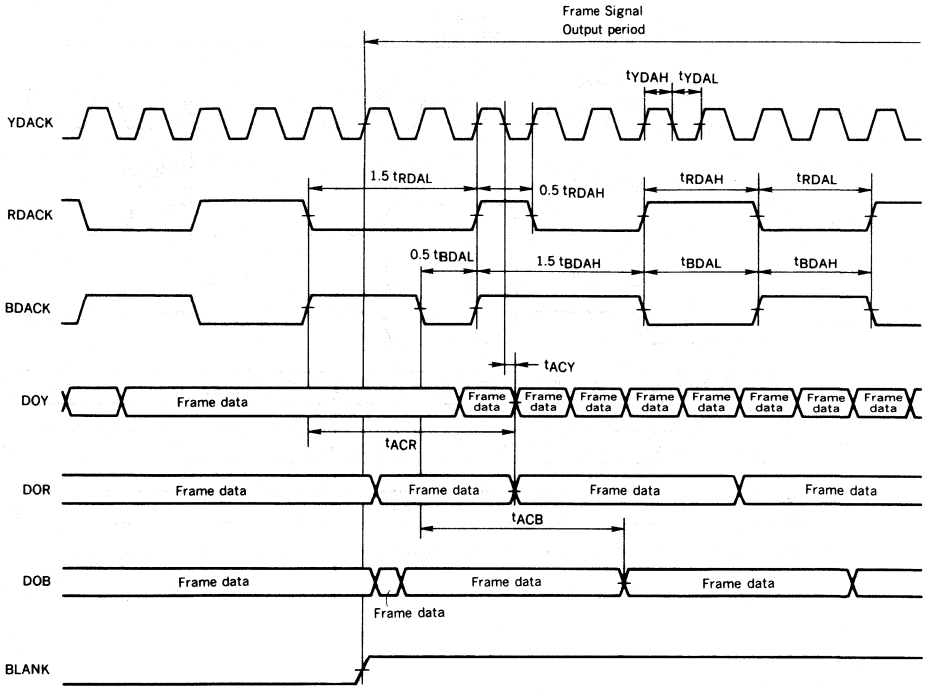
μPD42272A can display still subpicture by Still Picture Request Input (STILL). When the input level is H, the still picture is selected. When the input level is L, the moving picture is selected.

INPUT TIMING

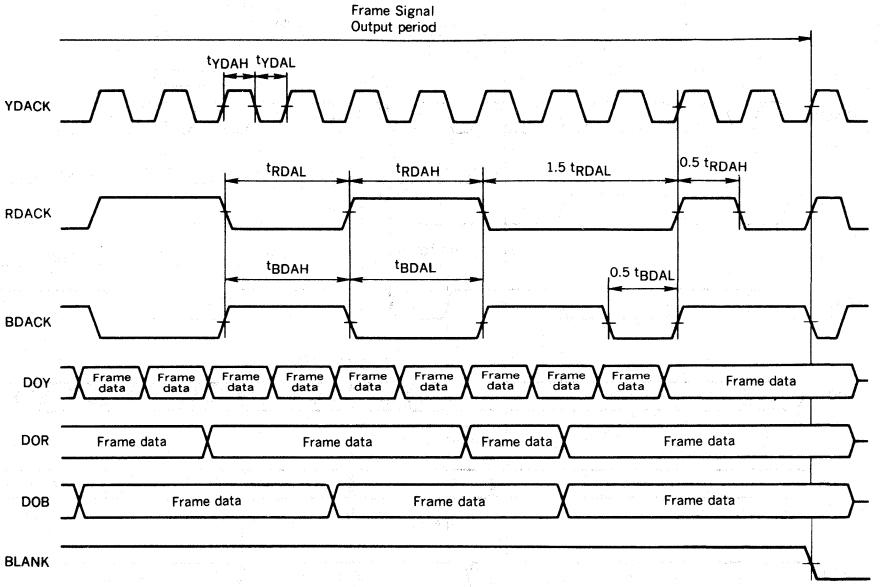


Note n: Odd number of 1 to 85

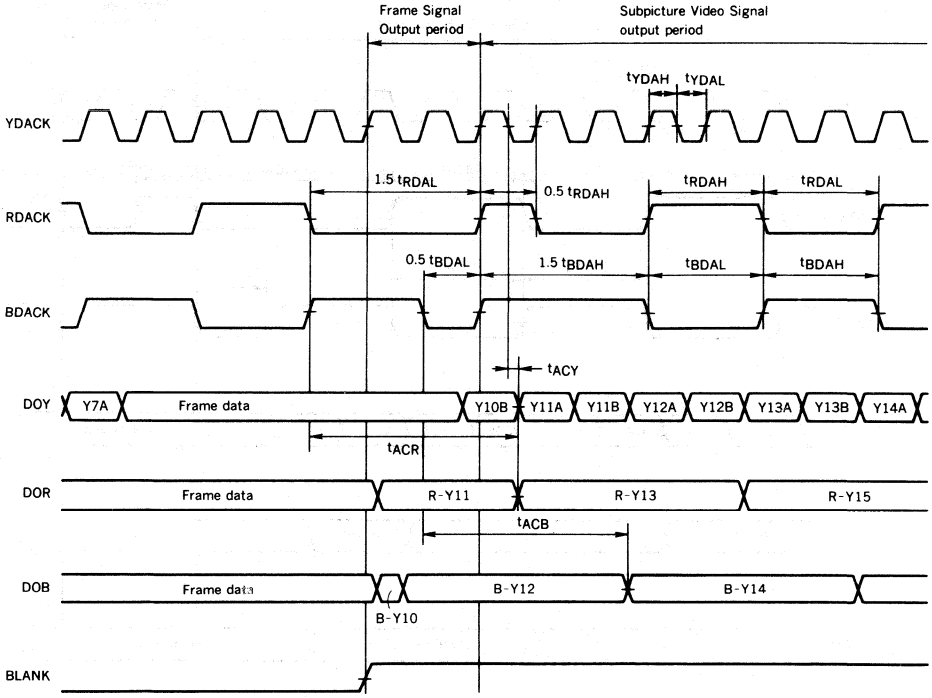
OUTPUT TIMING (1) [Subpicture 1 line, 76 line (at NTSC full screen)]



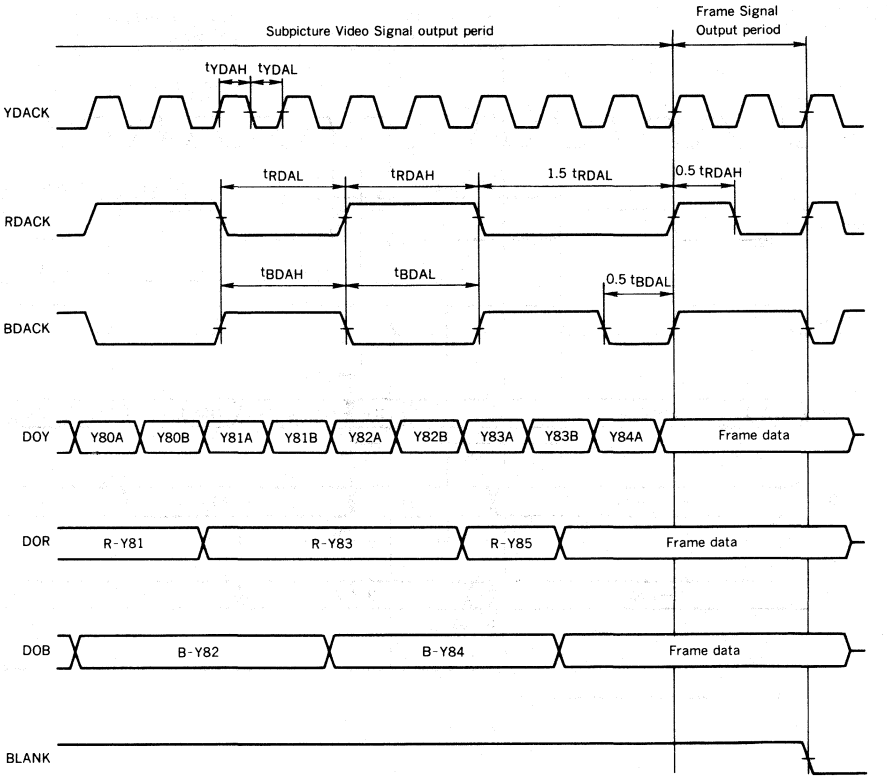
OUTPUT TIMING (2) [Subpicture 1 line, 76 line (at NTSC full screen)]



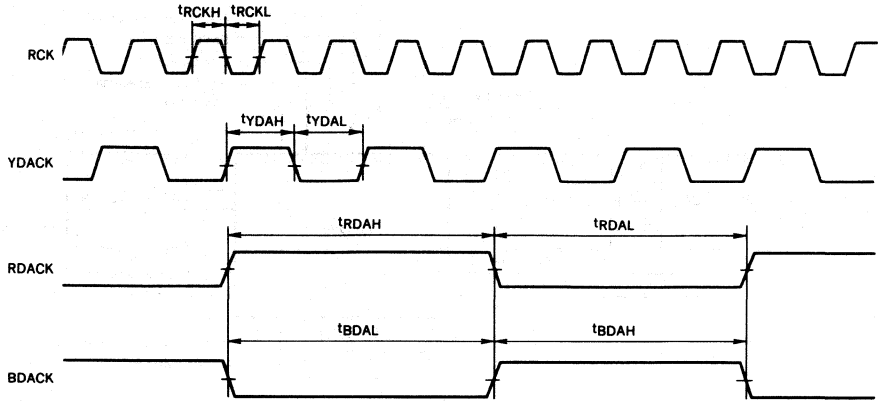
OUTPUT TIMING (3) [Subpicture 2 to 75 line (at NTSC full screen)]



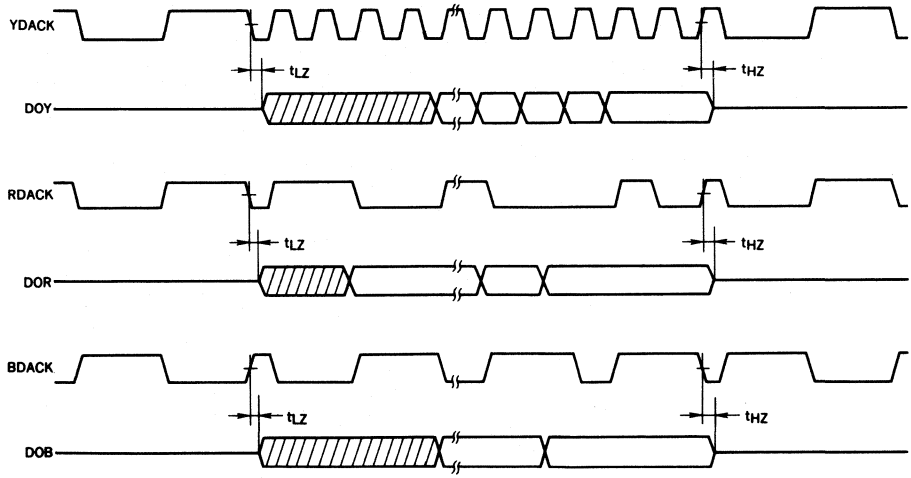
OUTPUT TIMING (4) [Subpicture 2 to 75 line (at NTSC full screen)]



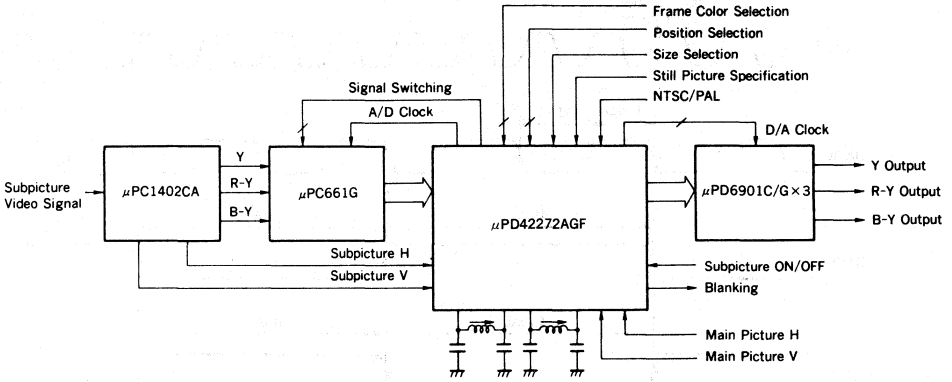
OUTPUT TIMING (5)



OUTPUT TIMING (6)



APPLICATION SYSTEM EXAMPLE



μPC1402CA ·····NTSC decoder
μPC661G····· Six-bits A/D converter
μPD6901C/G····· Six-bits D/A converter

A/D- and D/A-converter

Section 2 - A/D- and D/A-converter

Overview of A/D Converter

Device	Main application	Resolution	Conversion rate	Technology	Pins/Package
μPC659G	Video-signals	1 x 8 bit	20 MHz	Bipolar	24/SOP
μPC661G		4 x 6 bit	20 MHz	Bipolar	24/SOP
μPD7004C	CPU peripherals μCOM75 V-Series 8080, 8085	8 channels 10 bit	10 kHz	CMOS	28/DIP

Overview of A/D Converter

Device	Main application	Resolution	Conversion rate	Technology	Pins/Package
μPC662GH	Video-RGB	3 channels 8 bit	35 MHz	Bipolar	48/QFP
μPC664GS	Video Y-C-Signals	2 channels 8 bit	35 MHz	Bipolar	36/SOP
μPD6325C	TV Control signals (brightness, contrast, tone, color)	4 x 6 bit	100 kHz	CMOS	C: 16/DIP G: 16/SOP
μPD6326C		8 x 6 bit	100 kHz	CMOS	16/DIP
μPD6335C		4 x 6 bit	100 kHz	CMOS	C: 16/DIP G: 16/SOP
μPD6336C		8 x 6 bit	100 kHz	CMOS	16/DIP
μPD6900C	Video-signals	1 x 8 bit	20 MHz	CMOS	22/DIP
μPD6900C		1 x 6 bit	50 MHz	CMOS	22/DIP
μPD6900C		1 x 8 bit	50 MHz	CMOS	22/DIP
μPD7011C	CPU-Peripherals	1 x 8 bit	5 MHz	NMOS	18/DIP
μPD6376CX μPD6376GS	Digital audio	2 x 16 bit	400 kHz	CMOS	CX: 16/DIP GS: 16/SOP

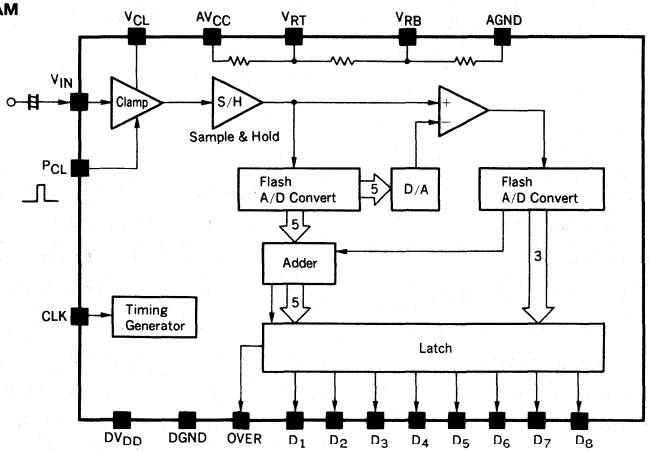
8 BIT A/D CONVERTER FOR VIDEO PROCESSING WITH REFERENCE GENERATOR AND CLAMP CIRCUIT

The μPC659 is a 8 bit A/D converter for video signal processing. The high speed and high quality Bipolar processing technology have enabled fast conversion rate and high resolution to be achieved. Conversion Rate is up to 20 MHz and Linearity Error within ±0.5 LSB while operating at low power consumption. Also, this IC include sample and hold circuit, clamp circuit and reference voltage generator, which enables simple external circuits to be constructed.

FEATURES

- Resolution: 8 bits
- Conversion Rate: 20 M_{sps} MAX.
- Differential Non-Linearity: ±0.5 LSB MAX.
- Power Supply Voltage: +5 V single
- Analog Input Voltage: 1.0 V_{p-p} TYP.
- Include Clamp Circuit (Clamp voltage and clamp pulse must be supplied.)
- Include Sample and Hold Circuit
- Include Reference Voltage Generator: V_{RT} = 3.3 V, V_{RB} = 2.3 V
- Low Power Consumption: 395 mW TYP.

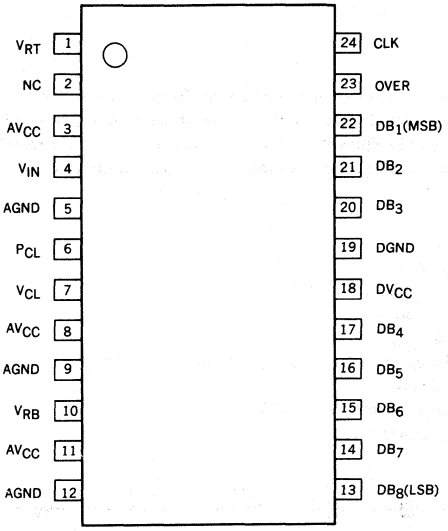
BLOCK DIAGRAM



ORDERING INFORMATION

ORDER NAME	PACKAGE
μPC659G	24 Pin Plastic SOP (300 mil)

CONNECTION DIAGRAM (Top View)



No.	Symbol	Pin Name	No.	Symbol	Pin Name
1	V_{RT}	Ref. Voltage (Top)	13	DB_8	Digital Data Output (LSB)
2	NC	No Connection	14	DB_7	Digital Data Output (7th)
3	AV_{CC}	Power Supply for Analog Circuit	15	DB_6	Digital Data Output (6th)
4	V_{IN}	Analog Signal Input Terminal	16	DB_5	Digital Data Output (5th)
5	AGND	Ground for Analog Circuit	17	DB_4	Digital Data Output (4th)
6	P_{CL}	Clamp Pulse Input Terminal	18	DV_{CC}	Power Supply for Digital Circuit
7	V_{CL}	Clamp Voltage Input Terminal	19	DGND	Ground for Digital Circuit
8	AV_{CC}	Power Supply for Analog Circuit	20	DB_3	Digital Data Output (3rd)
9	AGND	Ground for Analog Circuit	21	DB_2	Digital Data Output (2nd)
10	V_{RB}	Ref. Voltage (Bottom)	22	DB_1	Digital Data Output (MSB)
11	AV_{CC}	Power Supply for Analog Circuit	23	OVER	Digital Over Range Output
12	AGND	Ground for Analog Circuit	24	CLK	Sampling Clock Input Terminal

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	A, DV_{CC}	−0.3 to +6.0	V
Digital Input Voltage	V_{IND}	−0.3 to DV_{CC}+0.3	V
Analog Input Voltage	V_{INA}	−0.3 to AV_{CC}+0.3	V
Reference Input Voltage	V_{RT}, V_{RB}	−0.3 to AV_{CC}+0.3	V
Clamp Voltage	V_{CL}	−0.3 to AV_{CC}+0.3	V
Clamp Pulse Input Voltage	V_{PCL}	−0.3 to AV_{CC}+0.3	V
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +150	°C

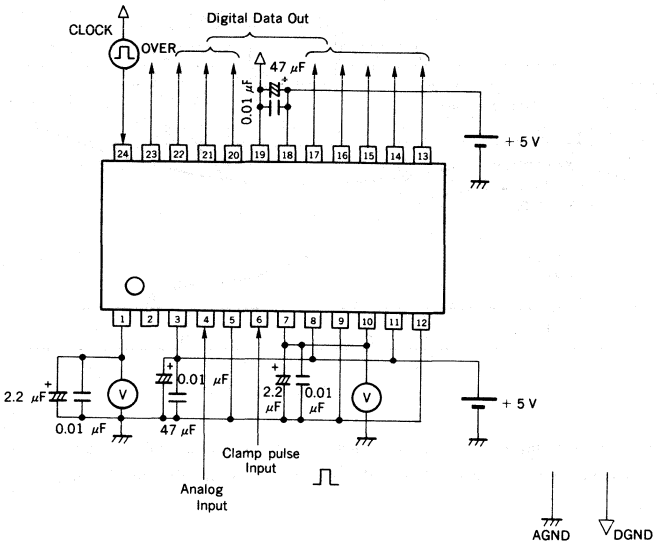
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +70 °C)

TITLE	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	AV_{CC}, DV_{CC}	4.7	5.0	5.3	V	AGND = DGND = 0
Analog Input Voltage	V_{INA}	V_{RB}−0.4		V_{RT}+0.4	V	V_{CC} = 5.0 V
Clamp Input Voltage	V_{CL}	V_{RB}−0.4		V_{RT}+0.4	V	V_{CC} = 5.0 V
Sampling Clock	f_{SAMP}	1.0		20	MHz	
Sampling Clock Low Pulse Width	t_{PWL}	25			ns	
Sampling Clock High Pulse Width	t_{PWH}	25			ns	
Clock Input High Level Voltage	V_{CKH}	2.0			V	
Clock Input Low Level Voltage	V_{CKL}			0.8	V	
Clamp Pulse Width	t_{PWCL}	1.0			μs	
Clamp Pulse High Level Voltage	V_{PCLH}	2.0			V	
Clamp Pulse Low Level Voltage	V_{PCLL}			0.8	V	
Clamp Capacitance	C_{CL}		10		μF	
Maximum Analog Input Frequency	f_{AIN}		8.0	5.0	MHz	−3 dB Point

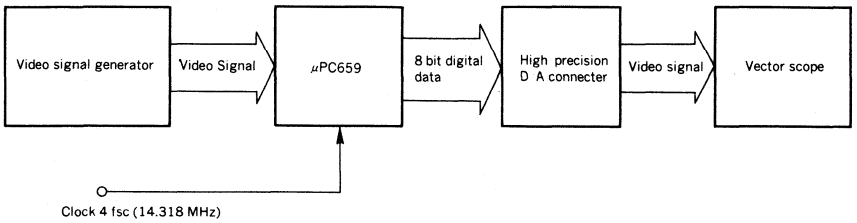
ELECTRICAL CHARACTERISTICS (T_a = −20 to + 70 °C AV_{CC} = DV_{CC} = 5.0±0.3 V)

TITLE	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Current	I_{CC}	50	79	110	mA	V_{CC} = 5.0 V, T_a = 25 °C
Resolution	RES		8		bit	
Non-linearity	NL			±1.5	LSB	V_{CC} = 5.0 V, T_a = 25 °C V_{IN} = 1.0 V_{P-P}
Differential Non-linearity	DNL			±0.5	LSB	V_{CC} = 5.0 V, T_a = 25 °C V_{IN} = 1.0 V_{P-P}
Differential Gain	DG		1.5	3.0	%	f_{SAMP} = 14.318 MHz NTSC Ramp wave (40 IRE)
Differential Phase	DP		0.8	3.0	deg	f_{SAMP} = 14.318 MHz NTSC Ramp wave (40 IRE)
Digital Data Output Delay Time	t_D		12	20	ns	Delay time from falling edge of sampling clock.
Digital Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA D_1 to D_8, OVER
Digital Output High Voltage	V_{OH}	2.7			V	I_{OH} = −400 μA D_1 to D_8, OVER
Digital Input Low Input Current	I_{INDL}			−200	μA	V_{IN} = 0.8 V
Digital Input High Input Current	I_{INDH}			10	μA	V_{IN} = 2.0 V
Analog Input Current	I_{INA}		10	35	μA	Measure input current from analog input terminal.
Reference Voltage (Bottom)	V_{RB}	2.1	2.3	2.5	V	V_{CC} = 5.0 V
Reference Voltage (Top)	V_{RT}	3.1	3.3	3.5	V	V_{CC} = 5.0 V
Analog Input Equivalent Capacitance	C_{IN}		3.0		pF	V_{IN} = V_{RB}
Clock Input Equivalent Capacitance	C_{CLK}		2.0		pF	
Reference Voltage (Difference)	V_{REF}		1.0		V	V_{RT}−V_{RB}, V_{CC} = 5.0 V

TEST CIRCUIT

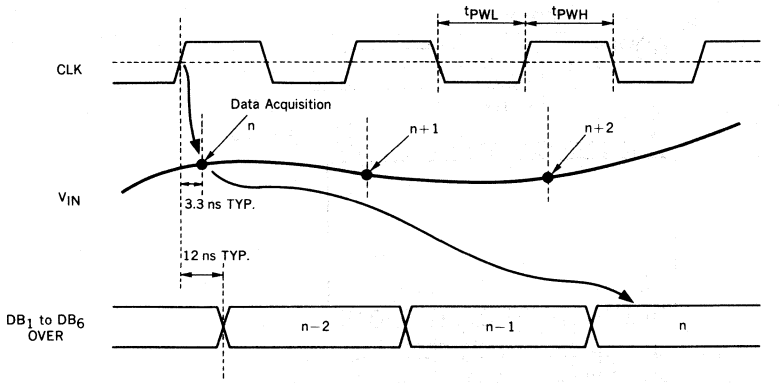


DG, DP TEST BLOCK



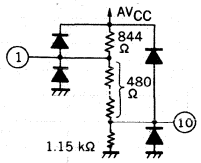
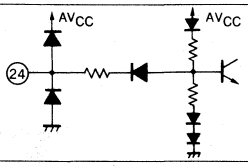
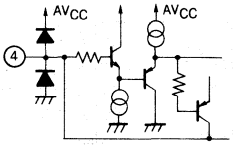
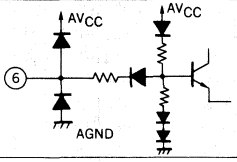
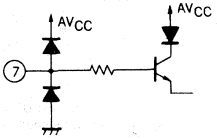
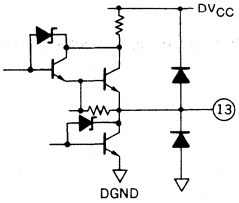
The video signal from the video signal generator is 40 IRE Ramp signal.

TIMING CHART



Analog signal is sampled with sampling clock and after the acquisition time (3.3 ns TYP.) started to be sampled. And converted data will be out after 2 sampling clock synchronized with the rise edge of sampling clock. Delay time from the rise edge of sampling clock is typically 12 ns.

EQUIVALENT CIRCUIT AROUND TERMINAL

Pin No.	Equivalent Circuit	Function
1, 10		1: Reference voltage (Top) V_{RT} 10: Reference voltage (Bottom) V_{RB}
5, 9, 12		Ground for Analog Circuit.
24		Sampling Clock input terminal. Analog data acquisition and digital data out are synchronized with the rise edge of this clock.
3, 8, 11		Power supply for analog circuit.
4		Analog signal input terminal. Input analog signal from this terminal. The clamp function also will be worked on this terminal. So it's necessary to connect capacitance and low impedance source.
6		Clamp pulse input terminal. Analog signal input from analog input terminal is clamped to the voltage; V_{CL} according to the high level term of this pulse.
7		Clamp bias input terminal. Analog input signal is clamped nearly to this input voltage; V_{CL} according to the clamp pulse; P_{CL} high level period.
13 to 17 21 to 22 23		Digital data output terminal. 13: Out of LSB data 14: Out of 7th data 15: Out of 6th data 16: Out of 5th data 17: Out of 4th data 20: Out of 3rd data 21: Out of 2nd data 22: Out of MSB data 23: Out of Over Flow (Active High)
18		Power supply for digital.
19		Ground for digital.

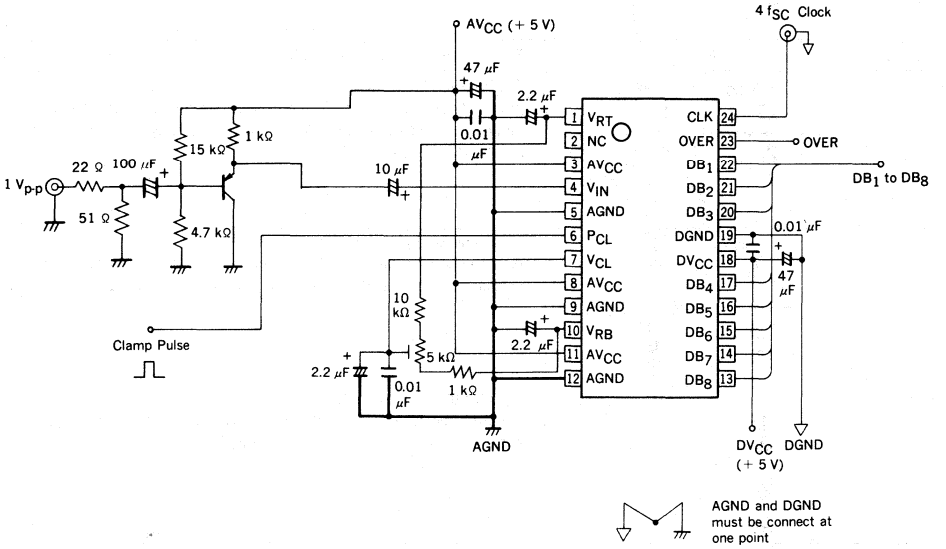
OUTPUT CODE FOR ANALOG INPUT

ANALOG INPUT	OUTPUT DIGITAL CODE								
	OVER	DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)
V_{RB} to ½ LSB	0	0	0	0	0	0	0	0	0
½ LSB to (1+½) LSB	0	0	0	0	0	0	0	0	1
to	to	to	to	to	to	to	to	to	to
(254+½) LSB to (255+½) LSB	0	1	1	1	1	1	1	1	1
(255+½) LSB to V_{RT}	1	1	1	1	1	1	1	1	1
V_{RT} to AV_{CC}	1	1	1	1	1	1	1	1	1

$$LSB \fallingdotseq \frac{V_{RT}-V_{RB}}{256} \fallingdotseq 3.906 \text{ mV TYP.}$$

V_{RB} = 2.3 V TYP.
V_{RT} = 3.3 V TYP.

APPLICATION

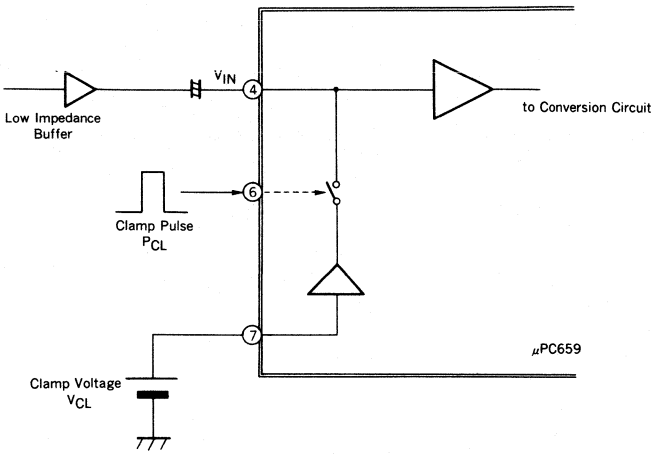


The application circuits and circuit constant described in this document don't apply to mass production where variations in parts quality and/or temperature characteristics are considered.

ATTENTION FOR APPLICATION

- Analog input terminal

  Please connect low impedance signal source to analog input terminal.
  And must be AC coupled. Clamp circuit is appeared by following rough block diagram.



- If don't use the clamp circuit

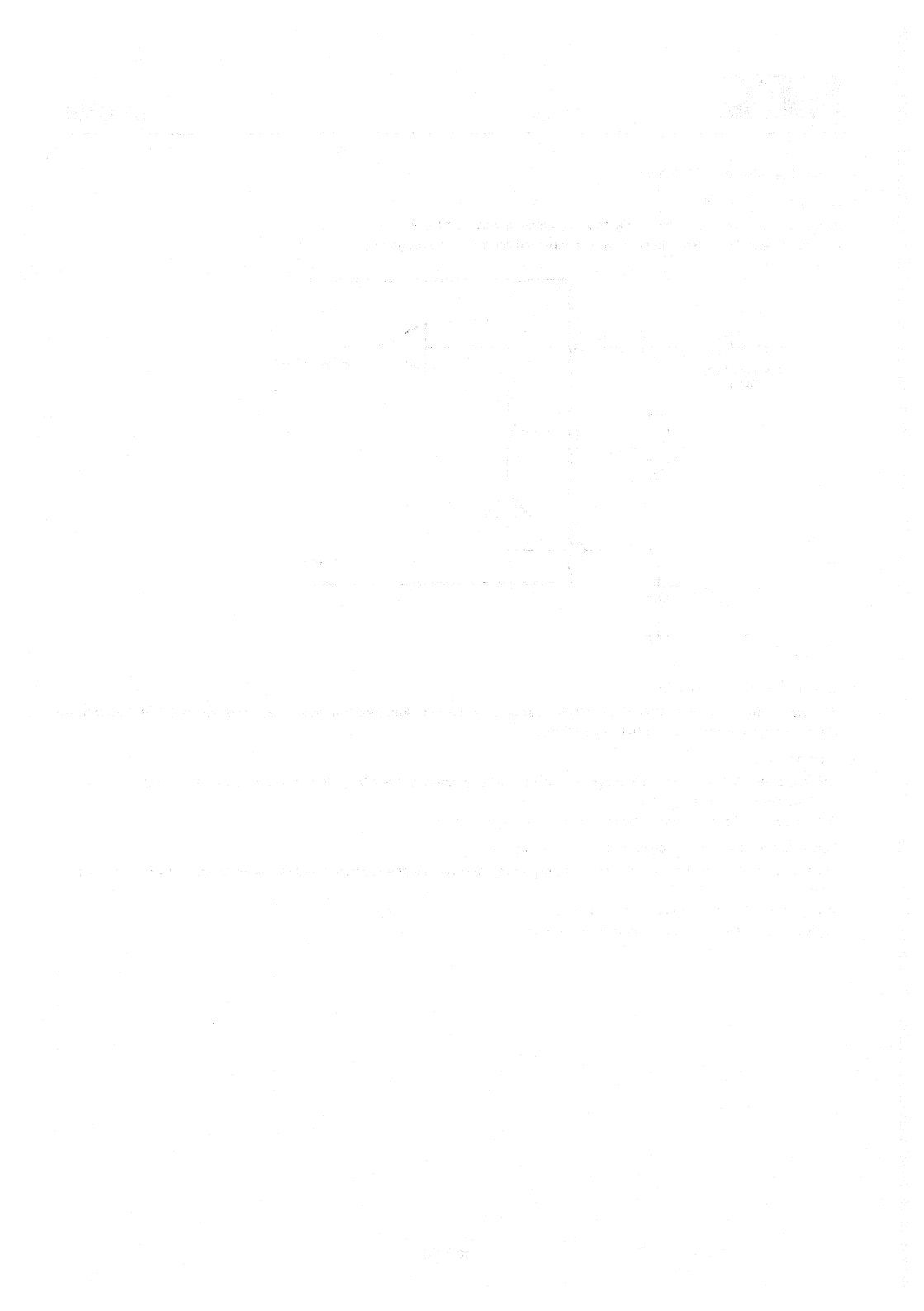
  The clamp pulse terminal (PIN 6) and GND must be short-circuit. And insert by-pass capacitor of about 0.1 μF between the clamp voltage input terminal (PIN 7) and GND.

- Clamp voltage

  There is a few difference clamp voltage between the supply clamp voltage V_{CL} (PIN 7) and really clamp voltage.
  Really clamp voltage = $V_{CL}+\alpha$
  Take account of the α (about ±20 mV) at supply V_{CL} to PIN 7

- Power supply lines for analog circuit and digital circuit

  Must be thick line wiring for the power supply lines. And reduce the resistance and reactance ingredient the power supply lines.
  AV_{CC} and DV_{CC} must be connect at one point.
  AGND and DGND must be connect at one point.



VIDEO SIGNAL PROCESSING 6-BIT A/D CONVERTER WITH BUILT-IN ANALOG MULTIPLEXER AND CLAMPER

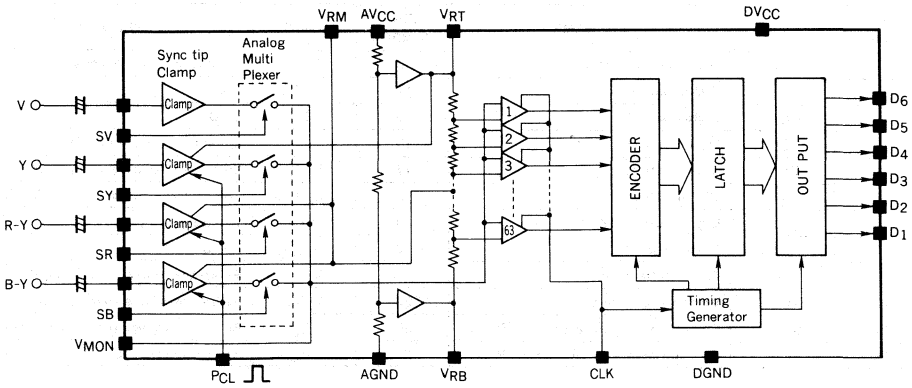
The μPC661 is a 6-bit A/D converter for video systems. The high-speed/high-precision bipolar processing technology embodied in this IC realizes 20 Msps and ±0.5 LSB (MAX.). The low power consumption design provide wide applicability of this IC to digital systems in various fields, such as digital TV systems, PIP (Picture-in-picture) system, or high speed facsimile system.

This IC has a built-in analog multiplexer for four inputs together with a clamper for each input for selective A/D conversion of video signal. In addition, a reference voltage generator is also built in for simpler circuit configurations.

CHARACTERISTICS

- Resolution: 6 bits
- Conversion rate: 20 Msps
- Non-linearity error: ±0.5 LSB
- +5 V single power supply
- Input voltage range: 1.0 V_{p-p}
- Built-in clamp circuit
- Built-in reference voltage generator: V_{RB} = 2.5 V, V_{RM} = 3.0 V, V_{RT} = 3.5 V
- Built-in analog multiplexer (for 4 inputs)
- Power consumption: 260 mW (TYP.)

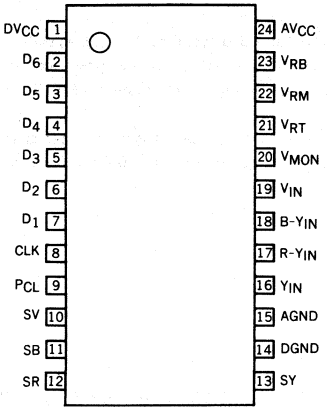
BLOCK DIAGRAM



ORDERING INFORMATION

Order name	Package
μPC661G	24-pin SOP (375 mil)

PIN CONNECTION DIAGRAM (Top View)



PIN NUMBER	SYMBOL	PIN NAME	PIN NUMBER	SYMBOL	PIN NAME
1	DV_{CC}	Digital power supply	13	SY	Luminance signal selector (Y)
2	D_6	Digital output (LSB)	14	DGND	GND
3	D_5	Digital output	15	AGND	GND
4	D_4	Digital output	16	Y_{IN}	Luminance signal input (Y)
5	D_3	Digital output	17	$R-Y_{IN}$	Color difference signal input (R−Y)
6	D_2	Digital output	18	$B-Y_{IN}$	Color difference signal input (B−Y)
7	D_1	Digital output (MSB)	19	V_{IN}	Video signal input
8	CLK	Clock input	20	V_{MON}	Analog Monitor
9	P_{CL}	Clamp pulse input	21	V_{RT}	Reference voltage (Top voltage)
10	SV	Video signal selector	22	V_{RM}	Reference voltage (Middle voltage)
11	SB	Color difference signal selector (B−Y)	23	V_{RB}	Reference voltage (Bottom voltage)
12	SR	Color difference signal selector (R−Y)	24	AV_{CC}	Analog power supply

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	AV_{CC}, DV_{CC}	−0.3 to +5.7	V
Input Voltage on Each Pin	V_I	−0.3 to V_{CC} +0.3	V
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

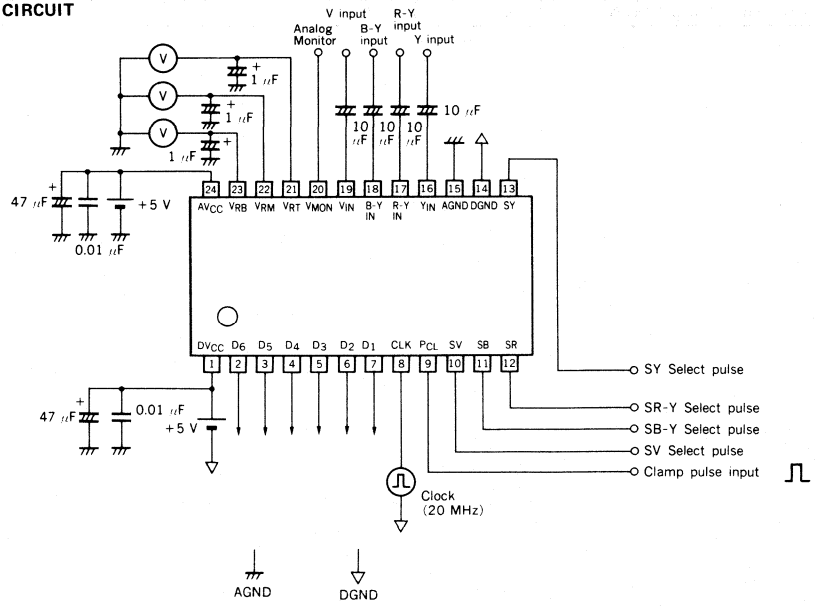
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	AV_{CC}, DV_{CC}	4.5	5.0	5.5	V	AGND = DGND = 0 V
Analog Input Voltage	V_{INA}	V_{RB}−0.4		V_{RT}+0.4	V	
Sampling Clock	f_{samp}	1		20	MHz	
Sampling Clock Low-level Pulse Width	t_{PWL}	20			ns	
Sampling Clock High-level Pulse Width	t_{PWH}	20			ns	
Select Pulse High-level Pulse Width	t_{SEH}	25			ns	
Select Pulse Low-level Pulse Width	t_{SEL}	25			ns	
Select Pulse Frequency	f_{SE}			15	MHz	
Clamp Pulse High-level Pulse Width	t_{PWCH}	1			μs	Clamp Capacitance C_{CL} = 10 μF
Clamp Pulse Low-level Pulse Width	t_{PWCL}			100	μs	Clamp Capacitance C_{CL} = 10 μF
Clamp Capacitance	C_{CL}		10		μF	
Digital Input High-level Voltage	V_{INDH}	2.0			V	
Digital Input Low-level Voltage	V_{INDL}			0.8	V	
Set Up Time at Rise of Select Pulse	t_{RS}	30			ns	
Hold Time at Rise of Select Pulse	t_{RH}	10			ns	
Set Up Time at Fall of Select Pulse	t_{fS}	30			ns	
Hold Time at Fall of Select Pulse	t_{fH}	−10			ns	

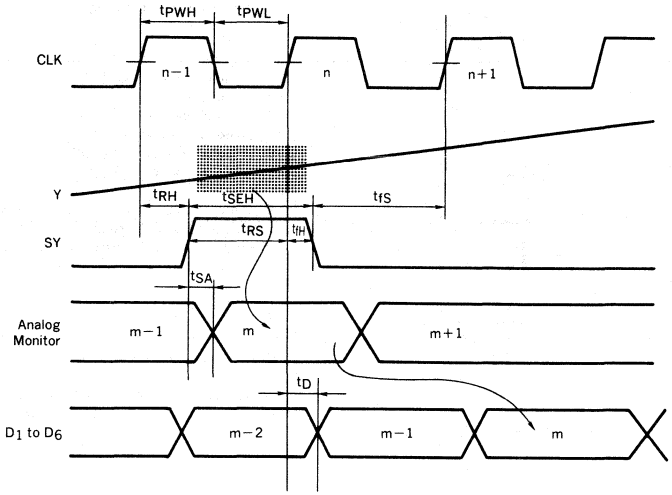
ELECTRICAL RATINGS (T_a = −20 to +75 °C, AV_{CC} = DV_{CC} = 5.0 ±0.5 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Consumption	I_{CC}	38	52	70	mA	AV_{CC} = DV_{CC} = 5.0 V, T_a = 25 °C
Nonlinearity Error	NL			±0.5	LSB	V_{CC} = 5.0 V, T_a = 0 to 60 °C V_{INA} = 1 V_{p-p} f_{samp} = 20 MHz
Differential Linearity Error	DNL			±0.5	LSB	V_{CC} = 5.0 V, T_a = 0 to 60 °C, V_{INA} = 1 V_{p-p} f_{samp} = 20 MHz
Data Output Delay Time	t_D		12	20	ns	Delay time from the rise of the clock signal, D_1 to D_6.
Digital Low-level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
Digital High-level Output Voltage	V_{OH}	2.7			V	I_{OH} = −400 μA
Digital Low-level Input Current	I_{INDL}			−500	μA	I_{INDL} = 0.8 V
Digital High-level Input Current	I_{INDH}			20	μA	V_{INDH} = 2.0 V
Reference Voltage (Bottom-voltage Side)	V_{RB}	2.2	2.5	2.8	V	V_{CCA} = 5.0 V
Reference Voltage (Middle-voltage Side)	V_{RM}	2.7	3.0	3.3	V	V_{CCA} = 5.0 V
Reference Voltage (Top-voltage Side)	V_{RT}	3.2	3.5	3.8	V	V_{CCA} = 5.0 V
Analog Input Capacitance	C_{IN}			7	pF	V_{IN} = V_{RB}
Clock Input Capacitance	C_{CLK}		2	5	pF	
Select Output Delay Time	t_{SA}		15	25	ns	Select pulse input → Analog monitor output

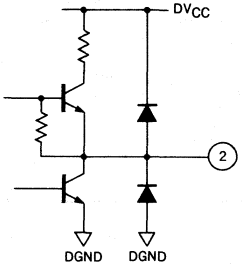
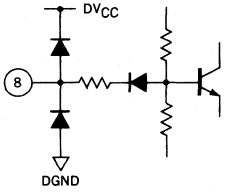
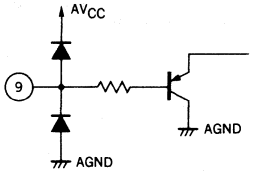
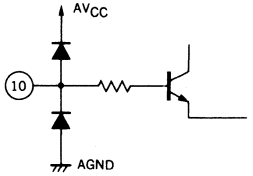
MEASUREMENT CIRCUIT

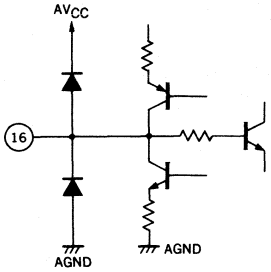
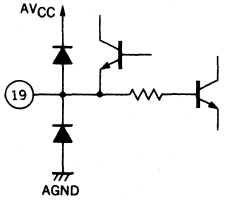
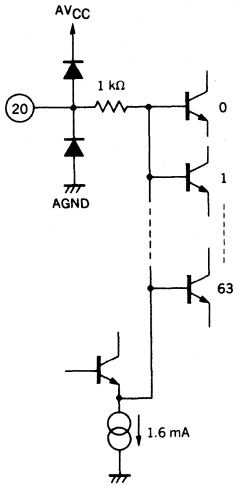


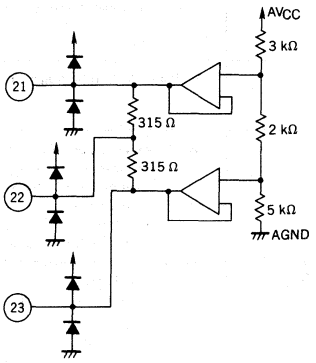
TIMING CHART



Analog monitor terminal output the analog Y signal after the Select Output Delay Time (t_{SA} = 15 ns TYP.) started to be rise high level SY terminal. In a similar timing about the timing between other analog input, select pulse and analog monitor.

PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
1		Digital system power supply
2, 3, 4, 5, 6, 7		2: Digital data output (LSB) 3: Digital data output (5th) 4: Digital data output (4th) 5: Digital data output (3rd) 6: Digital data output (2nd) 7: Digital data output (MSB) Digital data output terminals. The data is output one digital output delay period (t_D) after the rise of the clock. (Refer to the Timing Chart). Output at the TTL level.
8		Clock signal input terminal. Analog input is fetched and digital data is output at the rise of the signal input to this terminal.
9		Clamp pulse input terminal for color difference signal (R−Y, B−Y) and luminance signal (Y). The signal is clamped when this terminal is high. And at this time output digital data is fixed the following code. At Y or V Select : "000000" At R−Y or B−Y Select: "100000"
10, 11, 12, 13		10: Analog multiplexer switching signal input (SV). This terminal selects the signal from the V_{IN} terminal (Pin 19) while this terminal is high. 11: Analog multiplexer switching signal input (SB). This terminal selects the signal from the $B-Y_{IN}$ terminal (Pin 18) while this terminal is high. 12: Analog multiplexer switching signal input (SR). This terminal selects the signal from the $R-Y_{IN}$ terminal (Pin 17) while this terminal is high. 13: Analog multiplexer switching signal input (SY). This terminal selects the signal from the Y_{IN} terminal (Pin 16) while this terminal is high. Analog multiplexer switching signals (select pulses) don't input more than one high level at the sametime. At select pulses are all low level, the output digital data code is "000000" by compulsion.

PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
14		Digital system grounding terminal.
15		Analog system grounding terminal.
16, 17, 18		16: Luminance signal (Y) input terminal and clamper. Input level : 1 V_{p-p} Clamping level: V_{RT} 17: R–Y input terminal and clamper. Input level : 1 V_{p-p} Clamping level: V_{RM} 18: B–Y input terminal and clamper. Input level : 1 V_{p-p} Clamping level: V_{RM}
19		Composite video signal input terminal and clamper. Input level: 1 V_{p-p} The clamp is a Sync-tip (minimum value) clamp. The clamping level make other circuit that reference voltage (V_{RT}, V_{RM}). There is a few difference clamp voltage between the really clamping level (V_{20}) and V_{RT}.
20		Analog multiplexer output monitor terminal. This terminal monitors the input signal selected by pins 10 to 13. This terminal is normally open.

PIN NUMBER	EQUIVALENT CIRCUIT DIAGRAM	DESCRIPTION OF FUNCTIONS
21 22 23		21: Reference voltage output terminal (Top voltage side). V_{RT}. 22: Reference voltage output terminal (Middle voltage side). V_{RM}. 23: Reference voltage output terminal (Bottom voltage side). V_{RB}.
24		24: Analog system power supply.

OUTPUT CODE FOR ANALOG INPUT

ANALOG INPUT (V_{IN}, Y_{IN}, R–Y_{IN}, B–Y_{IN})	OUTPUT DIGITAL CODE					
	DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6 (LSB)
V_{RB} to ½LSB	0	0	0	0	0	0
½LSB to (1 + ½) LSB	0	0	0	0	0	1
⟩	⟩	⟩	⟩	⟩	⟩	⟩
(62 + ½) LSB to (63 + ½) LSB	1	1	1	1	1	1
(63 + ½) LSB to V_{RT}	1	1	1	1	1	1
V_{RT} to AV_{CC}	1	1	1	1	1	1

$$LSB \fallingdotseq \frac{V_{RT} - V_{RB}}{64}$$

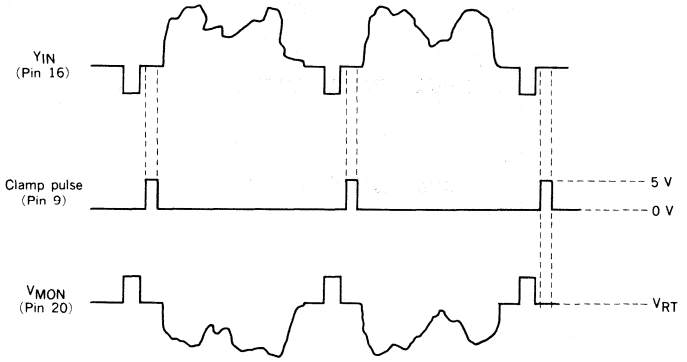
SUPPLEMENT

Clamp Operation

This IC has a built-in clamper that clamps using the coupling capacitance of the respective analog signal input terminals 16 to 19.

1) Clamping of the video signal input, V_{IN} (Pin 19)
The clamping here is based on the minimum value clamping system, which is mainly used for clamping the video sink chip. The voltage during clamping is generated by the internal regulator. Note that this clamper operates independently from the clamp pulse on the pin 9. But at clamp pulse is high-level, the output digital data code is "000000" by compulsion.

2) Clamping of the luminance signal input, Y_{IN} (Pin 16)
Clamping here is executed when the clamp pulse on pin 9 is high. When the clamp pulse is high, the signal voltage supplied from the pin 16 is clamped to V_{RT} (reference high voltage) at the V_{INA} terminal (Pin 20). The timing and the level of the clamping by the pedestal are as follows:
Note that at clamp pulse is high-level, the output digital data code is "000000" by compulsion.



3) Clamping of the color difference signals: $R-Y_{IN}$ (Pin 17) and $B-Y_{IN}$ (Pin 18)
This clamping is executed while the clamp pulse at pin 9 is high. When the clamp pulse is high, the signal voltage supplied from the pin 17 or 18 is clamped to V_{RM} (intermediate reference voltage) at the V_{IN} (Pin 20) terminal.
Note that at clamp pulse is high-level, the output digital data code is "100000" by compulsion.

4) Output digital code for select pulse and clamp pulse

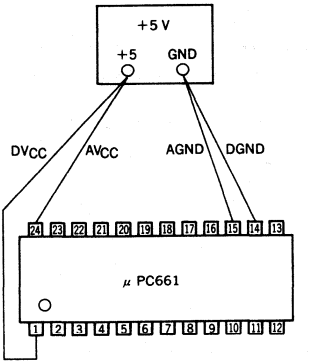
INPUT SELECT PULSE				CLAMP PULSE	OUTPUT DIGITAL CODE					
SV	SY	SR	SB	P_{CL}	D_1	D_2	D_3	D_4	D_5	D_6
0	0	0	1	0	$B-Y_{IN}$ A/D Converted Code					
0	0	1	0	0	$R-Y_{IN}$ A/D Converted Code					
0	1	0	0	0	Y_{IN} A/D Converted Code					
1	0	0	0	0	V_{IN} A/D Converted Code					
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	0	0
0	0	1	0	1	1	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0

Notes: "1": High level
"0": Low level

ATTENTION FOR APPLICATION

- Analog input terminal
  Please connect low impedance signal source to analog input terminal. And must be AC coupled.

- Power supply lines for analog circuit and digital circuit.
  Must be thick line wiring for the power supply lines. And reduce the resistance and reactance ingredient the power supply lines.
  AV_{CC} and DV_{CC} must be connect at one point.
  AGND and DGND must be connect at one point.



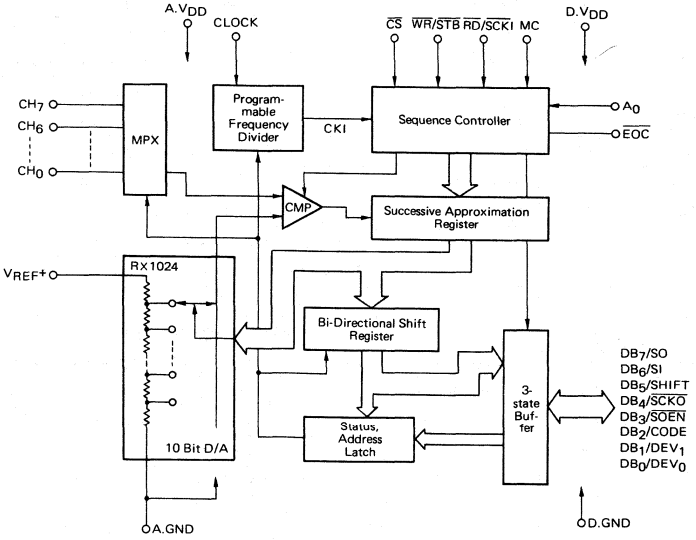
10-BIT CMOS SUCCESSIVE APPROXIMATION A/D CONVERTER

The μPD7004 is a 10-bit monolithic CMOS analog-to-digital converter using the Successive Approximation Register (SAR) technique. The μPD7004 incorporates an 8-channel multiplexed analog input and full microprocessor interface to achieve a high degree of versatility. The designer has a choice of either serial or parallel output and interface to 8080 type microprocessors or advanced signal processors like the μPD7720.

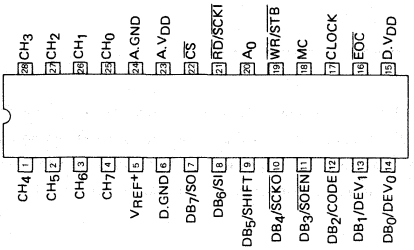
FEATURES

- 8-channel multiplexed analog input
- Serial or parallel interface
- 10-bit resolution
- Linearity: 1 LSB MAX. (T_a = 25 °C)
- Conversion time: 104 μs (f_{CKI} = 1 MHz)
- Input voltage range 0 to V_{REF}
- Temperature range from -40 to +85 °C
- Operates from single +5 volt supply (5 V ±10 %)

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



PIN IDENTIFICATION

Pin No.	Sumbol	Parallel mode		Serial mode	
		I/O	Function	I/O	Function
1	CH_4		Analog input CH_4		
2	CH_5		Analog input CH_5		
3	CH_6		Analog input CH_6		
4	CH_7		Analog input CH_7		
5	$V_{REF}+$		Positive reference voltage input		
6	D.GND		Digital Ground Note		
7	BD_7/SO	Output	Data bus (MSB)	Output	Serial output
8	DB_6/SI	Output	Data bus (2nd)	Input	Serial input
9	DB_5/SHIFT	Output	Data bus (3rd)	Input	First-bit select (LSB/MSB)
10	$DB_4/\overline{SCKO}$	Output	Data bus (4th)	I/O	Serial clock output
11	$DB_3/\overline{SOEN}$	Output	Data bus (5th)	I/O	Serial-out enable
12	DB_2/CODE	I/O	Data bus (6th)	Input	Code select
13	DB_1/DEV_1	I/O	Data bus (7th)	Input	Division ratio set
14	DB_0/DEV_0	I/O	Data bus (LSB)	Input	Division ratio set
15	D.V_{DD}		Digital Power Supply Note		
16	$\overline{EOC}$	Output	End-of-conversion signal (Active low)		
17	CLOCK	Input	Clock signal input terminal		
18	MC	Input	Mode select (H=Parallel, L=Serial)		
19	$\overline{WR}/\overline{STB}$	Input	Write signal input	Input	Address-write strobe signal
20	A_0	Input	Control address input	Input	Internal/external serial clock select
21	$\overline{RD}/SCKI$	Input	Read signal input	Input	Serial clock input
22	$\overline{CS}$	Input	Chip select signal		
23	A.V_{DD}		Analog Power Supply Note		
24	A.GND		Analog Ground Note		
25	CH_0		Analog input CH_0		
26	CH_1		Analog input CH_1		
27	CH_2		Analog input CH_2		
28	CH_3		Analog input CH_3		

Note: Connect to Digital Ground (D.GND) with Analog Ground (A.GND) externally.
Connect to Digital Power Supply (D.V_{DD}) with Analog Power Supply (A.V_{DD}) externally.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.3	V
Reference Voltage	V_{REF}	-0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -40 to +85 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	4.0		V_{DD}	V	
Analogue Input Voltage	V_I	0.0		V_{REF}	V	
High-level Input Voltage	V_{IH}	2.4			V	
Low-level Input Voltage	V_{IL}			0.8	V	
Clock Frequency	f_{CK}	0.4		8.8	MHz	
Internal Clock Frequency	f_{CKI}	0.4	1.0	1.1	MHz	$f_{CKI} = f_{CK}$ × Division ratio
Parallel Mode (MC = High)						
Address Setup Time	t_{AW}	20			ns	$\overline{CS}\downarrow$, $A_0 \rightarrow \overline{WR}\downarrow$
	t_{AR}	20			ns	$\overline{CS}\downarrow$, $A_0 \rightarrow \overline{RD}\downarrow$
Address Hold Time	t_{WA}	10			ns	$\overline{WR}\uparrow \rightarrow \overline{CS}\uparrow$, A_0
	t_{RA}	10			ns	$\overline{RD}\uparrow \rightarrow \overline{CS}\uparrow$, A_0
$\overline{WR}$ Signal Pulse Width	t_{WW}	200			ns	
$\overline{RD}$ Signal Pulse Width	t_{RR}	200			ns	
Data Setup Time	t_{DW}	100			ns	$DB \rightarrow \overline{WR}\uparrow$
Data Hold Time	t_{WD}	20			ns	$\overline{WR}\uparrow \rightarrow DB$
Serial Mode 1 (MC = Low, A_0 = Low; External Serial Clock)						
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}\downarrow \rightarrow \overline{CS}\downarrow$
$\overline{CS}$ Setup Time	t_{SCSK}	1			μs	$\overline{CS}\downarrow \rightarrow \overline{SCKI}\downarrow$ (*)
Serial Input Setup Time	t_{SIK}	150			ns	$SI \rightarrow \overline{SCKI}\uparrow$
Serial Input Hold Time	t_{HKI}	100			ns	$SCKI\uparrow \rightarrow SI$
Low-level Serial Clock Pulse Width	t_{WLK}	400			ns	
High-level Serial Clock Pulse Width	t_{WHK}	400			ns	
Strobe Pulse Width	t_{WLST}	200			ns	
Strobe Hold Time	t_{HKST}	200			ns	$\overline{SCKI}\uparrow \rightarrow \overline{STB}\uparrow$
Chip Select Hold Time	t_{HKCS}	100			ns	$\overline{SCKI}\uparrow \rightarrow \overline{CS}\uparrow$

* f_{CKI} = 1 MHz

↑ ... Rising edge
↓ ... Falling edge

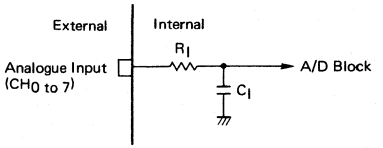
CONVERSION CHARACTERISTICS (T_a = 25 °C, V_{DD} = V_{REF} = 5.0 ±0.5 V, f_{CKI} = 1 MHz)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Resolution		10	10	10	Bit	T_a = -40 to +85 °C
Total Unajusted Error	NL			±1.0	LSB	
Total Unajusted Error				±2.0	LSB	T_a = -40 to +85 °C
Zero Scale Error				±0.5	LSB	
Zero Scale Temperature Coefficient			2		ppm/°C	T_a = -40 to +85 °C
Full Scale Error				±0.5	LSB	
Full Scale Temperature Coefficient			2		ppm/°C	T_a = -40 to +85 °C
Conversion Time	T_{CONV}	96		104	μs	Parallel Mode, Serial Mode 1
Conversion Time	T_{CONV}	104	104	104	μs	Serial Mode 2

DC CHARACTERISTICS (V_{DD} = V_{REF} = 5.0 ±0.5 V, T_a = -40 to +85 °C, f_{CKI} = 1 MHz)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
High-level Output Voltage	V_{OH}	3.5			V	I_O = -1.6 mA
Low-level Output Voltage	V_{OL}			0.4	V	I_O = 1.6 mA
Digital Input Leakage Current	I_{ID}			±10	μA	V_I = 0 to V_{DD}
Floating Output Leakage Current	I_{FO}			±10	μA	V_O = 0 to V_{DD}
Analog Input Resistance (DC)	R_I (DC)		2		MΩ	V_I = 0 to V_{DD}
Equivalent Analog Input Impedance (*)	RI		10		kΩ	The analogue input impedance is equivalent to the series circuit between RI and CI.
	CI		100		pF	
Reference Input Resistance	R_{REF}	5		50	kΩ	
Power Consumption	P_d		5	15	mW	

* Equivalent Circuit



Charge or discharge current flows at the internal multiplexer switching timing. Therefore, connect a capacitor (>0.01 μF) to the analog input terminal in case the external is high.

AC CHARACTERISTICS ($V_{DD} = V_{REF} = 5 \pm 0.5$ V, $T_a = -40$ to $+85$ °C, $f_{CKI} = 1$ MHz)

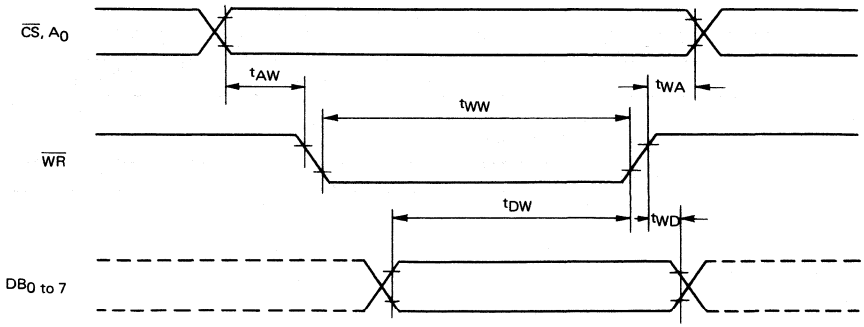
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Output Delay Time	t_{RD}			150	ns	$\overline{RD}$ ↓ → DB (Parallel Mode)
	t_{DKO}			250	ns	$\overline{SCKI}$ ↓, $\overline{SCKO}$ ↓ → SO (Serial Mode 1, 2)
Output Floating Delay Time	t_{DF}			100	ns	$\overline{RD}$ ↑ → DB Floating (Parallel Mode)
	t_{FCSO}			150	ns	$\overline{CS}$ ↑ → SO Floating (Serial Mode 1)
Serial-out Enable Delay Time	t_{SKS}	40		200	ns	$\overline{SCKO}$ ↑ → $\overline{SOEN}$ ↓ (Serial Mode 2)
Serial-out Enable Delay Time	t_{HKS}	0		200	ns	$\overline{SCKO}$ ↓ → $\overline{SOEN}$ ↑ (Serial Mode 2)
Serial Clock Output Cycle	t_{CYK}		$1/f_{CKI}$		ns	(Serial Mode 2)
High-level Serial Clock Pulse Width	t_{WHK}	400			ns	(Serial Mode 2)
Low-level Serial Clock Pulse Width	t_{WLK}	400			ns	(Serial Mode 2)
Serial Clock Rise Time	t_{rsc}		20		ns	(Serial Mode 2)
Serial Clock Fall Time	t_{fsc}		20		ns	(Serial Mode 2)

↑ ... Rising edge
↓ ... Falling edge

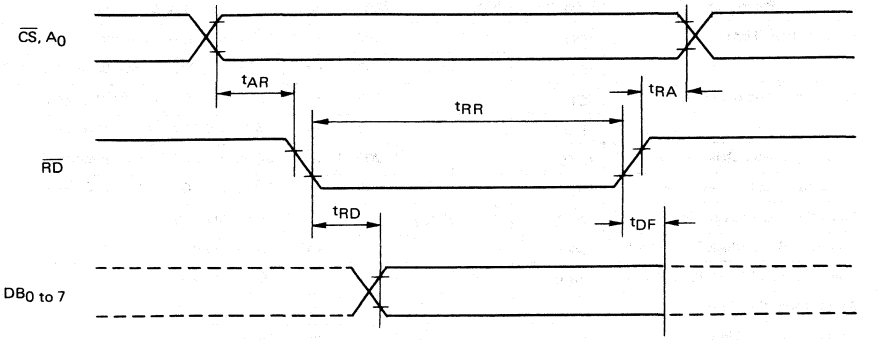
TIMING CHART

1. Parallel Mode

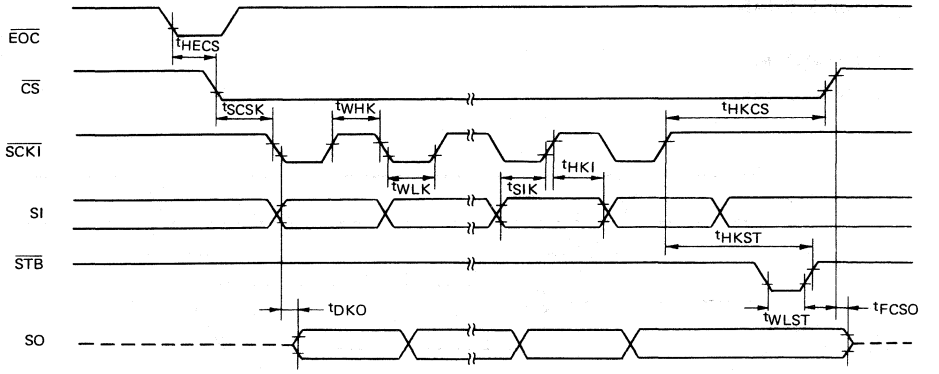
(1) Write Mode



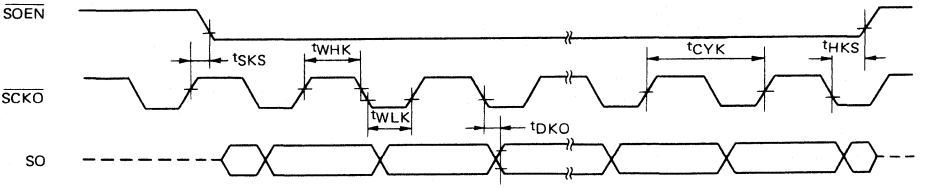
(2) Read Mode



2. Serial Mode 1



3. Serial Mode 2



INTERNAL BLOCK OPERATION

1. Sequence Controller

The sequence controller controls the operation of the comparator, internal sequence of the successive approximation register, and the 3-state buffers.

The A/D conversion starts in the parallel mode when the MPX address is written, and in the serial mode when the $\overline{CS}$ signal changes to the high level.

When the A/D conversion is terminated, the sequence controller issues an end-of-conversion signal ($\overline{EOC}$) to notify this to the external environment.

2. Successive Approximation Register

The successive approximation register sends signals to the decoder of the 10-bit D/A according to the control signals from the sequence controller and then decides to set or reset the signals for the decoder, starting with the MSB, with the help of the results from the comparator.

3. Bi Directional Shift Resister

This is the register into which the contents of the successive approximation register are entered. It outputs the converted data via 3-state buffers when in the parallel mode.

In serial mode 1, it outputs the converted data from the SO terminal when the $\overline{SIKI}$ signal falls and the $\overline{CS}$ signal is low, and fetches serial data (MPX address selector data) from the SI terminal when the $\overline{SCKI}$ signal rises.

In serial mode 2, 10-bit converted data accompanied by 6-bit high data is output from the SO terminal synchronously from the falling edge of the $\overline{SCKO}$ signal.

4. Status, Address Latch

The status and address latch are 3-bit registers to latch the clock division selector ratio data, code selector data of the conversion data, and selector data for the MPX address.

It reads the data entered from the data buses ($DB_{0\ to\ 7}$) in the parallel mode. In serial mode, it latches the division ratio selector data and code selector data specified by the multi-function terminals (DB_0/DEV_0, DB_1/DEV_1, DB_2/CODE) and also the MPX address selector data entered through the SI terminal.

However, that the MPX address is fixed at CH_7 and cannot be selected in serial mode 2.

5. Programmable Frequency Divider

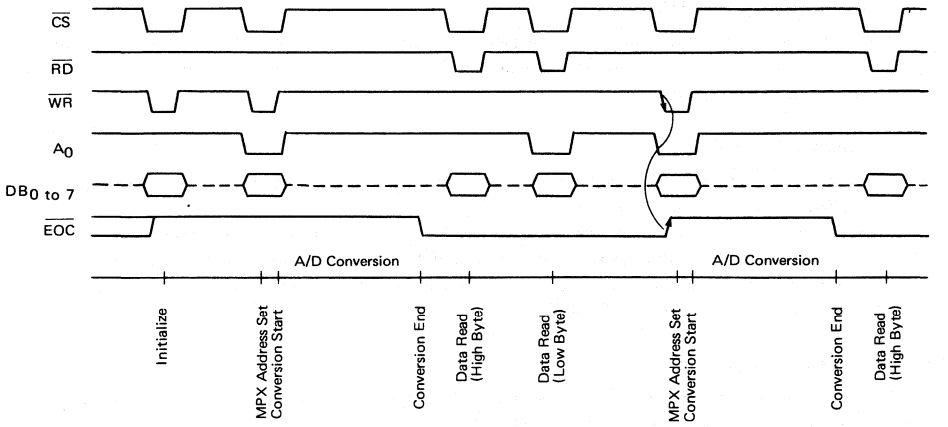
The programmable frequency divider designates clock signals entered from the external circuit to one of the ratios 1/1, 1/2, 1/4, and 1/8.

OPERATING MODE

The μPD7004, serving as an interface circuit with the microcomputer, supports two kinds of serial modes and a parallel mode.

1. Parallel Mode

The parallel mode allows a direct connection to the microprocessor data buses. Shown below is an example of the basic sequence;



The initialization designates the clock signal division ratio for the clock signal entered from the external environment and the conversion data code (2' s complement/binary). Normally, initialization is performed to initialize the peripheral circuits of the microcomputer. After initialization, the data entered is held until the next initialization. Writing the MPX address into the μPD7004 ($\overline{WR}$ signal) after the initialization makes the A/D conversion start from the rising edge of $\overline{WR}$ signal.

The A/D conversion requires f_{CKI} (internal clock: f_{CK} X division ratio) to be 96 to 104 cycles. The $\overline{EOC}$ signal changes to the low level when the A/D conversion is complete to notify this to the external environment. The 10-bit converted data is read out from the μPD7004 eight bits at a time. The low byte has valid data in its two high-order bits, followed by six "0"s in the rest (DB_5 to DB_0).

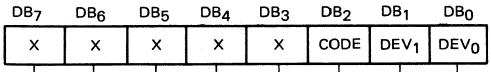
Resetting the MPX address starts the next A/D conversion, changing the $\overline{EOC}$ signal to the high level at the falling edge of $\overline{WR}$ signal.

Data Bus I/O Operation (parallel mode MC = H)

Control terminal				Operation	Serves as a data bus terminal
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0		
H	X	X	X	No Operation	High-impedance State
L	H	H	X		
L	L	H	H	Initialize	Code Select, Clock Division Ratio Input
L	L	H	L	Address Set	Analogue Channel Select Data Input
L	H	L	H	High-byte Read	High-byte Data Output
L	H	L	L	Low-byte Read	Low-byte Data Output
L	L	L	X	Inhibit	–

(1) Initialize

In the parallel mode, the initialization data for the clock division ratio and the A/D conversion data code are written into the μPD7004 through data buses.



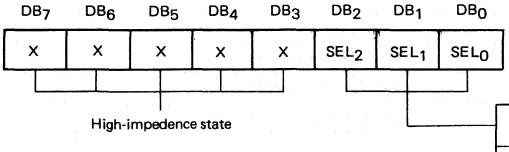
DEV_1	DEV_0	Clock Division Ratio
L	L	1/1
L	H	1/2
H	L	1/4
H	H	1/8

CODE	Code Select
L	Binary Data
H	2's Complement Data

Data written at the initialization is held afterwards.

(2) Address set

The selector data for the analog channel is written into the μPD7004.



SEL_2	SEL_1	SEL_0	MPX Channel
L	L	L	CH_0
L	L	H	CH_1
L	H	L	CH_2
L	H	H	CH_3
H	L	L	CH_4
H	L	H	CH_5
H	H	L	CH_6
H	H	H	CH_7

(3) High-byte/low-byte read

The A/D conversion data is read from the μPD7004.

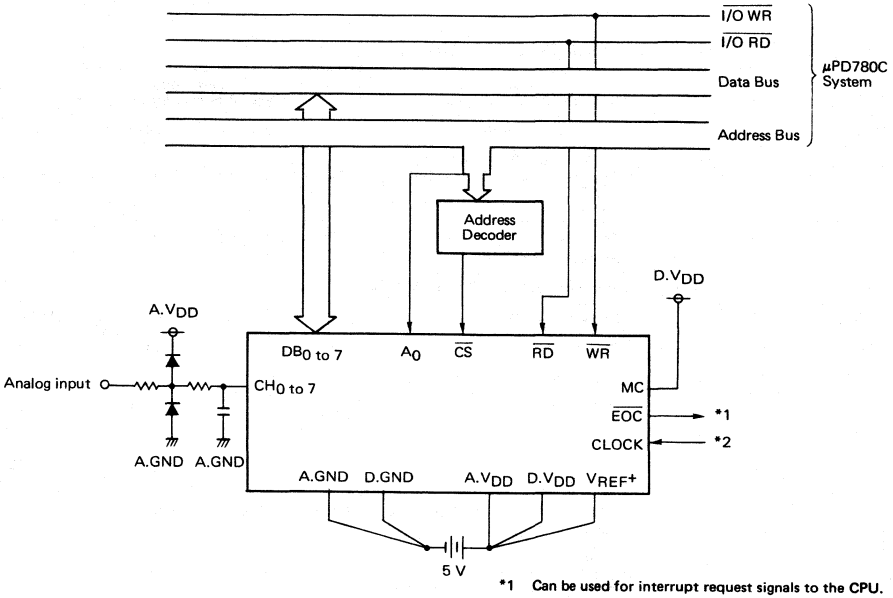
	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
High-byte	MSB	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Low-byte	9TH	LSB	L	L	L	L	L	L

EXAMPLE OF THE PARALLEL MODE INTERFACE

Fig. 1 shows an example of connecting the μPD7004C to the μPD780C system. As shown in the example, the parallel mode can handle connections using such basic interface circuits as microcomputer peripheral LSIs.

In this example, the μPD780C is employed as a CPU. It is also possible to have other 8-bit CPUs connected in the same logic design, with some timing management by the wait cycle.

Fig. 1 μPD780C/μPD7004C connection



*1 Can be used for interrupt request signals to the CPU.

*2 Can apply a clock to the CPU. (up to 8 MHz)

2. Serial Mode

The serial mode includes serial mode 1 and serial mode 2. Described below are the functions of terminals operating in each mode.

SERIAL I/O OPERATION (Serial Mode 1, 2, MC = L)

Symbol	Pin No.	Serial Mode 1 (External Serial Clock, A_0 = L)		Serial Mode 2 (Signal Processor Mode, A_0 = H)	
		I/O	Function	I/O	Function
SO	7	Output	Serial output (three state). Data are output at the falling edge of $\overline{SCKI}$ or $\overline{SCKO}$.		
SI	8	Input	Serial Input. Data read at the rising edge of $\overline{SCKI}$ or $\overline{SCKO}$.	Input	Connect to V_{DD}
SHIFT	9	Input	Shift Select (H: LSB first, L: MSB first)		
$\overline{SCKO}$	10	–	Connect to GND	Output	Serial Clock Output (= Internal Clock)
$\overline{SOEN}$	11	–	Connect to GND	Output	Serial Output Enable (= Active Low)
CODE	12	Input	Code Select (H = 2' s complement, L = Binary)		
DEV 1	13	Input	Division Ratio Setting		
DEV 0	14	Input			

DEV_1	L	L	H	H
DEV_0	L	H	L	H
Division Ratio	1/1	1/2	1/4	1/8

$\overline{STB}$	19	Input	Address strobe Input MPX addresses are latched at the rising edge of $\overline{STB}$ Input.	Input	Connect to GND
$\overline{SCKI}$	21	Input	$\overline{SCKI}$ controls the shift operation of I/O interface shift register. Data are output at the falling edge, and input at the rising edge.	–	Connect to V_{DD}
$\overline{CS}$	22	Input	Chip select signal input. Low level of $\overline{CS}$ resets the internal sequence, and I/O interface is enabled.	Input	Internal sequence reset signal input. Sequence controller are reset at the low level of $\overline{CS}$, and A/D conversion starts at the rising edge of $\overline{CS}$.

Notes: 1. In serial mode 1, the following signals are strobed by the $\overline{CS}$ signal. Therefore, the input signals are ignored and the output terminals become high impedance when $\overline{CS}$ = HIGH.

Input Terminal: SI, $\overline{STB}$, $\overline{SCKI}$

Output Terminal: SO

2. In serial mode 2, the internal sequence reset signal ($\overline{CS}$) specifies CH_7.

2.1 Serial Mode 1

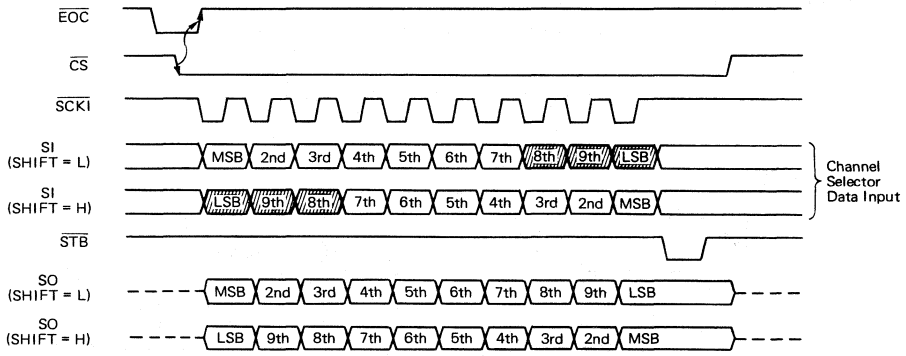
Serial mode 1 supports the serial data I/O when the $\overline{CS}$ signal is at the low level, outputs the serial data from the falling edge of the serial clock signal ($\overline{SCKI}$) entered from the external circuit, and fetches the serial input data at the rising edge of the $\overline{SCKI}$ signal.

If the MSB-first data is specified (SHIFT = L), the last three bits of the 10-bit serial input data for the MPX address selection contain valid data. If the LSB-first data is specified (SHIFT = H), the first three bits of the 10-bit data for the MPX address selection contain valid data. This MPX address data latch in the μPD7004C is implemented when at the rising edge of the $\overline{STB}$ signal. The latch can also be achieved at the rising edge the $\overline{CS}$ signal, if the $\overline{STB}$ signal is fixed at the low level.

The A/D conversion starts from the rising edge of $\overline{CS}$ signal. The $\overline{EOC}$ signal changes to the low level at the end of the conversion to notify this to the external environment. The time required for the A/D conversion is the same as that required in the parallel mode. The $\overline{EOC}$ signal changes to the high level from the falling edge of $\overline{CS}$ signal.

The A/D conversion is repeatedly operated when the $\overline{CS}$ signal stays in the high-level and the $\overline{EOC}$ signal remains in the low-level.

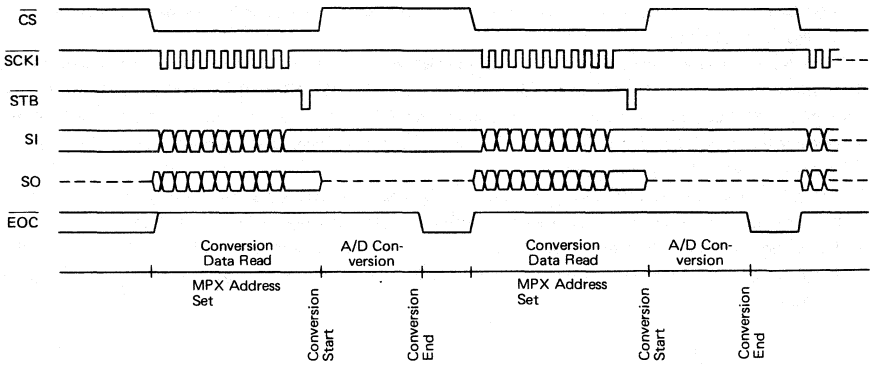
Serial Mode 1 Timing Chart



The 3 low-order bits of the serial input data serve as channel selection data.

8th	L	L	L	L	H	H	H	H
9th	L	L	H	H	L	L	H	H
LSB	L	H	L	H	L	H	L	H
Channel	CH_0	CH_1	CH_2	CH_3	CH_4	CH_5	CH_6	CH_7

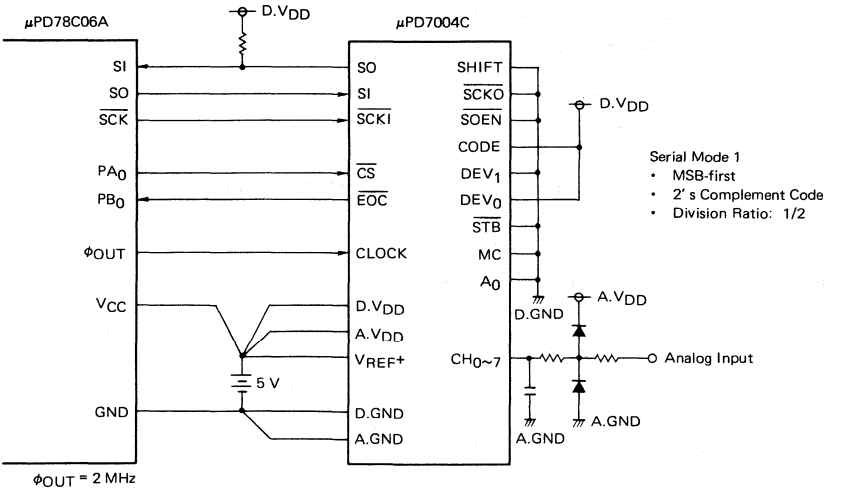
Serial Mode 1 Sequence Timing Chart



Example of the Interface with the μPD78C06A

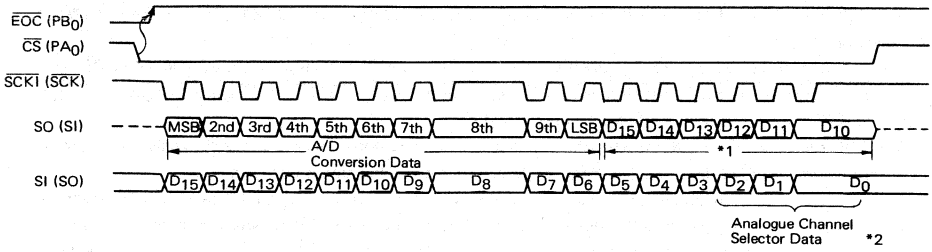
Fig. 2 shows an example of the interface with the μPD78C06A

Fig. 2 μPD7004C/μPD78C06A connection



μPD78C06A contains a serial interface circuit and handles 8-bit data transfer. Therefore, the μPD78C06A operates 8-bit data transfer twice to handle the μPD7004C's 10-bit serial data transfer. The timing of the data transfer is shown in Fig. 3.

Fig. 3 Timing in serial mode 1 (connection with μPD78C06A)



*1 The data entered through the SI terminal is output from SO.

*2 Channel selector data is latched at the rising edge of the CS signal when the STB signal is fixed at the low level.

Channel selector data

D_2	L	L	L	L	H	H	H	H
D_1	L	L	H	H	L	L	H	H
D_0	L	H	L	H	L	H	L	H
Channel	CH_0	CH_1	CH_2	CH_3	CH_4	CH_5	CH_6	CH_7

2.2 Serial Mode 2

Serial mode 2 allows direct connection to the serial interface of the signal processor μPD7720AC.

Shown on the right is an example of connecting principal terminals between the μPD7004C and μPD7720AC. Serial mode 2 differs from the other two modes. This mode cannot specify the MPX address to the μPD7004C since the address is fixed at CH_7.

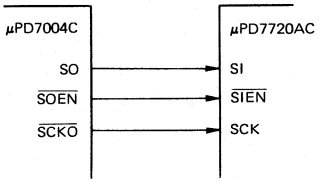
Although the data through the A/D conversion consists of 10 bits, it is followed by six bits of high data when it is output as serial data.

These six bits of high data always follow the converted data for MSB-first or LSB-first. (Refer to the Serial Mode 2 Timing Chart.)

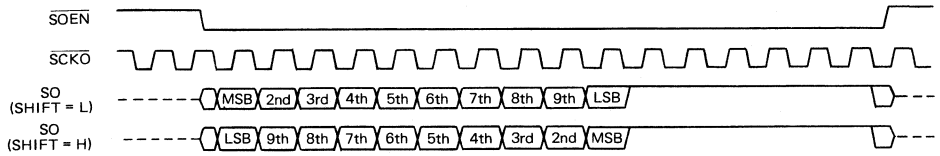
The A/D conversion sequence starts upon the initialization. The initialization is operated by holding the $\overline{CS}$ signal at the low level for more than eight clock cycles. The A/D conversion starts when the $\overline{CS}$ signal changes to the high-level. The A/D conversion requires 104 clock pulses (f_{CKI}).

The $\overline{EOC}$ signal, as in the other modes, changes to the low level to notify the end of the conversion to the external environment. The $\overline{EOC}$ signal remains at the low level until the initialization is implemented.

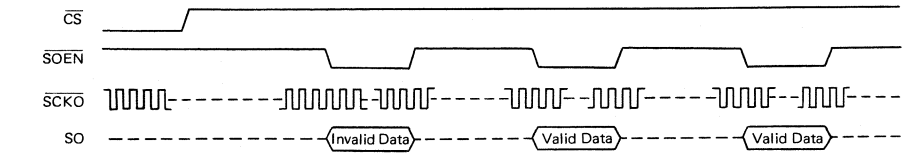
The data converted and output immediately after the initialization is invalid. Valid data is available from the second output. This is because the MPX address is fixed at CH_7 for the converted data output after the initialization. The A/D conversion and the converted data output are repeatedly operated while the $\overline{CS}$ signal is in the high level. (Refer to the Serial Mode 2 Sequence Timing Chart.)



Serial Mode 2 Timing Chart



Serial Mode 2 Sequence Timing Chart

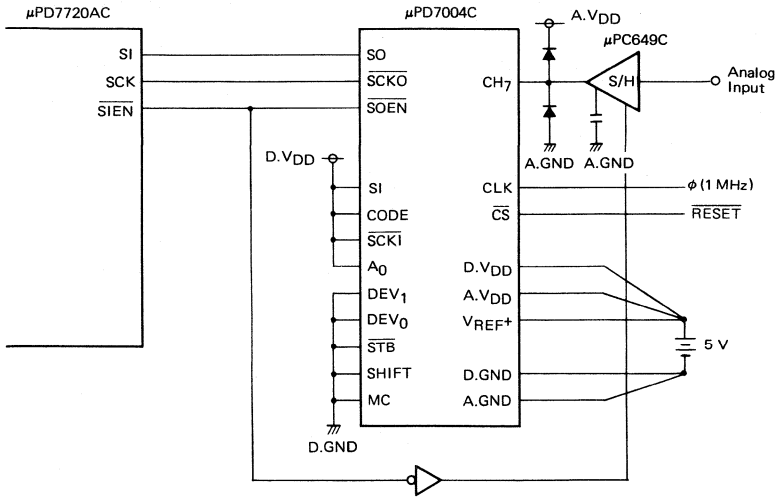


INTERFACE IN SERIAL MODE 2

In serial mode 2 direct connection can be made to the digital signal processor (μPD7720AC) and A/D conversion, unlike the parallel mode and serial mode 1, is operated in a periodic cycle.

Signals in the interface, unlike with serial mode 1, are controlled by the μPD7004C. Fig. 4 shows an example of connecting the μPD7004C to the μPD7720AC.

Fig. 4 μPD7004C/μPD7720AC connection



As shown in Fig. 4, it is possible to interface with only three kinds of signal connection lines in serial mode 2. A/D conversion is operated every 104 μs cycle (where clock = 1 MHz). The converted data is output synchronously with the $\overline{SOEN}$ signal.

The μPD7720AC's serial interface operates 16-bit data transfer, while the converted data consists of 10 bits. Therefore, 6 bits of high data automatically follow the 10 bits of converted data.

In the example above, the external sample & hold circuit (μPC649C) is used and the whole operation is operated as a kind of pipe-line processing. The $\overline{SOEN}$ signal supplies valid data three cycles after the reset cancellation, and then supplies converted data every 104 μs after this.

3 CHANNEL D/A CONVERTER FOR VIDEO PROCESSING

DESCRIPTION

μPC662 is a video 8-bit 3-channel digital analog converter having the following features: High speed and high precision bipolar processing technology for excellent performance of 35 MHz, ±0.5 LSB (MAX.); three channels of identical digital analog converters; power consumption minimized to 200 mW (TYP.); because the three channels are laid out on the same chip, little deviation among the converters, ideal for processing RGB, R-Y, B-Y, and Y signals, where strict deviation control is essential; and reference voltage generating circuit for simplified circuit configuration.

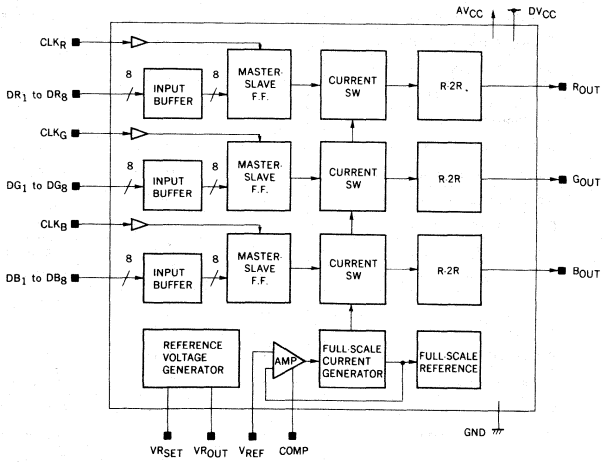
FEATURES

- 8-bit digital analog converter
- Clock rate: 35 Msps
- Conversion precision: ±0.5 LSB (MAX.)
- 5 V single power supply
- 3 channels incorporated
- Reference voltage generating circuit incorporated
- Power consumption: 200 mW (TYP.)

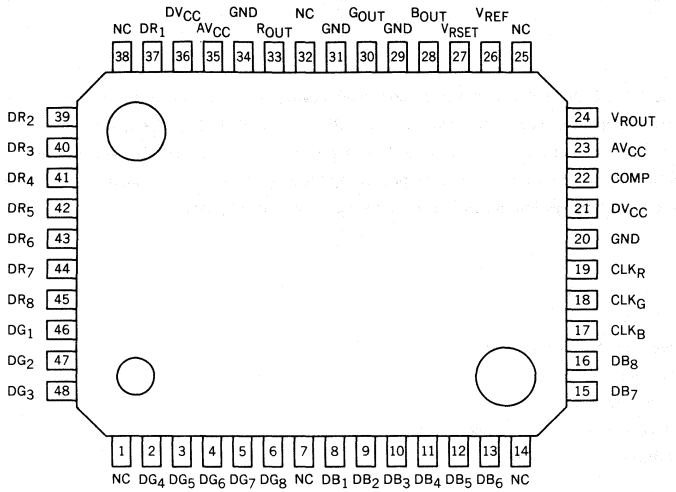
ORDERING INFORMATION

Part Number	Package
μPC662GH	48 Pin Plastic QFP

BLOCK DIAGRAM



PIN CONNECTION (Top View)



PIN NO.	SYMBOL	PIN NAME
1	NC	No Connection
2	DG_4	G channel digital input (4th)
3	DG_5	G channel digital input (5th)
4	DG_6	G channel digital input (6th)
5	DG_7	G channel digital input (7th)
6	DG_8	G channel digital input (LSB)
7	NC	No Connection
8	DB_1	B channel digital input (MSB)
9	DB_2	B channel digital input (2nd)
10	DB_3	B channel digital input (3rd)
11	DB_4	B channel digital input (4th)
12	DB_5	B channel digital input (5th)
13	DB_6	B channel digital input (6th)
14	NC	No Connection
15	DB_7	B channel digital input (7th)
16	DB_8	B channel digital input (LSB)
17	CLK_B	B channel clock input
18	CLK_G	G channel clock input
19	CLK_R	R channel clock input
20	GND	Ground
21	DV_{CC}	Digital power supply
22	COMP	Phase compensating pin
23	AV_{CC}	Analog power supply
24	V_{ROUT}	Reference voltage output

PIN NO.	SYMBOL	PIN NAME
25	NC	No Connection
26	V_{REF}	Reference voltage input
27	V_{RSET}	Reference voltage adjustment
28	B_{OUT}	B output
29	GND	Ground
30	G_{OUT}	G output
31	GND	Ground
32	NC	No Connection
33	R_{OUT}	R output
34	GND	Ground
35	AV_{CC}	Analog power supply
36	DV_{CC}	Digital power supply
37	DR_1	R channel digital input (MSB)
38	NC	No Connection
39	DR_2	R channel digital input (2nd)
40	DR_3	R channel digital input (3rd)
41	DR_4	R channel digital input (4th)
42	DR_5	R channel digital input (5th)
43	DR_6	R channel digital input (6th)
44	DR_7	R channel digital input (7th)
45	DR_8	R channel digital input (LSB)
46	DG_1	G channel digital input (MSB)
47	DG_2	G channel digital input (2nd)
48	DG_3	G channel digital input (3rd)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power Voltage	AV_{CC}, DV_{CC}	−0.3 to +6.0	V
Pin Input Voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Operation Temperature Range	T_{opt}	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C
Package Allowable Loss	P_d	333 (T_a = 75 °C)	mW

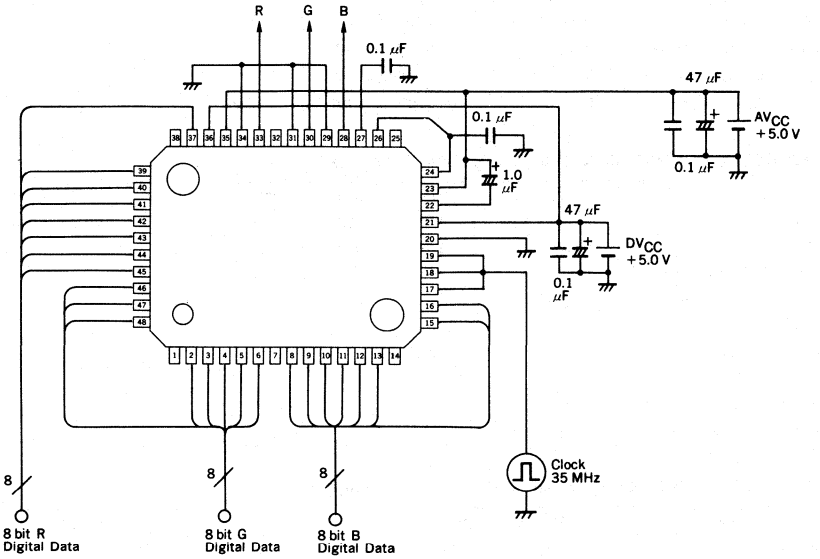
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power voltage	AV_{CC}, DV_{CC}	4.75	5.0	5.25	V	AGND = DGND = 0
Analog reference voltage	V_{REF}	3.70	4.00	4.30	V	
Digital input high level voltage	V_{INDH}	2.0	–	–	V	
Digital input low level voltage	V_{INDL}	–	–	0.8	V	
Sampling frequency	f_{samp}	–	–	35	MHz	
Data input set up time	t_s	12.0	–	–	ns	
Data input hold time	t_h	4.0	–	–	ns	
Sampling clock high pulse width	t_{PWH}	10		1000	ns	
Sampling clock low pulse width	t_{PWL}	10		1000	ns	

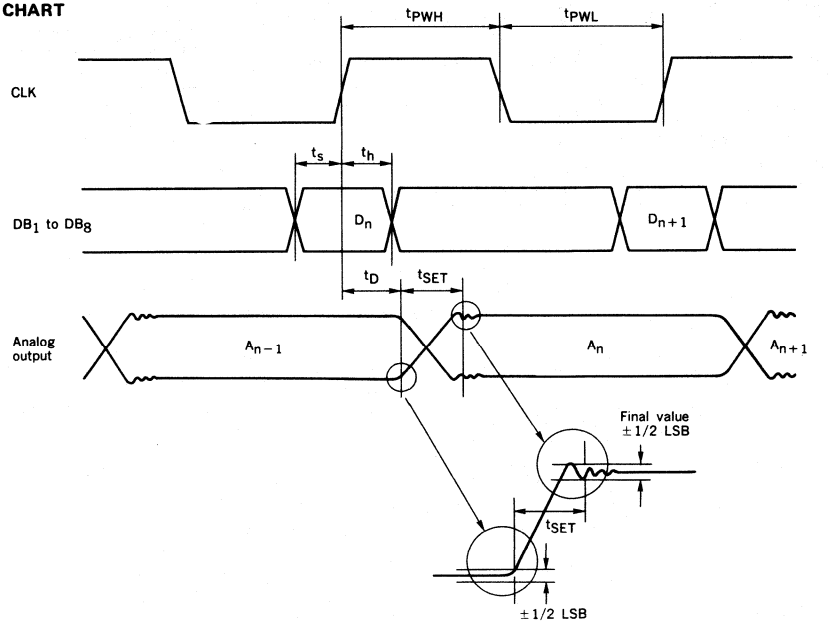
ELECTRIC CHARACTERISTICS (T_a = −20 to +75 °C, AV_{CC} = DV_{CC} = 5±0.25 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power consumption	I_{CC}	25	40	60	mA	T_a = 25 °C
Integral linearity error	ILE			±0.5	LSB	T_a = 0 to +75 °C
Differential linearity error	DLE			±0.5	LSB	T_a = 0 to +75 °C
Output voltage full scale precision	V_{OFS}	0.85	1.0	1.15	V	AV_{CC} = DV_{CC} = 5.0 V, V_{REF} = 4.0 V This precision is the difference between the full-scale output voltage and zero-scale output voltage.
RGB output voltage ratio	FSR	−0.8	0	+8.0	%	
Reference power supply output voltage	V_{ROUT}	3.8	4.0	4.2	V	AV_{CC} = DV_{CC} = 5.0 V
Output delay time	t_D		15		ns	
Settling time	t_{SET}		25		ns	C_L = 5 pF

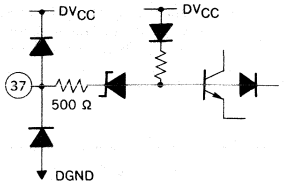
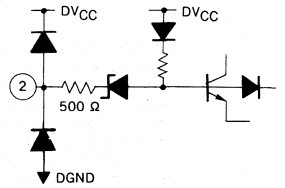
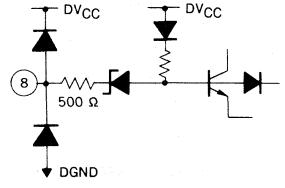
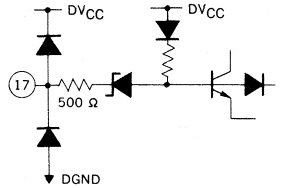
MEASUREMENT CIRCUIT

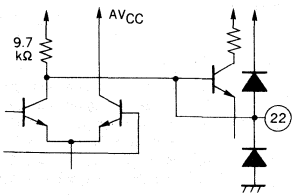
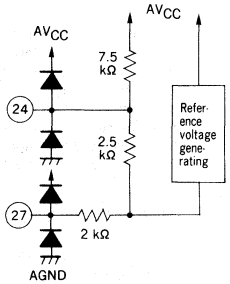
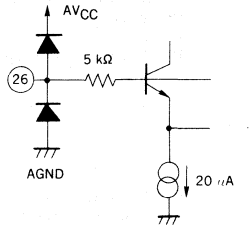
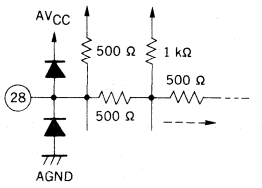


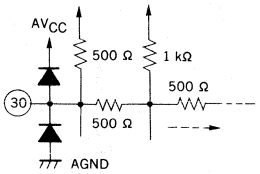
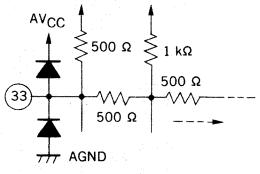
TIMING CHART



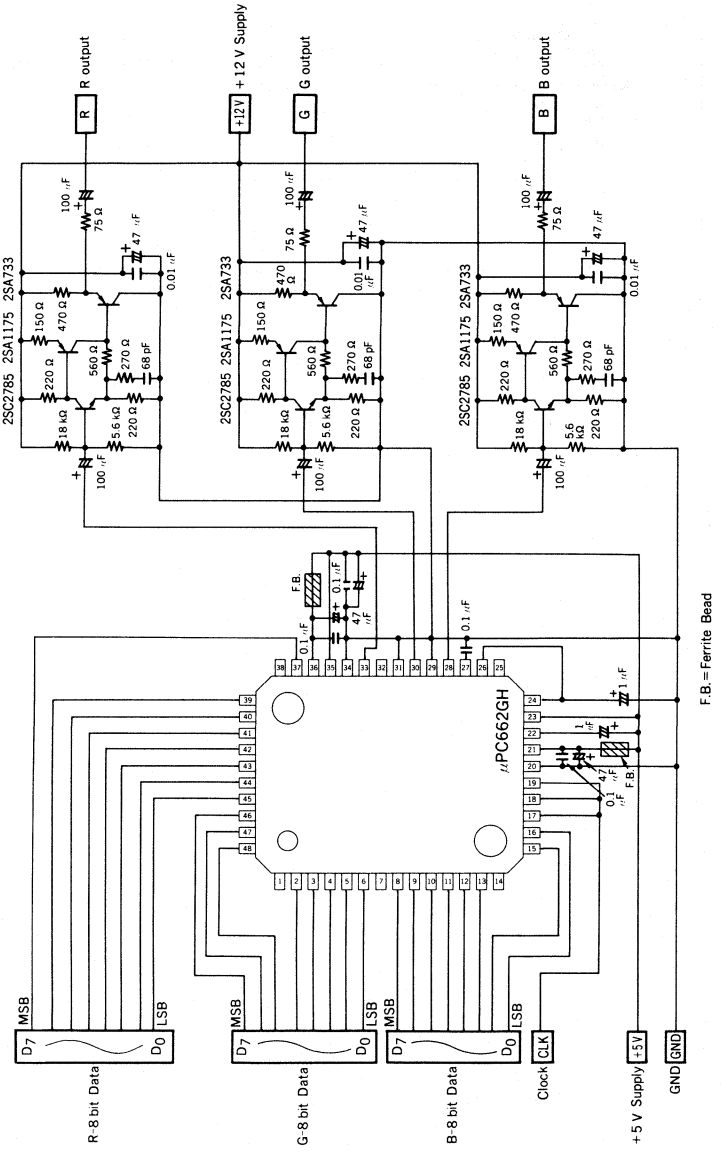
DESCRIPTION OF PINS

PIN NO.	EQUIVALENT CIRCUIT	FUNCTIONS
37, 39, 40, 41, 42, 43, 44, 45		37: R channel digital input (MSB) 39: R channel digital input (2nd) 40: R channel digital input (3rd) 41: R channel digital input (4th) 42: R channel digital input (5th) 43: R channel digital input (6th) 44: R channel digital input (7th) 45: R channel digital input (LSB)
2, 3, 4, 5, 6, 46, 47, 48		46: G channel digital input (MSB) 47: G channel digital input (2nd) 48: G channel digital input (3rd) 2: G channel digital input (4th) 3: G channel digital input (5th) 4: G channel digital input (6th) 5: G channel digital input (7th) 6: G channel digital input (LSB)
8, 9, 10, 11, 12, 13, 15, 16		8: B channel digital input (MSB) 9: B channel digital input (2nd) 10: B channel digital input (3rd) 11: B channel digital input (4th) 12: B channel digital input (5th) 13: B channel digital input (6th) 15: B channel digital input (7th) 16: B channel digital input (LSB)
17, 18, 19		17: B channel clock input 18: G channel clock input 19: R channel clock input
21, 36		Digital power pin

PIN NO.	EQUIVALENT CIRCUIT	FUNCTIONS
22		Phase compensating capacitor connection pin for full-scale amplifier. The capacitor must be connected between this pin and analog power supply.
23, 35		Analog power pin
24 27		24: Voltage output pin of the incorporated reference voltage generating circuit. This pin has high output impedance, and must be connected with a high impedance element. 27: Voltage adjusting pin for the incorporated reference voltage generating circuit. The output voltage from pin 26 is varied depending on the voltage applied to pin 28. When no particular adjustment is necessary, connect approx. 0.1 μF capacitance between pin 28 and the analog ground.
26		Reference voltage input pin. The output full-scale range is set according to the voltage applied to this pin. Apply standard 4.0 V. When no adjustment is necessary, connect the output from pin 24 directly to this pin.
28		B signal output pin. The output resistance is approximately 333 Ω (TYP.).
20, 29, 31, 34		Grounding pin

PIN NO.	EQUIVALENT CIRCUIT	FUNCTIONS
30		G signal output pin. The output resistance is approx. 333 Ω (TYP.).
33		R signal output pin. The output resistance is approx. 333 Ω (TYP.).

APPLICATION



2 CHANNEL D/A CONVERTER FOR VIDEO PROCESSING

DESCRIPTION

μPC664 is a video 8-bit 2-channel digital analog converter having the following features: High speed and high precision bipolar processing technology for excellent performance of 35 MHz, ±0.5 LSB (MAX.); two channels of identical digital analog converters; power consumption minimized to 135 mW (TYP.); because the two channels are laid out on the same chip, little deviation among the converters, ideal for processing Y and C signals, where strict deviation control is essential; and reference voltage generating circuit for simplified circuit configuration.

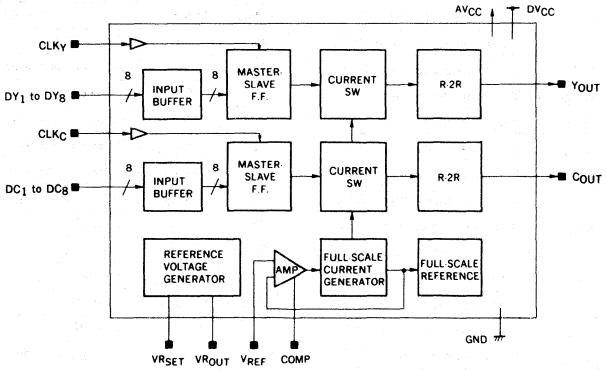
FEATURES

- 8-bit digital analog converter
- Clock rate: 35 Msps
- Conversion precision: ±0.5 LSB (MAX.)
- 5 V single power supply
- 2 channels incorporated
- Reference voltage generating circuit incorporated
- Power consumption: 135 mW (TYP.)

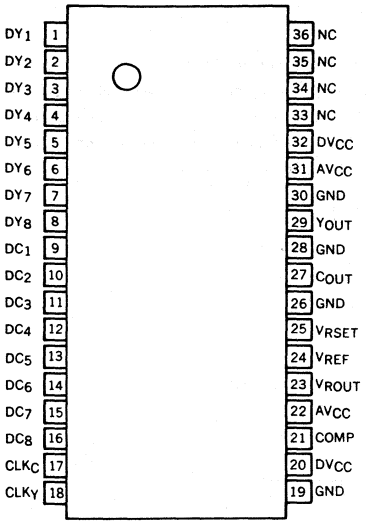
ORDERING INFORMATION

Part Number	Package
μPC664GS	36 Pin Plastic SOP (300 mil)

BLOCK DIAGRAM



PIN CONNECTION (Top View)



PIN NO.	SYMBOL	PIN NAME	PIN NO.	SYMBOL	PIN NAME
1	DY_1	Y channel digital input (MSB)	19	GND	Ground
2	DY_2	Y channel digital input (2nd)	20	DV_{CC}	Digital power supply
3	DY_3	Y channel digital input (3rd)	21	COMP	Phase compensating pin
4	DY_4	Y channel digital input (4th)	22	AV_{CC}	Analog power supply
5	DY_5	Y channel digital input (5th)	23	V_{ROUT}	Reference voltage output
6	DY_6	Y channel digital input (6th)	24	V_{REF}	Reference voltage input
7	DY_7	Y channel digital input (7th)	25	V_{RSET}	Reference voltage adjustment
8	DY_8	Y channel digital input (LSB)	26	GND	Ground
9	DC_1	C channel digital input (MSB)	27	C_{OUT}	C output
10	DC_2	C channel digital input (2nd)	28	GND	Ground
11	DC_3	C channel digital input (3rd)	29	X_{OUT}	Y output
12	DC_4	C channel digital input (4th)	30	GND	Ground
13	DC_5	C channel digital input (5th)	31	AV_{CC}	Analog power supply
14	DC_6	C channel digital input (6th)	32	DV_{CC}	Digital power supply
15	DC_7	C channel digital input (7th)	33	NC	No Connection
16	DC_8	C channel digital input (LSB)	34	NC	No Connection
17	CLK_C	C channel clock input	35	NC	No Connection
18	CLK_Y	Y channel clock input	36	NC	No Connection

2

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power Voltage	AV_{CC}, DV_{CC}	−0.3 to +6.0	V
Pin Input Voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Operation Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C
Package Allowable Loss	P_d	560 (T_a = 25 °C)	mW

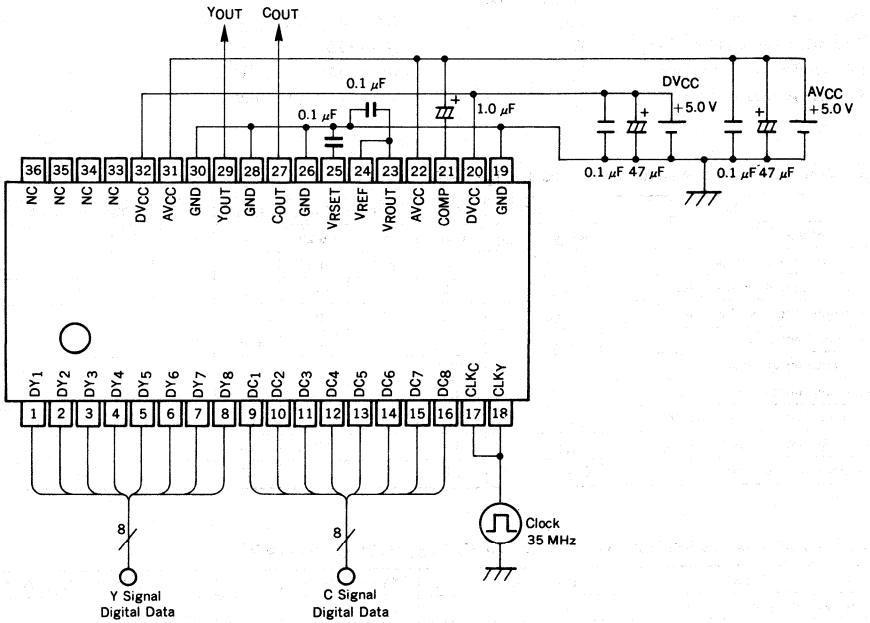
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power voltage	AV_{CC}, DV_{CC}	4.75	5.0	5.25	V	AGND = DGND = 0
Analog reference voltage	V_{REF}	3.70	4.00	4.30	V	
Digital input high level voltage	V_{INDH}	2.0	–	–	V	
Digital input low level voltage	V_{INDL}	–	–	0.8	V	
Sampling frequency	f_{samp}	–	–	35	MHz	
Data input set up time	t_s	12.0	–	–	ns	
Data input hold time	t_h	4.0	–	–	ns	
Sampling clock high pulse width	t_{PWH}	10		1000	ns	
Sampling clock low pulse width	t_{PWL}	10		1000	ns	
Compensation capacity	C_{comp}	1.0	–	–	μF	

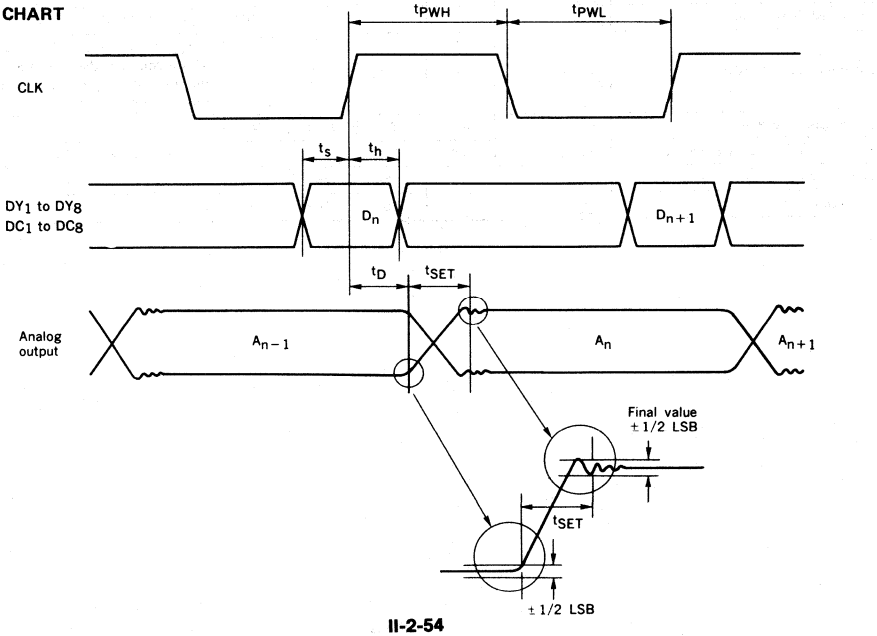
ELECTRIC CHARACTERISTICS (T_a = −20 to +75 °C, AV_{CC} = DV_{CC} = 5±0.25 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power consumption	I_{CC}		27	40	mA	T_a = 25 °C
Integral linearity error	ILE			±0.5	LSB	T_a = 0 to +75 °C
Differential linearity error	DLE			±0.5	LSB	T_a = 0 to +75 °C
Output voltage full-scale precision	V_{OFS}	0.85	1.0	1.15	V	AV_{CC} = DV_{CC} = 5.0 V, V_{REF} = 4.0 V This precision is the difference between the full-scale output voltage and zero-scale output voltage.
RGB output voltage ratio	FSR	−0.8	0	+8.0	%	
Reference power supply output voltage	V_{ROUT}	3.8	4.0	4.2	V	AV_{CC} = DV_{CC} = 5.0 V
Output delay time	t_D		15	25	ns	
Setting time	t_{SET}		25	40	ns	C_L = 5 pF

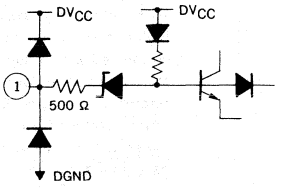
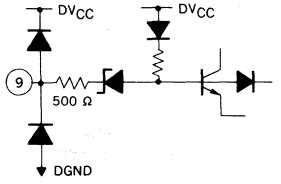
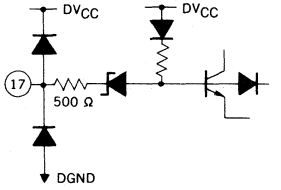
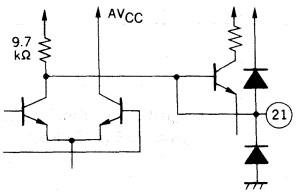
MEASUREMENT CIRCUIT

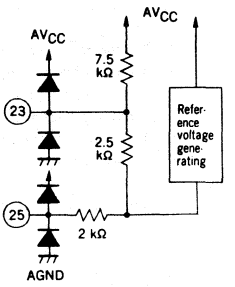
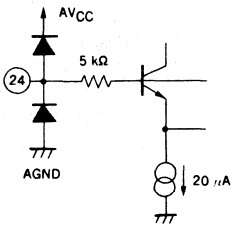
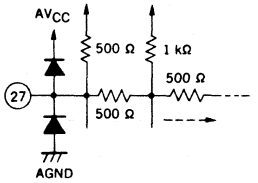
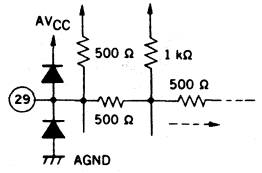


TIMING CHART

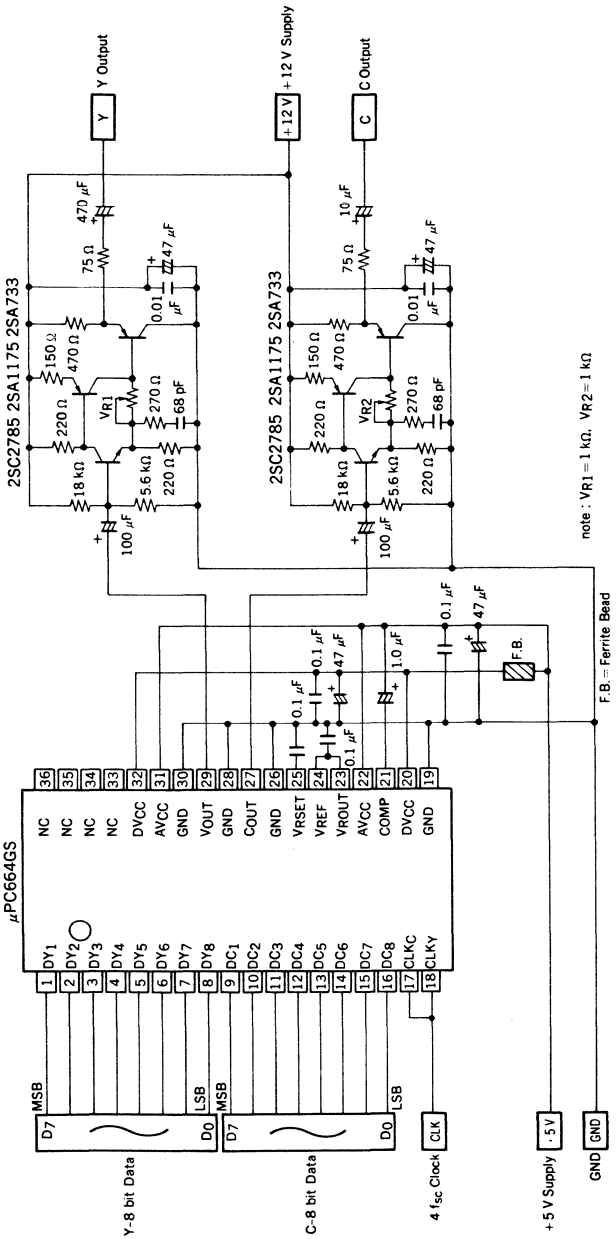


DESCRIPTION OF PINS

PIN NO.	EQUIVALENT CIRCUIT	FUNCTIONS
1, 2, 3, 4, 5, 6, 7, 8		1: Y channel digital input (MSB) 2: Y channel digital input (2nd) 3: Y channel digital input (3rd) 4: Y channel digital input (4th) 5: Y channel digital input (5th) 6: Y channel digital input (6th) 7: Y channel digital input (7th) 8: Y channel digital input (LSB)
9, 10, 11, 12, 13, 14, 15, 16		9: C channel digital input (MSB) 10: C channel digital input (2nd) 11: C channel digital input (3rd) 12: C channel digital input (4th) 13: C channel digital input (5th) 14: C channel digital input (6th) 15: C channel digital input (7th) 16: C channel digital input (LSB)
17, 18		17: C channel clock input 18: Y channel clock input
20, 32		Digital power pin
21		Phase compensating capacitor connection pin for full-scale amplifier. The capacitor must be connected between this pin and analog power supply.
22, 31		Analog power pin

PIN NO.	EQUIVALENT CIRCUIT	FUNCTIONS
23 25		23: Voltage output pin of the incorporated reference voltage generating circuit. This pin has high output impedance, and must be connected with a high impedance element. 25: Voltage adjusting pin for the incorporated reference voltage generating circuit. The output voltage from pin 23 is varied depending on the voltage applied to pin 25. When no particular adjustment is necessary, connect approx. 0.1 μF capacitance between pin 25 and the analog ground.
24		Reference voltage input pin. The output full-scale range is set according to the voltage applied to this pin. Apply standard 4.0 V. When no adjustment is necessary, connect the output from pin 23 directly to this pin.
27		C signal output pin. The output resistance is approximately 333 Ω (TYP.).
29		Y signal output pin. The output resistance is approx. 333 Ω (TYP.).
19, 26, 28, 30		Grounding pin
33, 34, 35, 36		No-Connection pin

APPLICATION



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

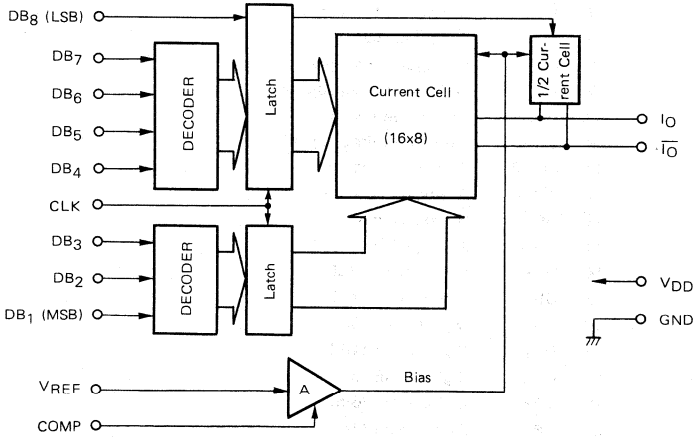
8 bit D/A Converter for Video Signal Processing CMOS LSI

The μPD6900C is an 8 bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 20 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems.

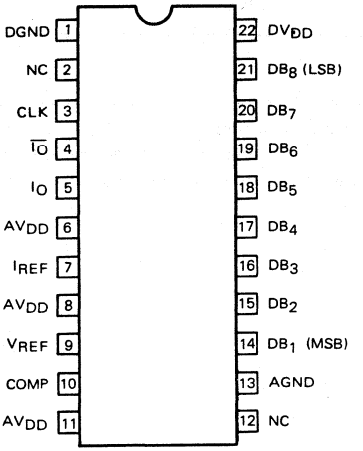
FEATURES

- Resolution : 8 bits
- Conversion rate : 20 Msps
- Linearity : ±1/2 LSB TYP.
- Reference voltage : 2.0 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (150 mW TYP.)
- TTL compatible (Digital inputs)
- 22 pin plastic DIP

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



1	DGND	Digital GND
2	NC	No connection
3	CLK	Sampling clock input
4	$\overline{I_O}$	Complementary current output
5	I_O	Current output
6	AV_{DD}	Analog power supply
7	I_{REF}	Full-scale current adjustment
8	AV_{DD}	Analog power supply
9	V_{REF}	Reference voltage input
10	COMP	Amp compensation
11	AV_{DD}	Analog power supply
12	NC	No connection
13	AGND	Analog GND
14	DB_1	Digital input (MSB)
15	DB_2	Digital input (2nd)
16	DB_3	Digital input (3rd)
17	DB_4	Digital input (4th)
18	DB_5	Digital input (5th)
19	DB_6	Digital input (6th)
20	DB_7	Digital input (7th)
21	DB_8	Digital input (LSB)
22	DV_{DD}	Digital power supply

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to V_{DD}+0.3	V
Output terminal voltage	−0.3 to V_{DD}+0.3	V
Operating temperature range	−20 to +75	°C
Storage temperature range	−40 to +125	°C

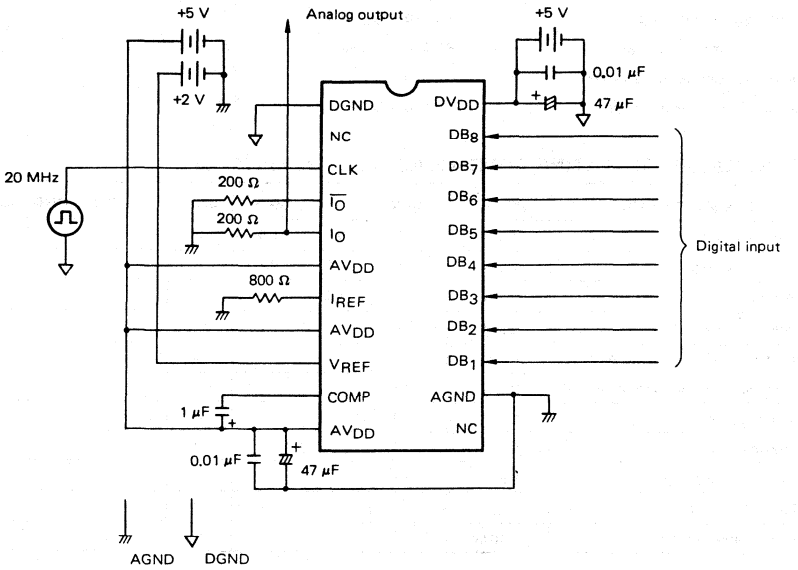
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	V_{DD}	4.5	5.0	5.5	V	
Reference voltage	V_{REF}	1.8	2.0	2.2	V	
Reference resistance	R_{REF}		800		Ω	
Sampling clock	f_{samp}	DC		20	MHz	
Sampling clock low level pulse width	t_{PWL}	10			ns	
Sampling clock high level pulse width	t_{PWH}	10			ns	
Data set up time	t_S	20			ns	
Data hold time	t_H	10			ns	
Digital input high level	V_{IH}	2.7			V	
Digital input low level	V_{IL}			0.4	V	
Compensation capacity	C_{COMP}	1.0			μF	

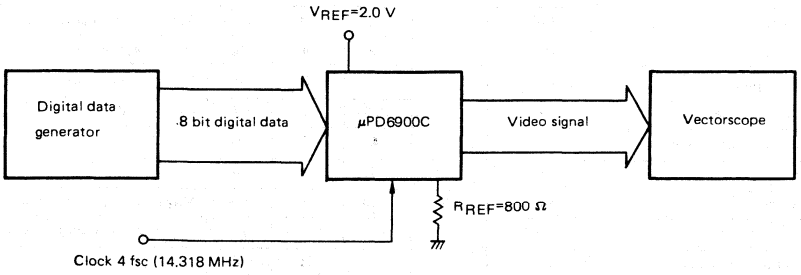
ELECTRICAL CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V ± 0.5 V, f_{samp} = 20 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply current	I_{DD}		30	50	mA	V_{DD}=5.0 V
Resolution	RES		8		bit	
Non-linearity error	NL		±1/2	±1	LSB	T_a=0~60 °C, V_{REF}=2.0 V
Differential non-linearity	DNL		±1/2	±1	LSB	T_a=0~60 °C, V_{REF}=2.0 V
Differential gain	DG		3	4	%	f_{samp}=14.318 MHz
Differential phase	DP		1	3	deg	f_{samp}=14.318 MHz
Output compliance	V_O	2.5	3.0		V	V_{DD}=5.0 V
Analog output delay time	t_D		40		ns	
Settling time	t_{SET}		40		ns	
Full-scale current	I_{FS}	9	10	11	mA	V_{REF}=2.0 V, R_{REF}=800 Ω
Zero-scale offset current	I_{ZS}			20	μA	V_{REF}=2.0 V, R_{REF}=800 Ω
Digital input capacitance	C_{DI}			30	pF	
Digital input current	I_I			10	μA	

TEST CIRCUIT

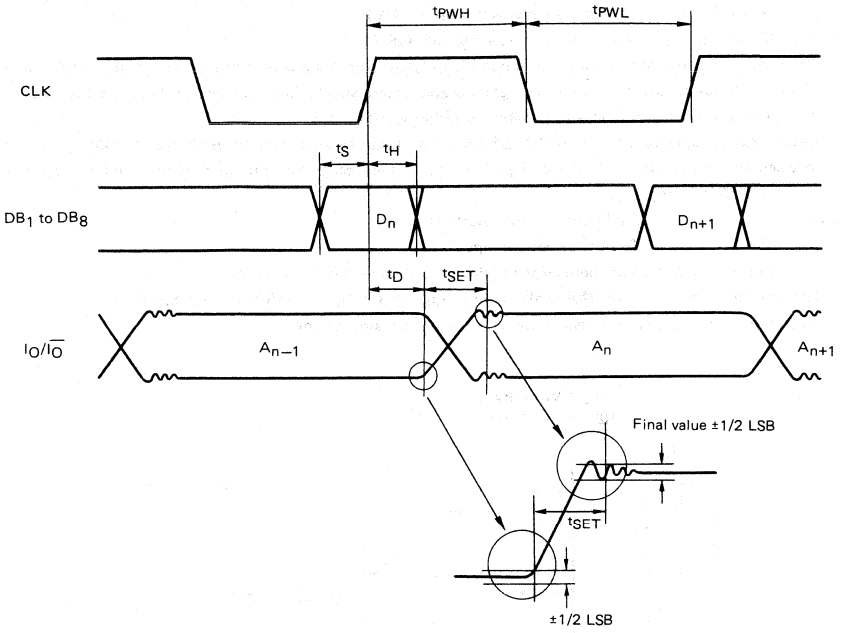


DG AND DP MEASUREMENT BLOCK DIAGRAM



The data from the digital data generator is 40 IRE lamp signal (NTSC) digital data.

TIMING CHART



PIN DESCRIPTIONS

DGND (Pin 1) Digital system ground

AGND (Pin 13) Analog system ground

DV_{DD} (Pin 22) Digital system power supply (+5 V)

AV_{DD} (Pins 6, 8, 11) Analog system power supply (+5 V)

The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

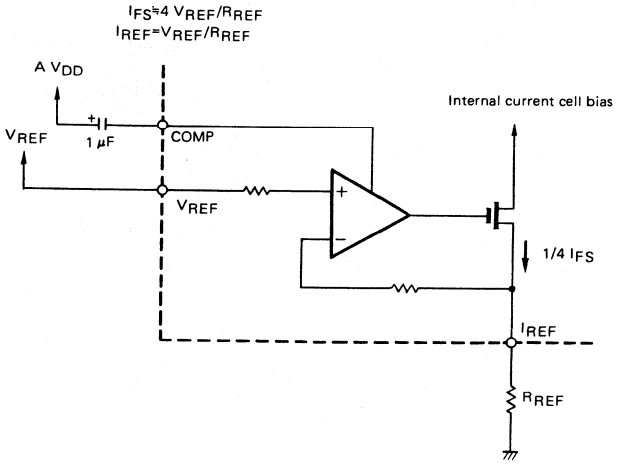
Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6900C pins.

I_{REF} (Pin 7) Full-scale current adjustment pin

V_{REF} (Pin 9) Reference voltage input pin

These pins are used in adjustment of the analog output current (full-scale current).

The analog output current (full-scale current I_{FS}) is set by the reference voltage V_{REF} and the reference resistance R_{REF} connected between the I_{REF} pin and analog ground.



The recommended reference voltage and reference resistance values are V_{REF} = 2.0 V and R_{REF} = 800 Ω respectively. The output analog current I_{FS} in this case will be 10 mA. Also connect by-pass capacitors of about 0.01 μF and 47 μF between the V_{REF} pin and GND in the same way as the by-pass capacitors connected to the power pins.

COMP (Pin 10) Phase compensation capacitor connection

A capacitor for phase compensation of the internal amplifier is connected to this pin. Connect a 1.0 μF capacitor between this pin and analog V_{DD}.

DB_1 to DB_8 (Pins 14 thru 21) Digital data input pins

DB_1 to DB_8 are the 8 bit digital data input pins. The code format is binary, and the input voltage level is TTL compatible.

Digital input code								Analog output current
DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)	
0	0	0	0	0	0	0	0	0 note
0	0	0	0	0	0	0	1	1/256 I_{FS}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	253/256 I_{FS}
1	1	1	1	1	1	1	0	254/256 I_{FS}
1	1	1	1	1	1	1	1	255/256 I_{FS}

note : Excluding offset current

Digital data (DB_1 to DB_8) is latched by the rising edge of the sampling clock, and converted to corresponding analog outputs.

CLK (Pin 3) Sampling clock input pin

Digital data is latched by the rising edge of the clock signal applied to the sampling clock input pin, and is subsequently converted to analog outputs. The maximum clock frequency is 20 MHz.

I_O (Pin 5) Analog signal output pin

$\overline{I/O}$ (Pin 4) Analog signal complementary output pin

These two pins are current output pins. The full-scale output current is determined by the reference resistance R_{REF} and reference voltage V_{REF}.

$$I_{FS} = I_O + \overline{I_O} = 4\ V_{REF}/R_{REF}$$

$\overline{I_O}$ is the complementary output pin of I_O. The added output current from the I_O and $\overline{I_O}$ pins becomes the full-scale current in accordance with the above equation. Analog output current can be easily converted to an analog output voltage by connecting a resistance between the I_O or $\overline{I_O}$ pin and analog ground. In this case resistances must also be connected to the I_O and $\overline{I_O}$ pins.

NC (Pins 2 and 12) No connection

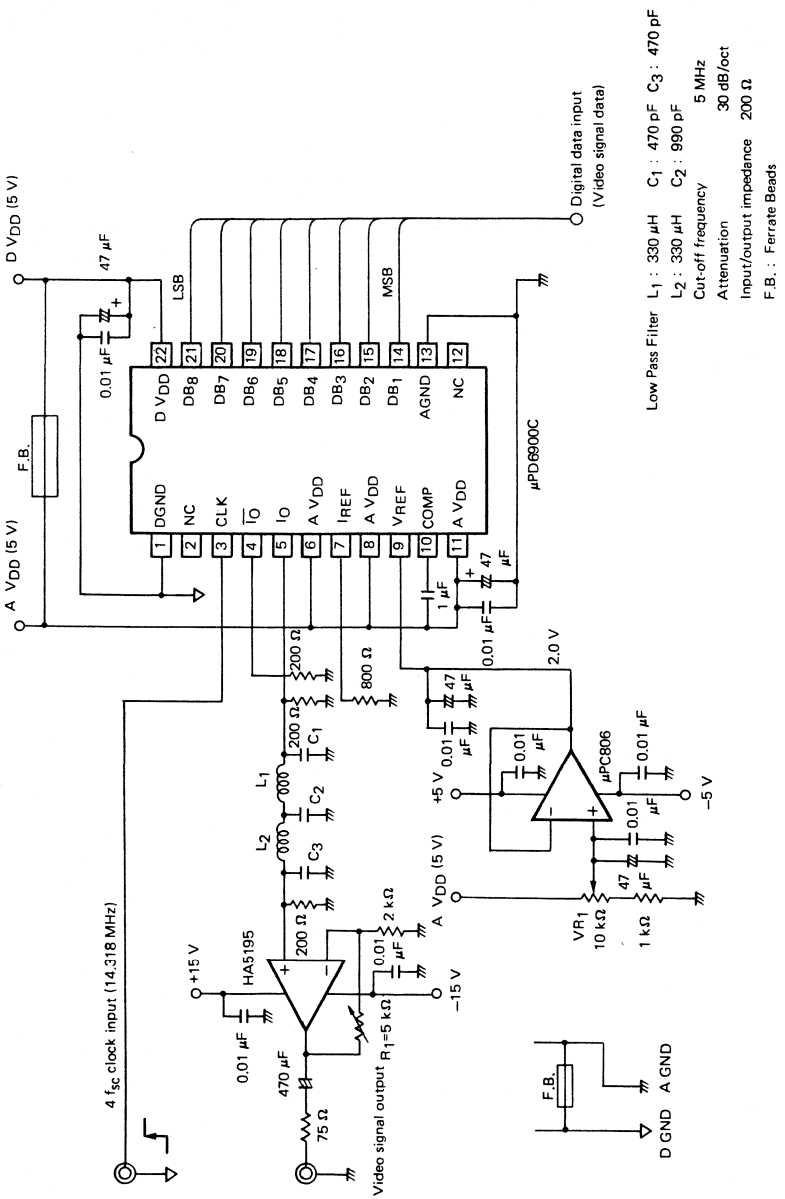
These pins may be connected to analog ground.

Example of an Application Circuit

This example shows D/A conversion of video signal (NTSC) digital data at a conversion rate of four times the subcarrier frequency ($4\ f_{sc}$) to obtain the video output signal.

The analog output signal is passed via a low-pass filter (LPF) to a video amplifier (HA5195) to be amplified prior to output.

APPLICATION CIRCUIT



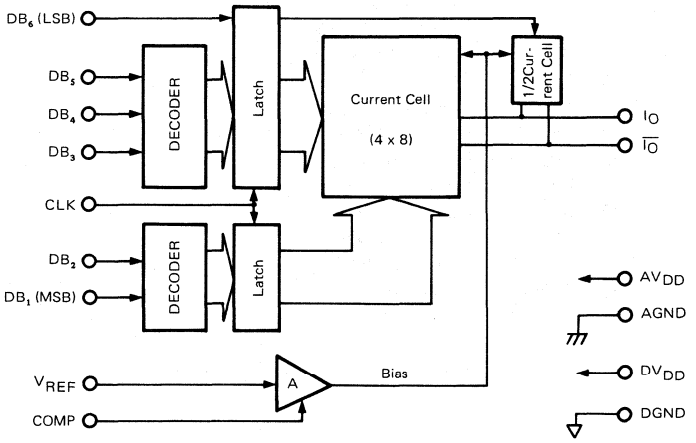
6 BIT D/A CONVERTER FOR VIDEO SIGNAL PROCESSING CMOS LSI

The μPD6901C is an 6 bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 20 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems.

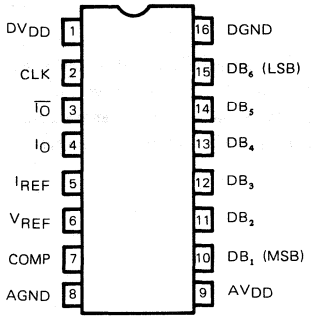
FEATURES

- Resolution : 6 bits
- Conversion rate : 20 Mpsps
- Linearity : ±1/2 LSB MAX.
- Reference voltage : 2.0 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (110 mW TYP.)
- TTL compatible (Digital inputs)
- 16 pin plastic DIP

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



1	DV_{DD}	Digital power supply
2	CLK	Sampling clock input
3	$\overline{I_O}$	Complementary current output
4	I_O	Current output
5	I_{REF}	Full-scale current adjustment
6	V_{REF}	Reference voltage input
7	COMP	Amp compensation
8	AGND	Analog GND
9	AV_{DD}	Analog power supply
10	DB_1	Digital input (MSB)
11	DB_2	Digital input (2nd)
12	DB_3	Digital input (3rd)
13	DB_4	Digital input (4th)
14	DB_5	Digital input (5th)
15	DB_6	Digital input (LSB)
16	DGND	Digital GND

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Power supply voltage	-0.3 to +7.0	V
Input terminal voltage	-0.3 to V_{DD} +0.3	V
Output terminal voltage	-0.3 to V_{DD} +0.3	V
Analog power supply voltage	DV_{DD}-0.3 to DV_{DD} +0.3	V
Analog GND voltage	DGND-0.3 to DGND+0.3	V
Operating temperature range	-20 to +75	°C
Storage temperature range	-40 to +125	°C

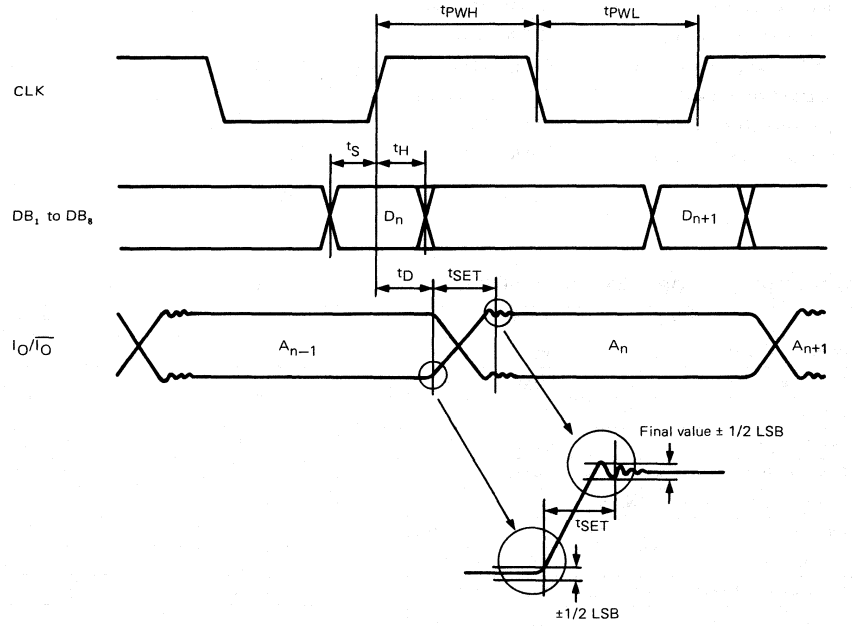
RECOMMENDED OPERATING CONDITIONS (T_a = -20 to +75°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	V_{DD}	4.5	5.0	5.5	V	
Reference voltage	V_{REF}	1.8	2.0	2.2	V	
Reference resistance	R_{REF}		390		Ω	
Sampling clock	f_{samp}	DC		20	MHz	
Sampling clock low level pulse width	t_{PWL}	15			ns	
Sampling clock high level pulse width	t_{PWH}	15			ns	
Data set up time	t_S	20			ns	
Data hold time	t_H	10			ns	
Digital input high level	V_{IH}	2.7			V	
Digital input low level	V_{IL}			0.6	V	
Compensation capacity	C_{COMP}	0.01	1.0		μF	

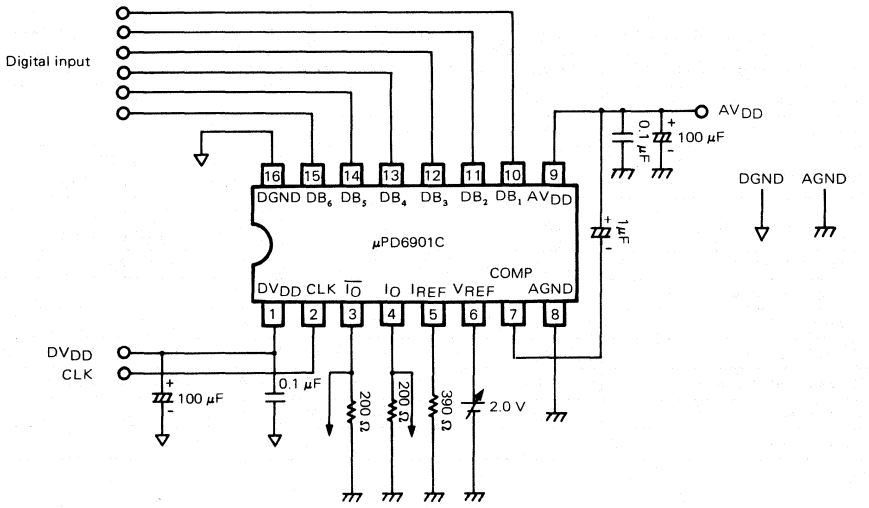
ELECTRICAL CHARACTERISTICS (T_a = -20 to +75°C, V_{DD} = 5 V ± 0.5 V, f_{samp} = 20 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power supply current	I_{DD}		22	50	mA	V_{DD} = 5.0 V
Resolution	RES		6		bit	
Non-linearity error	NL		±0.11	±0.5	LSB	T_a = 0 to 60°C, V_{DD} = 5 V ± 0.25 V
Differential non-linearity	DNL		±0.04	±0.5	LSB	T_a = 0 to 60°C, V_{DD} = 5 V ± 0.25 V
Output compliance	V_O	2.5	3.0		V	V_{DD} = 5.0 V
Analog output delay time	t_D		40		ns	
Settling time	t_{SET}		40		ns	
Full-scale current	I_{FS}	9	10	11	mA	V_{REF}=2.0 V, R_{REF}=390 Ω
Zero-scale offset current	I_{ZS}			20	μA	V_{REF}=2.0 V, R_{REF}=390 Ω
Digital input capacitance	C_{DI}		10	20	pF	
Digital input current	I_I			10	μA	

TIMING CHART



TEST CIRCUIT



PIN DESCRIPTIONS

DGND (Pin 16) Digital system ground
AGND (Pin 8) Analog system ground
DV_{DD} (Pin 1) Digital system power supply (+5 V)
AV_{DD} (Pin 9) Analog system power supply (+5 V)

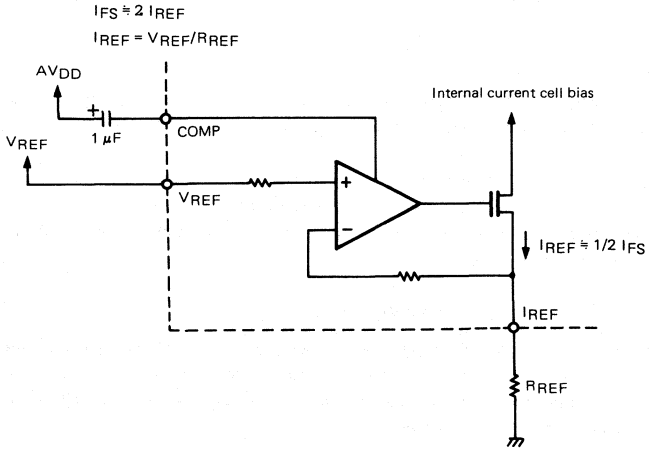
The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible, to the μPD6901C pins. Supply the digital system power from the analog power line through the low path filter to prevent from luch up.

I_{REF} (Pin 5) Full-scale current adjustment pin
V_{REF} (Pin 6) Reference voltage input pin

These pins are used in adjustment of the analog output current (full-scale current).

The analog output current (full-scale current I_{FS}) is set by the reference voltage V_{REF} and the reference resistance R_{REF} connected between the I_{REF} pin and analog ground.



The recommended reference voltage and reference resistance values are V_{REF} = 2.0 V and R_{REF} = 390 Ω respectively. The output analog current I_{FS} in this case will be 10 mA. Also connect by-pass capacitors of about 0.01 μF and 47 μF between the V_{REF} pin and GND in the same way as the by-pass capacitors connected to the power pins.

COMP (Pin 7) Phase compensation capacitor connection

A capacitor for phase compensation of the internal amplifier is connected to this pin. Connect a 1.0 μF capacitor between this pin and analog V_{DD}.

DB_1 to DB_6 (Pins 10 thru 15) Digital data input pins

DB_1 to DB_6 are the 6 bit digital data input pins. The code format is binary, and the input voltage level is TTL compatible.

Digital input code						Analog output current
DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6 (LSB)	
0	0	0	0	0	0	0 note
0	0	0	0	0	1	1/64 I_{FS}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	61/64 I_{FS}
1	1	1	1	1	0	62/64 I_{FS}
1	1	1	1	1	1	63/64 I_{FS}

Note: Excluding offset current

Digital data (DB_1 to DB_6) is latched by the rising edge of the sampling clock, and converted to corresponding analog outputs.

CLK (Pin 2) Sampling clock input pin

Digital data is latched by the rising edge of the clock signal applied to the sampling clock input pin, and is subsequently converted to analog outputs. The maximum clock frequency is 20 MHz.

I_O (Pin 4) Analog signal output pin

$\overline{I_O}$ (Pin 3) Analog signal complementary output pin

These two pins are current output pins. The full-scale output current is determined by the reference resistance R_{REF} and reference voltage V_{REF}.

$$I_{FS} = I_O + \overline{I_O} = 2\ V_{REF}/R_{REF}$$

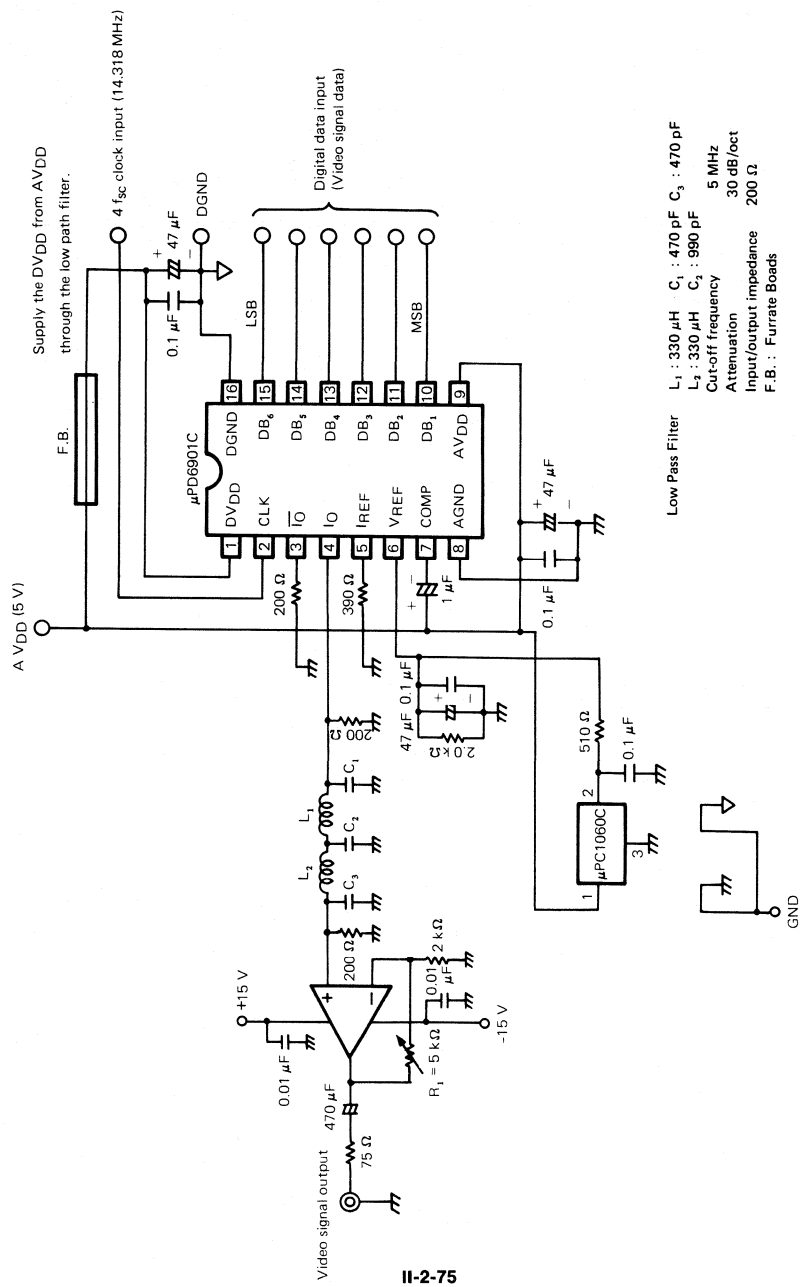
$\overline{I_O}$ is the complementary output pin of I_O. The added output current from the I_O and $\overline{I_O}$ pins becomes the full-scale current in accordance with the above equation. Analog output current can be easily converted to an analog output voltage by connecting a resistance between the I_O or $\overline{I_O}$ pin and analog ground. In this case resistances must also be connected to the I_O and $\overline{I_O}$ pins.

Example of an Application Circuit

This example shows D/A conversion of video signal (NTSC) digital data at a conversion rate of four times the subcarrier frequency (4 f_{SC}) to obtain the video output signal.

The analog output signal is passed via a low-pass filter (LPF) to a video amplifier to be amplified prior to output.

APPLICATION CIRCUIT



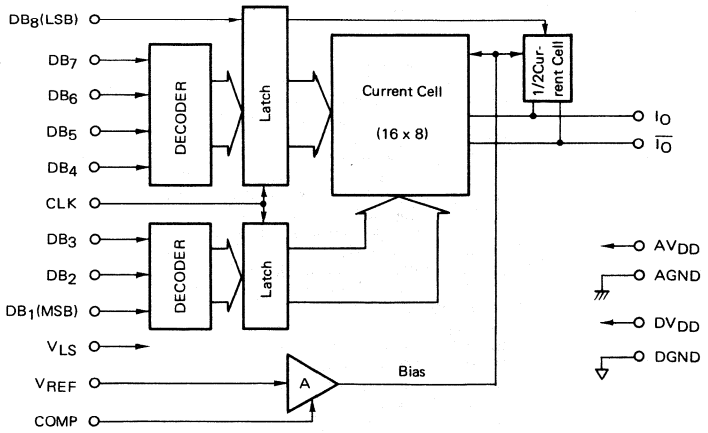
8 bit 50MSPS D/A Converter CMOS

The μPD6902C is an 8 bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 50 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems.

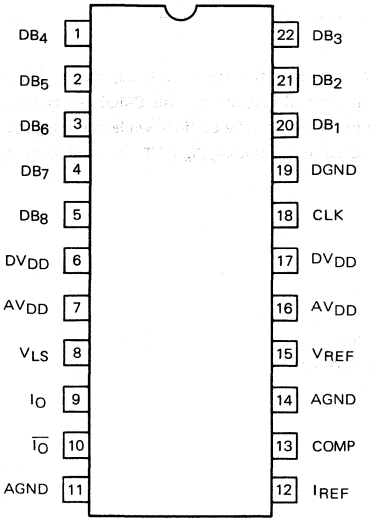
FEATURES

- Resolution: 8 bits
- Conversion rate: 50 Msps
- Liniarity: ±1/2 LSB TYP.
- Reference voltage: 2.5 V TYP.
- Power supply voltage: +5 V single
- Low power comsumption (400 mW TYP.)
- TTL compatible (Digital inputs)
- 22 pin plastic DIP

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



1	DB_4	Digital input (4th)
2	DB_5	Digital input (5th)
3	DB_6	Digital input (6th)
4	DB_7	Digital input (7th)
5	DB_8	Digital input (LSB)
6	DV_{DD}	Digital power supply
7	AV_{DD}	Analog power supply
8	V_{LS}	Digital input level select (TTL/CMOS)
9	I_o	Current output
10	$\overline{I_o}$	Complementary current output
11	AGND	Analog GND
12	I_{REF}	Full-scale current adjustment
13	COMP	Amp compensation
14	AGND	Analog GND
15	V_{REF}	Reference voltage input
16	AV_{DD}	Analog power supply
17	DV_{DD}	Digital power supply
18	CLK	Sampling clock input
19	DGND	Digital GND
20	DB_1	Digital input (MSB)
21	DB_2	Digital input (2nd)
22	DB_3	Digital input (3rd)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to V_{DD} +0.3	V
Output terminal voltage	−0.3 to V_{DD} +0.3	V
Analog power supply voltage	DV_{DD}−0.3 to DV_{DD}+0.3	V
Analog GND voltage	DGND−0.3 to DGND+0.3	V
Operating temperature range	−20 to +75	°C
Storage temperature range	−40 to +125	°C

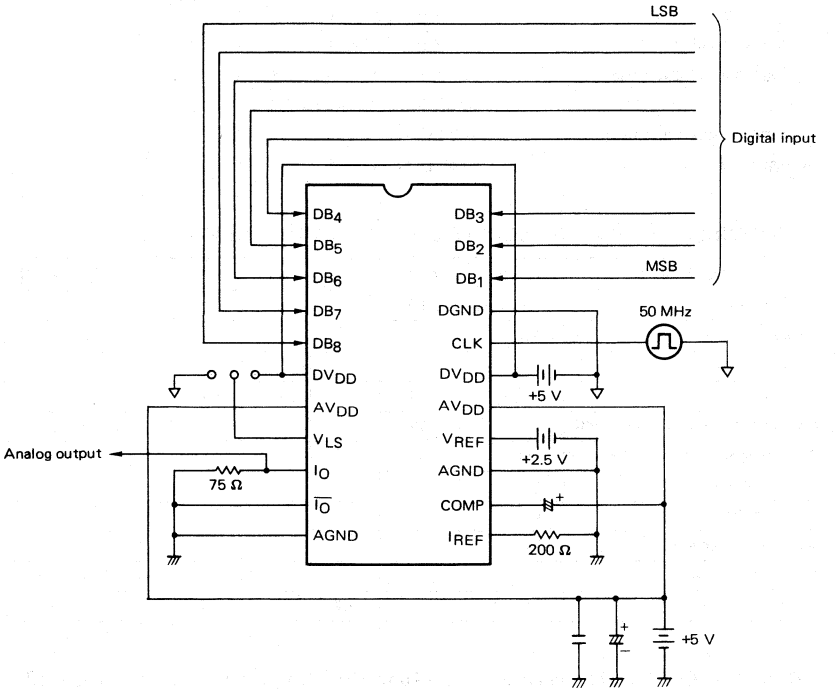
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	AV_{DD},DV_{DD}	4.5	5.0	5.5	V	
Reference voltage	V_{REF}		2.5		V	
Reference resistance	R_{REF}		200		Ω	
Sampling clock	f_{samp}	0.1		50	MHz	
Sampling clock low level pulse width	t_{PWL}	10			ns	
Sampling clock high level pulse width	t_{PWH}	10			ns	
Data set up time	t_S	8			ns	
Data hold time	t_H	5			ns	
Digital input high level	V_{IH}	2.7			V	VLS=GND
Digital input low level	V_{IL}			0.4	V	VLS=GND
Compensation capacity	C_{COMP}		1.0		μF	

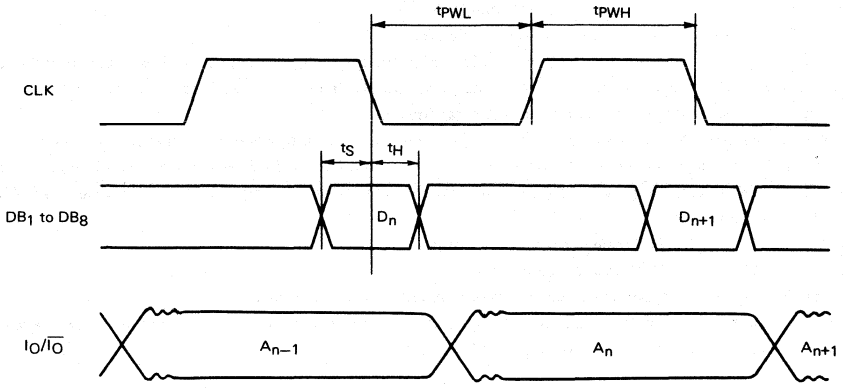
ELECTRICAL CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V ±0.5 V, f_{samp} = 50 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply current	I_{DD}		100		mA	f_{samp} = 50 MHz
Resolution	RES		8		bit	
Non-linearity error	NL		±0.25	±1	LSB	T_a=0 to 60 °C, V_{DD}=5 V ±0.25 V
Differential non-linearity	DNL		±0.1	±1	LSB	T_a=0 to 60 °C, V_{DD}=5 V ±0.25 V
Output compliance	V_O	1.0			V	V_{DD}=5.0 V
Full-scale current	I_{FS}		20.4		mA	V_{REF}=2.5 V, R_{REF}=200 Ω

TEST CIRCUIT



TIMING CHART



PIN DESCRIPTIONS

DGND (Pin 19) Digital system ground

AGND (Pins 11, 14) Analog system ground

DV_{DD} (Pins 6, 17) Digital system power supply (+5 V)

AV_{DD} (Pins 7, 16) Analog system power supply (+5 V)

The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6902C pins. Supply the digital system power from the analog power line through the low path filter to prevent from luch up.

I_{REF} (Pin 12) Full-scale current adjustment pin

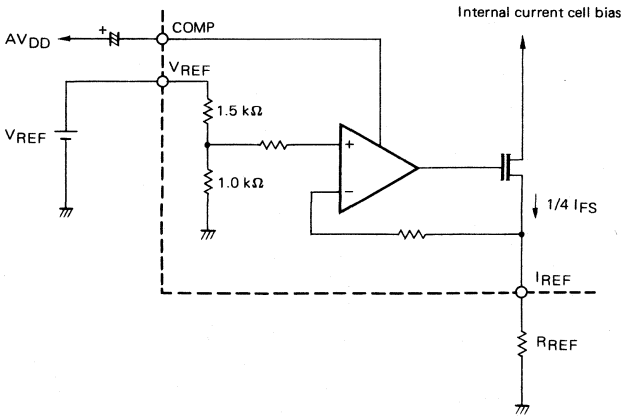
V_{REF} (Pin 15) Reference voltage input pin

These pins are used in adjustment of the analog output current (full-scale current).

The analog output current (full-scale current I_{FS}) is set by the reference voltage V_{REF} and the reference resistance R_{REF} connected between the I_{REF} pin and analog ground.

$$I_{FS} \fallingdotseq \frac{4}{2.5} V_{REF} / R_{REF}$$

$$I_{REF} = \frac{1}{2.5} V_{REF} / R_{REF}$$



The recommended reference voltage and reference resistance values are V_{REF} = 2.5 V and R_{REF} = 200 Ω respectively. The output analog current I_{FS} in this case will be 20 mA. Also connect by-pass capacitors of about 0.01 μF and 47 μF between the V_{REF} pin and AGND in the same way as the by-pass capacitors connected to the power pins.

COMP (Pin 13) Phase compensation capacitor connection

A capacitor for phase compensation of the internal amplifier is connected to this pin. Connect a 1.0 μF capacitor between this pin and analog V_{DD}.

DB_1 to DB_8 (Pins 20 to 22, Pins 1 to 5) Digital data input pins

DB_1 to DB_8 are the 8 bit digital data input pins. The code format is binary.

Digital input code								Analog output current
DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)	
0	0	0	0	0	0	0	0	0 note
0	0	0	0	0	0	0	1	1/256 I_{FS}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	253/256 I_{FS}
1	1	1	1	1	1	1	0	254/256 I_{FS}
1	1	1	1	1	1	1	1	255/256 I_{FS}

note : Excluding offset current

Digital data (DB_1 to DB_8) is latched by the falling edge of the sampling clock, and converted to corresponding analog outputs.

CLK (Pin 18) Sampling clock input pin

Digital data is latched by the falling edge of the clock signal applied to the sampling clock input pin, and is subsequently converted to analog outputs. The maximum clock frequency is 50 MHz.

I_O (Pin 9) Analog signal output pin

$\overline{I_O}$ (Pin 10) Complementary current output pin of I_O pin

These two pins are current output pins. The full-scale output current is determined by the reference resistance R_{REF} and reference voltage V_{REF}.

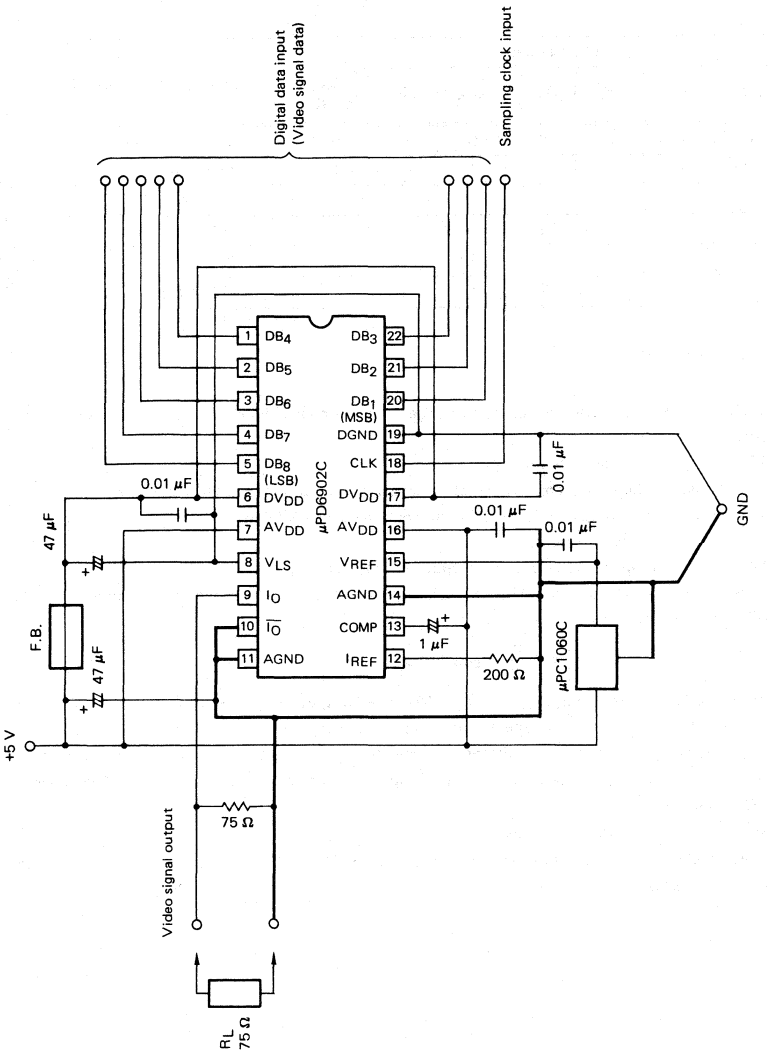
$$I_{FS} = I_O + \overline{I_O} = \frac{4}{2.5} V_{REF} / R_{REF}$$

$\overline{I_O}$ is the complementary current output pin of I_O. The added output current from the I_O and $\overline{I_O}$ pins becomes the full-scale current in accordance with the above equation. Analog output current can be easily converted to an analog output voltage by connecting a resistance between the I_O pin and analog ground. $\overline{I_O}$ pin cannot use for a complementary analog voltage output, because the compliance voltage of $\overline{I_O}$ pin is very low. Then connect $\overline{I_O}$ pin to the AGND directly.

V_{LS} (Pin 8) Digital input level select pin

This pin is used for digital input level selection. If connect to the GND the input level becomes TTL level, and to V_{DD} it becomes CMOS level.

APPLICATION CIRCUIT



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NEC reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

16 BIT D/A CONVERTER

The μPD6376 is a 16-bit D/A converter for digital audio equipment.

Resistance strings system and built-in 0-point offset circuit realizes high sound quality. This CMOS LSI operates on +5 V single power supply with low current consumption. As the pin 1 is "Low" or open, this IC's pin configuration is compatible with the μPD6372.

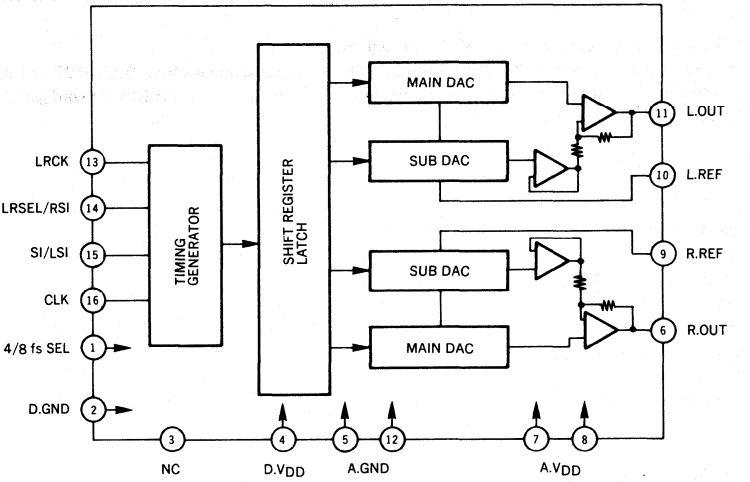
FEATURES

- +5 V single power supply
- CMOS configuration
- Built-in output operational amplifier
- Built-in 0-point offset circuit
- Resistance strings system
- 8 f_s (2 channels x 400 kHz) capability
- Built-in 2 channel DAC
- Symmetrical phase output

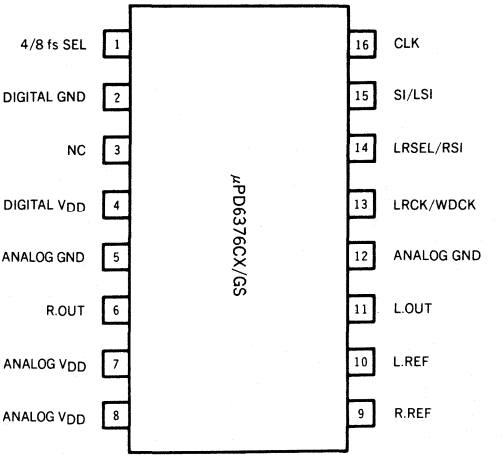
ORDERING INFORMATION

Ordering Name	Package
μPD6376CX	16-Pin Plastic DIP (300 mil)
μPD6376GS	16-Pin Plastic SOP (300 mil)

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V
Input Voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

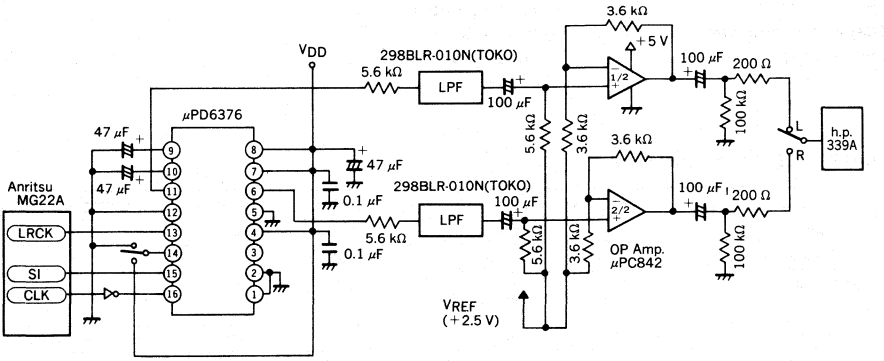
RECOMMENDED OPERATING RANGES

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
High-level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low-level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	
Ambient Temperature	T_a	−20	25	75	°C	
Load Resistance	R_L	5			kΩ	R.OUT, L.OUT terminal
Sampling Frequency	f_s			400	kHz	
Clock Frequency	f_{CLK}			10	MHz	
Clock Pulse Width	t_{SCK}	40			ns	
SI, LRCK Setup Time	t_{DC}	12			ns	
SI, LRCK Hold Time	t_{CD}	12			ns	

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = +5 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Resolution	RES		16		Bit	
Total Harmonic Distortion 1	THD_1		0.04	0.09	%	f_{IN} = 1 kHz, 0 dB
Total Harmonic Distortion 2	THD_2		0.1	0.3	%	f_{IN} = 1 kHz, −20 dB
Full Scale Output Voltage	V_{FS}		2.0	2.3	V_{p-p}	
Cross Talk	C.T	85	95		dB	One Side Channel 0 dB f_{IN} = 1 kHz
S/N Ratio	S/N	96			dB	JIS-A
Dynamic Range	D.R	92			dB	f_{IN} = 1 kHz, −60 dB
Supply Current	I_{DD}		6.0	12	mA	f_{IN} = 1 kHz, 0 dB

TEST CIRCUIT



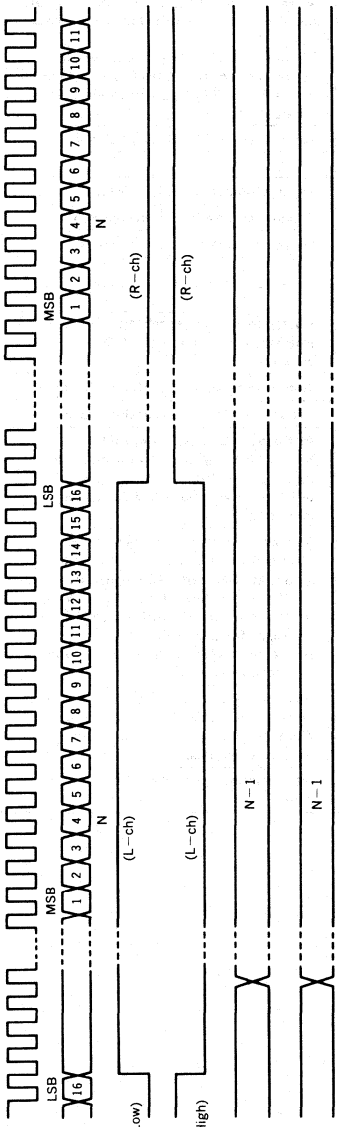
Sampling Frequency $f_S = 88.2$ kHz

TERMINAL FUNCTION

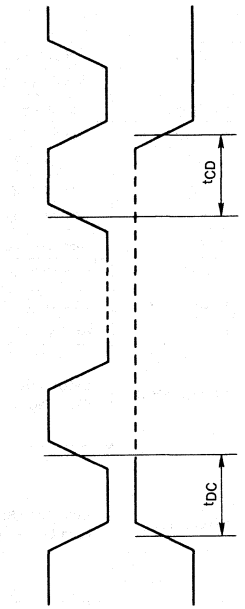
TERMINAL NO.	SYMBOL	TERMINAL NAME	DESCRIPTION	INPUT/ OUTPUT
1	4/8 f_s SEL	4/8 f_s Selection	As this terminal is "Low" or open, L-ch data and R-ch data are inputted for serial data by the pin 15. As this terminal is "High", L-ch data is inputted by the pin 15, R-ch data is inputted by the pin 14. (Pull-downed by the 100 kΩ resistance in IC.)	Input
2	D. GND	Digital GND	Ground terminal for the logic circuit	
3	NC	Non Connection	—	
4	D. V_{DD}	Digital V_{DD}	Power supply terminal for the logic circuit	
5	A. GND	Analog GND	Ground terminal for the analog circuit	
6	R. OUT	R-ch OUTPUT	Output terminal for the right analog signal	Output
7	A. V_{DD}	Analog V_{DD}	Power supply terminal for the analog circuit	
8	A. V_{DD}	Analog V_{DD}		
9	R. REF	R-ch Voltage Reference	Operational Amplifier reference bias terminal. Normally connected to A. GND via a capacitor.	
10	L. REF	L-ch Voltage Reference		
11	L. OUT	L-ch OUTPUT	Output terminal for the left analog signal	Output
12	A. GND	Analog GND	Ground terminal for the analog circuit	
13	LRCK/WDCK	Left/Right Clock Word Clock	As the pin 1 is "Low" or open, this is input terminal for left/right identification signal. As the pin 1 is "High", this is input terminal for word identification signal of input data.	Input
14	LRSEL/RSI	Left/Right Selection R-ch Series Input	As the pin 1 is "Low" or open, this is left/right selection terminal for LRCK signal. At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input. At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input. As the pin 1 is "High", this is input terminal for R-ch serial data.	Input
15	SI/LSI	Series Input L-ch Series Input	As the pin 1 is "Low" or open, this is input terminal for L-ch and R-ch serial data. As the pin 1 is "High", this is input terminal for L-ch serial data.	Input
16	CLK	Clock	Input terminal for read clock of serial input data.	Input

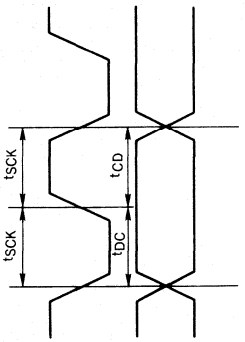
TIMING CHART 1

As the pin 1 is "Low" or open



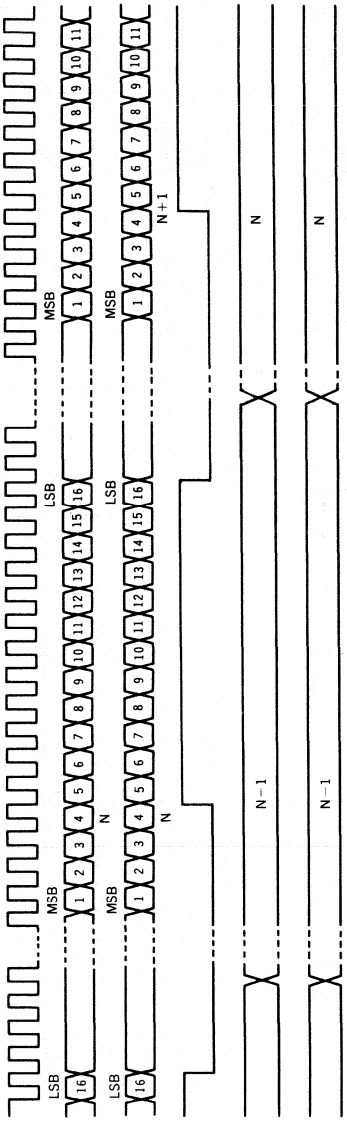
(NOTICE) At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input.
At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input.

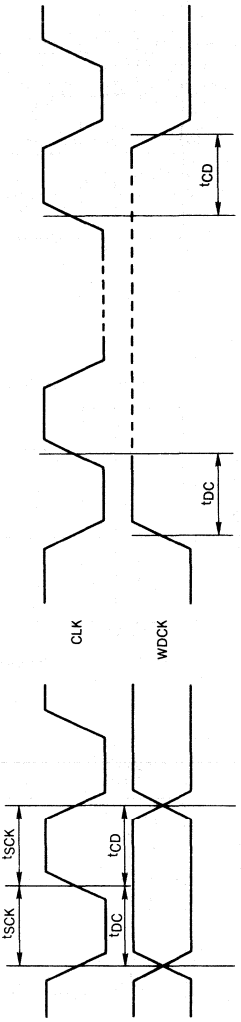




TIMING CHART 2

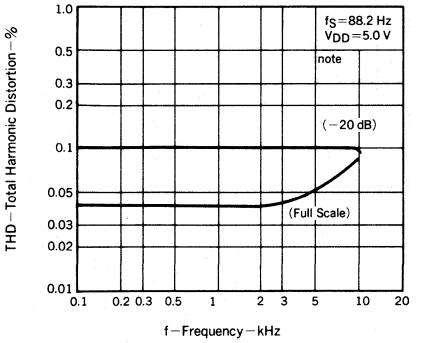
As the pin 1 is "High"



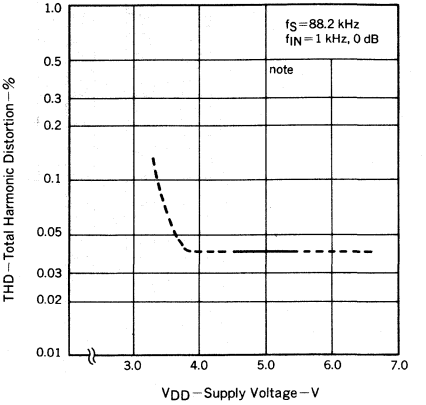


TYPICAL CHARACTERISTICS (T_a = 25 °C)

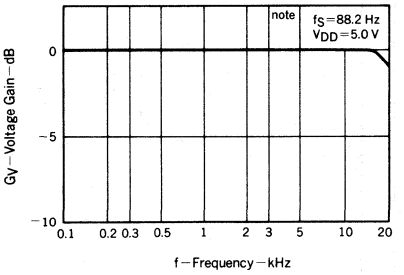
TOTAL HARMONIC DISTORTION vs. FREQUENCY



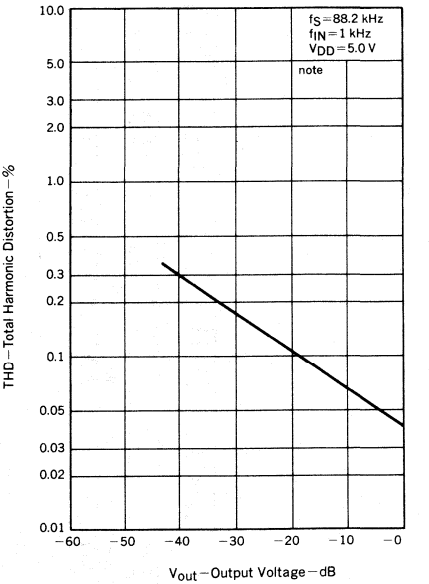
TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



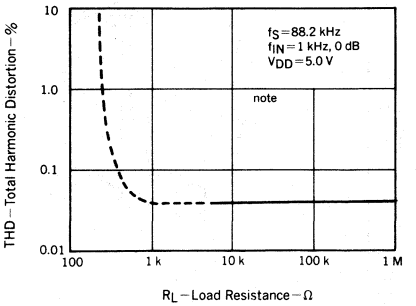
VOLTAGE GAIN vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



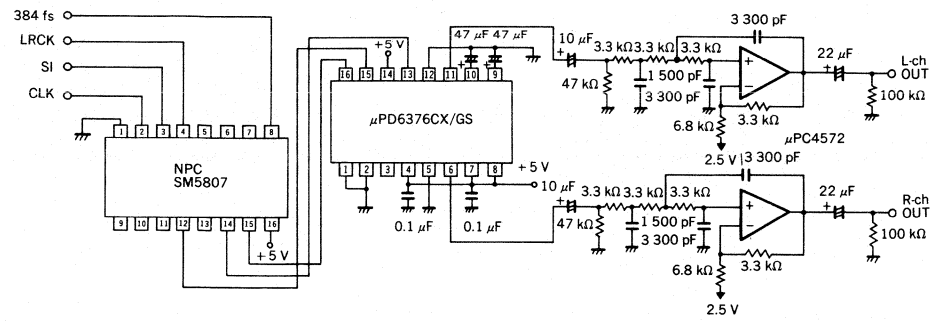
TOTAL HARMONIC DISTORTION vs. LOAD RESISTANCE



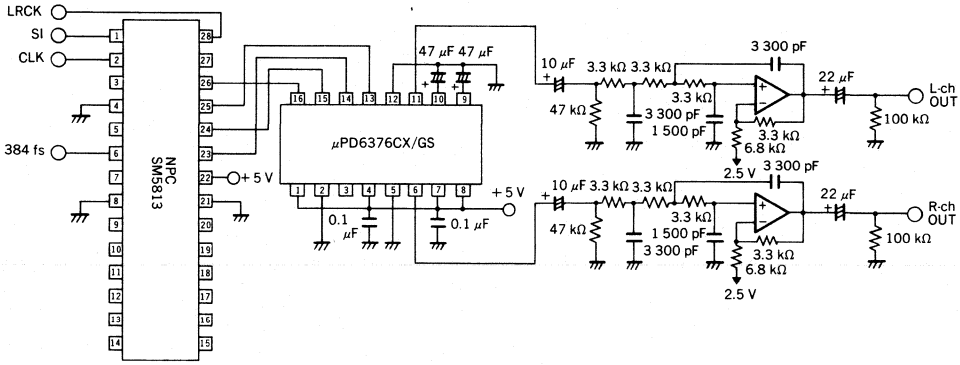
note. 20 kHz Low Pass Filter
: 298BLR-010N(TOKO)

APPLICATION CIRCUIT

(1) f_s to 4 f_s mode (L/R data serial input mode)



(2) 8 f_s mode (L/R data parallel input mode)



QUAD/OCTAL 6BIT D/A CONVERTER
CMOS LSI

DESCRIPTION

μPD6325 Serise are 6 bit D/A Converter for control volumn, brightness, contrast, color or tone of TV set. The data are transferring serially from micro-computers.

μPD6325 Serise Line-up	QUAD D/A	OCTAL D/A
D/A output is consist of Emitter follower buffer	μPD6325C, 6325G	μPD6326C
Non buffer output	μPD6335C, 6335G	μPD6336C

FEATURES

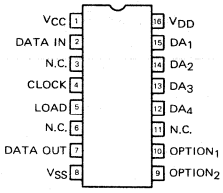
- R-2R ladder D/A
- Serial Data input (DATA IN, CLOCK, LOAD)
- Power supply voltage of interface is 5 V (V_{CC}) and D/A reference voltage is free (V_{CC} to 15 V).

ORDERING INFORMATION

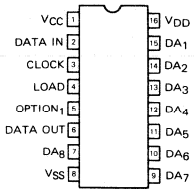
Part No.	Package
μPD6325C	16-pin plastic DIP (300 mil)
μPD6325G	16-pin plastic SOP (300 mil)
μPD6326C	16-pin plastic DIP (300 mil)
μPD6335C	16-pin plastic DIP (300 mil)
μPD6335G	16-pin plastic SOP (300 mil)
μPD6336C	16-pin plastic DIP (300 mil)

PIN CONNECTION DIAGRAM (Top View)

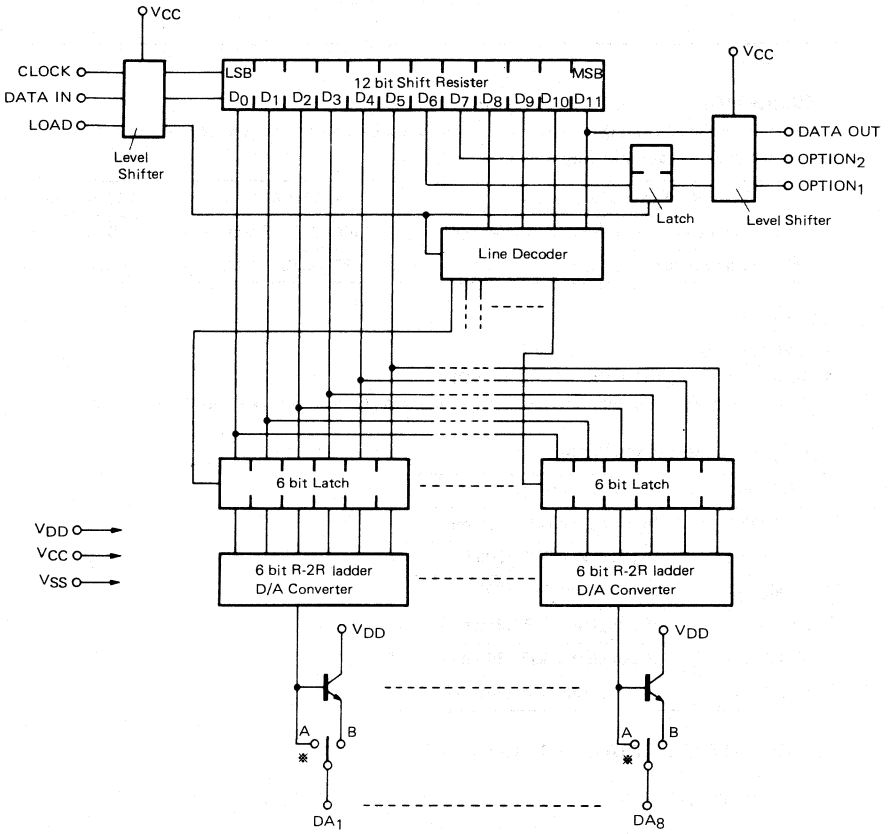
μPD6325, μPD6335



μPD6326, μPD6336



BLOCK DIAGRAM



* A ····· μPD6335, μPD6336
B ····· μPD6325, μPD6326

μPD6325, μPD6335 have Quad D/As.

PIN CONFIGURATION

Pin No.		Symbol	Pin Name	Function
μPD^{6325}_{6335}	μPD^{6326}_{6336}			
1	1	V_{CC}	Input Reference Voltage Supply	This pin is used to interface with the control IC (ex. micro processor). Supply the voltage high level of the control IC.
2	2	DATA IN	Serial Data Input	Control data input terminal. Data is read in synchronization with the clocks input to the CLOCK terminal.
4	3	CLOCK	Shift Clock Input	Data read clock input terminal. The Data input to the DATA IN terminal is read at the leading edge of the clock.
5	4	LOAD	Load Pulse Input	This terminal is used to input Load signals after inputting serial data. 12 bit data is read after leading edge of a pulse input to the LOAD terminal.
7	6	DATA OUT	Serial Data Output	Serial data output terminal. The final stage data of 12 bit shift register appeares on this terminal in synchronization with shift clock.
8	8	V_{SS}	Ground	System ground.
9	–	$OPTION_2$	Expantion Output Port	D_7 the data of the shift register appears on this terminal. (Only μPD6325 and μPD6335)
10	5	$OPTION_1$	Expantion Output Port	D_6 the data of the shift register apeares on this terminal.
–	7	DA_8	Analog Output Channel 8	Analog Output
–	9	DA_7	Analog Output Channel 7	Analog Output
–	10	DA_6	Analog Output Channel 6	Analog Output
–	11	DA_5	Analog Output Channel 5	Analog Output
12	12	DA_4	Analog Output Channel 4	Analog Output
13	13	DA_3	Analog Output Channel 3	Analog Output
14	14	DA_2	Analog Output Channel 2	Analog Output
15	15	DA_1	Analog Output Channel 1	Analog Output
16	16	V_{DD}	Power Supply	Reference Voltage for D/A converters. Analog output voltage range is GND–V_{DD}.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}, V_{CC}	−0.5 to +18, $V_{CC} \leqq V_{DD}$	V
Output Voltage	V_{OUT}	−0.5 to V_{DD} +0.5	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Input Current	I_{IN}	10	mA
Emitter Follower Current	I_{OE}	10	mA
Power Dissipation	P_D	500*/200**	mW
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C

*DIP
** SOP

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage*	V_{DD}	V_{CC}		15	V
Supply Voltage of Interface	V_{CC}	4.5		5.5	V

* V_{DD} Voltage should be higher than V_{CC} Voltage at all time.

ELECTRICAL CHARACTERISTICS

(T_a = −40 to +85 °C, V_{SS} = 0 V, V_{CC} = 4.5 to 5.5 V, V_{DD} = V_{CC} to 15 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Operating Voltage	V_{DD}	V_{CC}		15	V	
Input Reference Voltage	V_{CC}	4.5		5.5	V	
Current Consumption	I_{DD}			10	mA	No Load
Low Level Input Voltage	V_{IL}	0.8			V	V_{CC} = 5 V
High Level Input Voltage	V_{IH}			3.5	V	V_{CC} = 5 V
Input Leak Current	$I_{I\ LEAK}$			±1	μA	V_{IN} = V_{CC} or V_{SS}
DATA OUT High Level Output Voltage	I_{OH}	−100			μA	V_{OH} = V_{DD} −0.5 V
DATA OUT Low Level Output Voltage	I_{OL}	100			μA	V_{OL} = 0.5 V
Emitter Follower Leak Current	I_{OLEAK}			20	μA	for μPD6325, 6326
Emitter Follower Power Dissipation	P_E/unit			5	mW	T_a = 85 °C for μPD6325, 6326
Emitter Follower Power Dissipation	P_E/unit			15	mW	T_a = 70 °C for μPD6325, 6326
Emitter Follower Power Dissipation	P_E/total			25	mW	T_a = 85 °C for μPD6325, 6326
Emitter Follower Power Dissipation	P_E/total			75	mW	T_a = 70 °C for μPD6325, 6326
Settling Time	$t_{DA\ set}$			10	μs	*

* μPD6325, 6326: R_L = 20 kΩ, C_L = 50 pF
μPD6335, 6336: No Load.

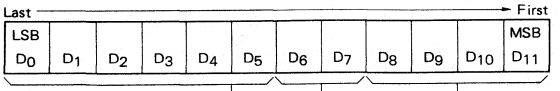
SWITCHING CHARACTERISTICS

(T_a = −40 to +85 °C, V_{SS} = 0 V, V_{CC} = 5 V, V_{DD} = V_{CC} to 15 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
CLOCK High Level Width	t_{CH}	4.0	0.2		μs
CLOCK Low Level Width	t_{CL}	10	1.5		μs
CLOCK Rise Time	t_{Cr}			1.0	μs
CLOCK Fall Time	t_{Cf}			1.0	μs
DATA IN Setup Time	t_{Dsetup}	2.0	0.1		μs
DATA IN Hold Time	t_{Dhold}	10	1.5		μs
Pulse Width, LOAD High	$t_{W(LOAD)}$	4.0	0.2		μs
LOAD Lead Time	t_{Llead}	10	1.5		μs
LOAD Lag Time	t_{Llag}	10	1.5		μs

DATA CONFIGURATION

Data Length is 12 bit.



D/A output CONTROL BIT

D_{11}	D_{10}	D_9	D_8	Select D/A	Target device
0	0	0	0	Don't Care	μPD6325, 6326 μPD6335, 6336
0	0	0	1	DA_1	"
0	0	1	0	DA_2	"
0	0	1	1	DA_3	"
0	1	0	0	DA_4	"
0	1	0	1	DA_5	μPD6326 μPD6336
0	1	1	0	DA_6	"
0	1	1	1	DA_7	"
1	0	0	0	DA_8	"
1	X	X	X	Don't Care	μPD6325, 6326 μPD6335, 6336

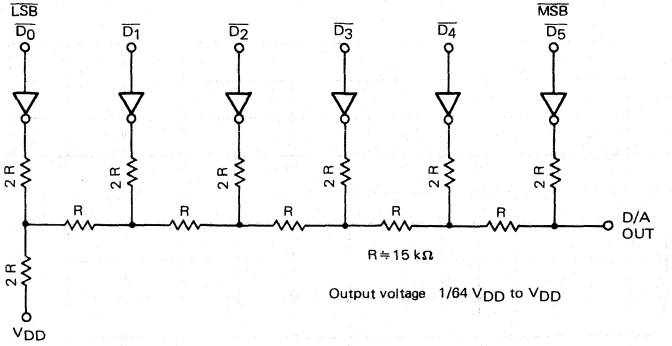
OPTION output CONTROL BIT

D_7	D_6	$OPTION_1$ out.	$OPTION_2$ out.	Note
0	0	L	L	OPTION2 is only μPD6325, 6326
0	1	H	L	"
1	0	L	H	"
1	1	H	H	"

D/A Output Voltage CONTROL BIT

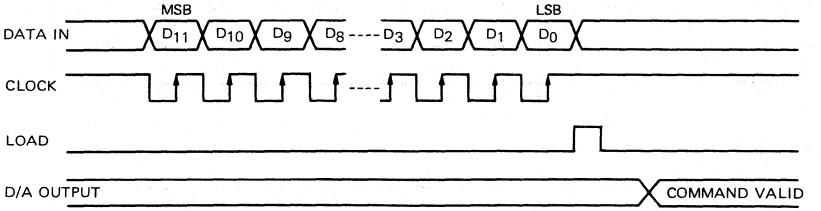
D_5	D_4	D_3	D_2	D_1	D_0	Output Voltage
0	0	0	0	0	0	$\fallingdotseq V_{DD}/64$
0	0	0	0	0	1	$\fallingdotseq 2 \times V_{DD}/64$
0	0	0	0	1	0	$\fallingdotseq 3 \times V_{DD}/64$
0	0	0	0	1	1	$\fallingdotseq 4 \times V_{DD}/64$
⟆	⟆	⟆	⟆	⟆	⟆	⟆
1	1	1	1	1	0	$\fallingdotseq 63 \times V_{DD}/64$
1	1	1	1	1	1	$\fallingdotseq V_{DD}$

EQUIVALENT CIRCUIT OF 6 bit D/A

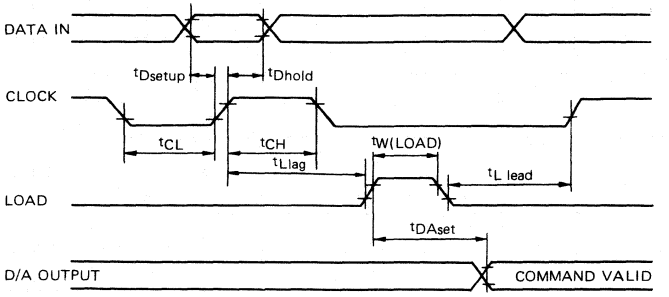


Output voltage 1/64 V_{DD} to V_{DD}

TIMING CHART

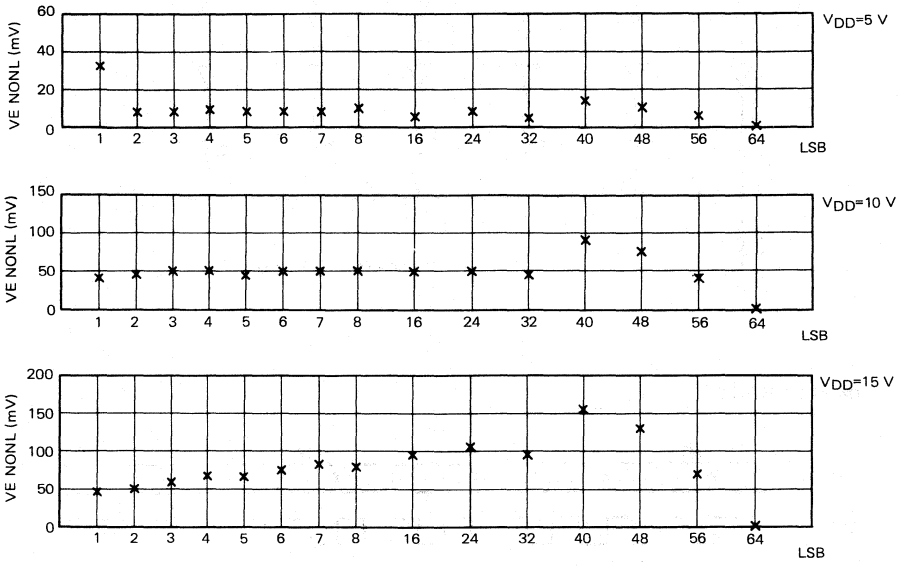


Data is loaded when LOAD is high level.

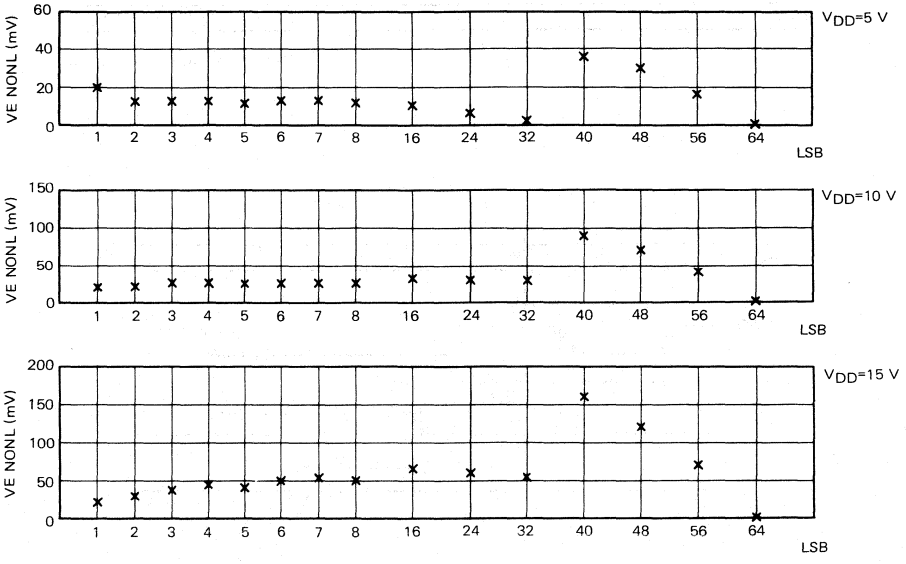


LINIARITY OF D/A OUTPUT (μPD6335, 6336)

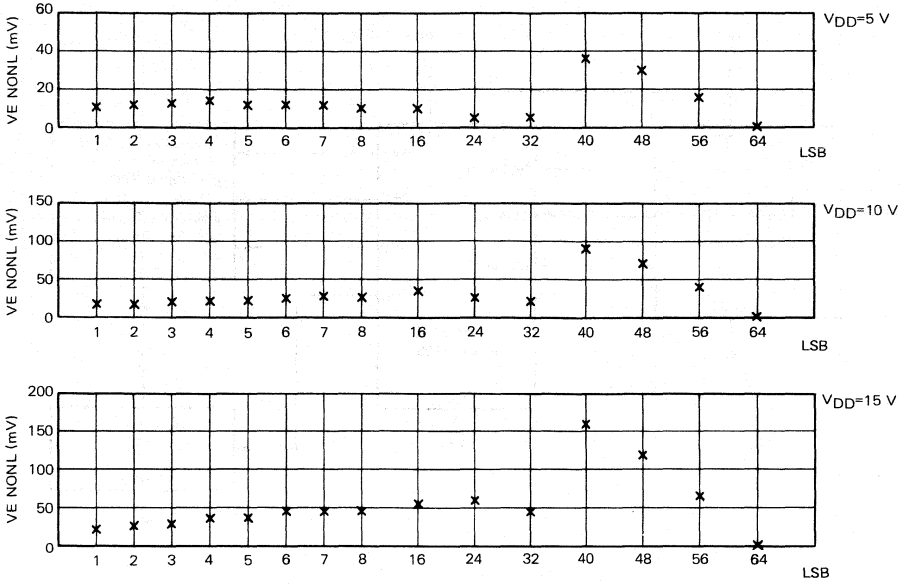
- $T_a = -40\,^{\circ}C$



- $T_a = 25\,^{\circ}C$

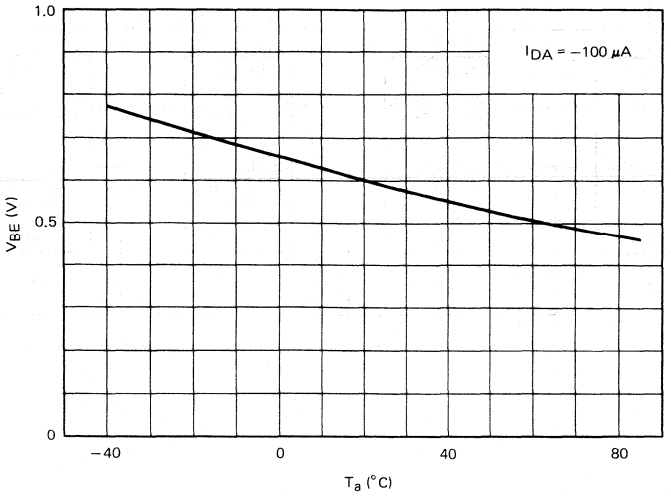


• T_a = 85 °C

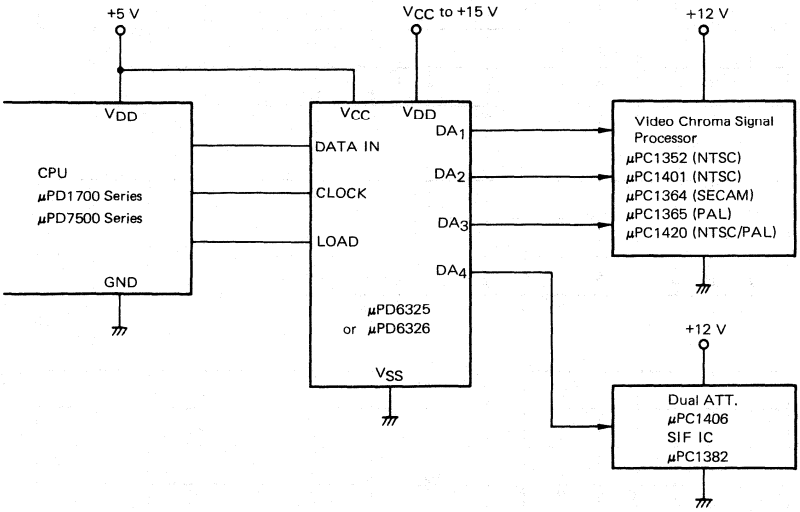


* VE NONL = (MEASUREMENT VALUE) – (IDEAL VALUE)

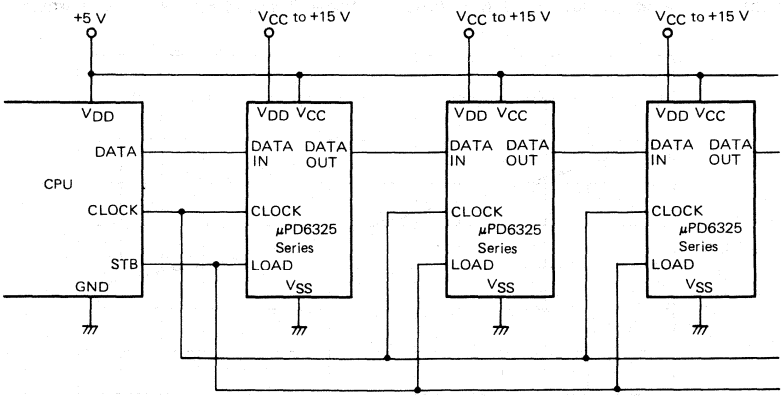
Emitter follower buffer (μPD6325, 6326)'s Voltage between Base and Emitter vs Temperature



APPLICATION FOR TV SET



APPLICATION FOR CASCADE CONNECTING



8-BIT NMOS D/A CONVERTER

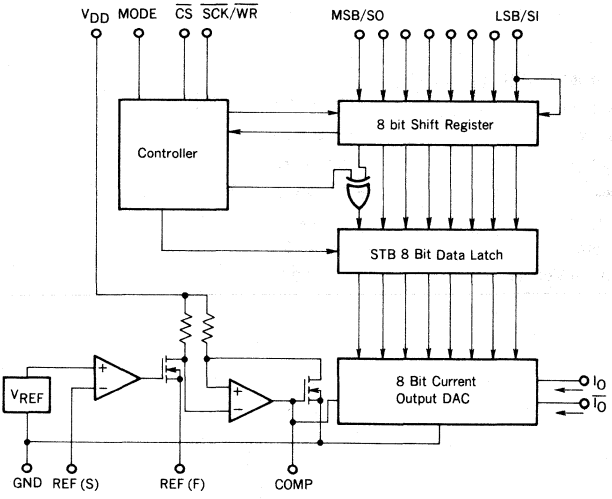
The μPD7011 is a low cost 8-bit NMOS digital-to-analog converter using Enhancement Depletion (ED) technology. The μPD7011 features single +5 V power supply operation and on board voltage reference.

The serial interface option allows easy interface to the μCOM-87, and -75 series of single chip microcomputers and the μPD7720 Signal Processing chip (SPI). In parallel mode the μPD7011 is easily connected to the 8080 and 8085 type bus structures by the bus interface facilities.

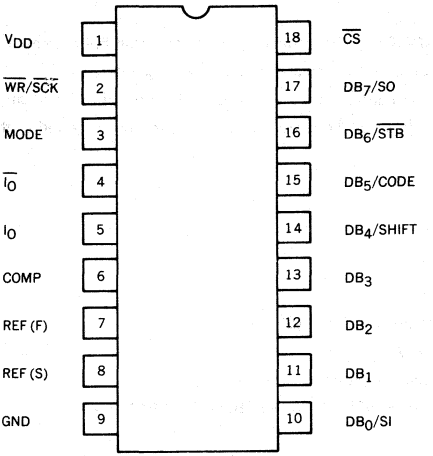
FEATURES

- E/D NMOS monolithic
- Internal voltage reference
- Serial interface with μCOM-87, -75 and μPD7720 (SPI)
- Bus interface with 8080 and 8085A-2
- Pure binary and 2's complement code available in serial mode
- Two performance ranges linearity error: μPD7011C, 1 LSB; μPD7011C-1, 1/2 LSB
- Single +5 V power supply
- 18-pin plastic DIP (300 mil)

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



μPD7011C, 7011C-1

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Operating Temperature	−20 to +70	°C
Storage Temperature	−65 to +150	°C
Power Supply Voltage	−0.3 to +7.0	V
All Input Voltages	−0.3 to V_{DD} +0.3	V
Power Dissipation	300	mW
SO Pin Pull-up Voltage	V_{DD} +0.3	V
$I_O/\overline{I_O}$ Output Pull-up Voltage	+10	V

RECOMMENDED OPERATING CONDITIONS (T_a = +25 °C)

PARAMETER	SYMBOL	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Reference Current	I_{REF}	225	250	275	μA
Full-Scale Current	I_{FS}	0.9	1.0	1.1	mA
Reference Force Terminal Voltage	$V_{REF(F)}$	2.65	2.7	2.75	V
Low-Level Logic Input	V_{IL}	0		0.8	V
High-Level Logic Input	V_{IH}	2.0		V_{DD}	V
Analog Output Pull-up Voltage		2.4		3.0	V
SO Pin 17 Output Pull-up Voltage			V_{DD}		V
Frequency Compensation Capacitor (See Note)	C_{COMP}	0.01	0.1	1.0	μF

Note: Using a frequency compensation capacitor larger than 1 μF will promote low noise operation of the μPD7011C. However, the turn-on time at initial power on will increase.

DC CHARACTERISTICS (V_{DD} = 5±0.25 V, T_a = 25 °C, I_{FS} = 1 mA, C_{COMP} = 0.1 μF)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Resolution		8	8	8	Bits	−20 °C to +70 °C
Nonlinearity, 7011C-1	NL		0.25	0.5	LSB	−20 °C to +70 °C
Nonlinearity, 7011C	NL		0.5	1	LSB	−20 °C to +70 °C
Differential Nonlinearity	DNL		0.1	1.0	LSB	−20 °C to +70 °C
Zero-Scale Error				0.5	LSB	−20 °C to +70 °C
Zero-Scale Symmetry		−1.5	−1.0	−0.5	LSB	Note 1
Gain Error, 7011C-1				3	%FSR	
Gain Error, 7011C				5	%FSR	Note 2
Full-Scale Symmetry		−1.5	−1.0	−0.5	LSB	Note 3
Reference Voltage	$V_{REF}(S)$	1.41	2.0	2.59	V	
Power Supply Current	I_{DD}		7	13	mA	
Logic Input Leakage	I_{ILEAK}		0.1	10	μA	$0 \leq V_I \leq V_{DD}$
Low-Level Output Voltage	V_{OL}			0.5	V	SO (Pin 17) $I_{SINK} \leq 2$ mA
Output Leakage	I_{OH}		0.1	10	μA	SO (Pin 17) $V_O = V_{DD}$
Full-Scale Drift			70		PPM/°C	$\Delta I_O(FS)/\Delta T$
Supply Voltage 7011C-1 Rejection Ratio	SVRR			0.8	%FSR/V	$\Delta I_O(FS)/\Delta T$
Supply Voltage 7011C Rejection Ratio	SVRR			1.2	%FSR/V	$\Delta I_O(FS)/\Delta V_{DD}$
Analog Output Compliance		2.4		8.0	V	$\Delta I_O(FS) \leq 1$ LSB

Notes: 1. Zero-scale symmetry is defined as follows:
$255(I_O(ZS) - \overline{I_O}(ZS))/I_O(FS)$.
2. Gain error is defined as follows:
$100(I_O(FS) \times 256/255 - 4I_{REF})/4I_{REF}$.
3. Full-scale symmetry is defined as follows:
$255(I_O(ZS) - \overline{I_O}(ZS))/I_O(FS)$.

AC RECOMMENDED CONDITIONS (T_a = 25 °C, V_{DD} = 5±0.25 V, Note 1)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Serial Mode						
Serial Clock Setup Time	t_{SKCS}	30			ns	$\overline{SCK}$ ↑ → $\overline{CS}$ ↓
CS Setup Time	t_{SCSK}	300			ns	$\overline{CS}$ ↓ → $\overline{SCK}$ ↑
Data Setup Time	t_{SIK}	120			ns	SI → $\overline{SCK}$ ↑
Data Hold Time	t_{HKI}	50			ns	$\overline{SCK}$ ↑ → SI
High-Level Serial Clock Pulse Width	t_{WHK}	300			ns	
Low-Level Serial Clock Pulse Width	t_{WLK}	300			ns	
Strobe Hold Time	t_{HKST}	100			ns	$\overline{SCK}$ ↑ → $\overline{STB}$ ↑
High-Level Strobe Pulse Width	t_{WHST}	200			ns	
Low-Level Strobe Pulse Width	t_{WLST}	200			ns	
Chip Select Hold Time	t_{HKCS}	0			ns	$\overline{SCK}$ ↑ → $\overline{CS}$ ↑
Serial Clock Hold Time	t_{HCSK}	100			ns	$\overline{CS}$ ↑ → $\overline{SCK}$ ↓
Strobe Setup Time	t_{SSTCS}	300			ns	$\overline{STB}$ ↑ → $\overline{CS}$ ↓
Parallel Mode						
Address Setup Time	t_{AW}	0			ns	$\overline{CS}$ ↓ → $\overline{WR}$ ↓
Low-Level WR Pulse Width	t_{WW}	200			ns	
Address Hold Time	t_{WA}	0			ns	$\overline{WR}$ ↑ → $\overline{CS}$ ↑
Data Setup Time	t_{DW}	180			ns	DB → $\overline{WR}$ ↑
Data Hold Time	t_{WD}	0			ns	$\overline{WR}$ ↑ → DB

Note: t_r, $t_f \leq 50$ ns.

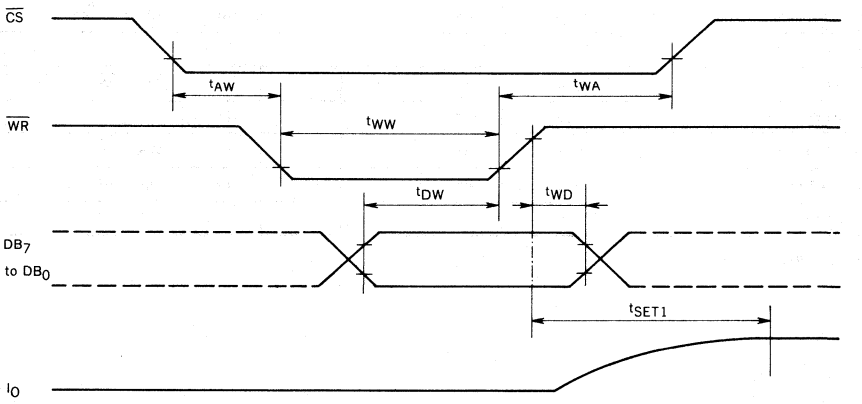
AC CHARACTERISTICS (T_a = 25 °C, V_{DD} = 5±0.25 V)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Analog Output Setting Time	t_{SET1}		1	3	μs	Parallel Mode, Note 1
	t_{SET2}		1	3	μs	Serial Mode, Note 2
Serial Data Delay Time	t_{DKO}			450	ns	SCK ↓ → SO. Note 2
Delay Time T_D Floating S_O	t_{FCSO}			250	ns	CS ↑ → SO, High Impedance

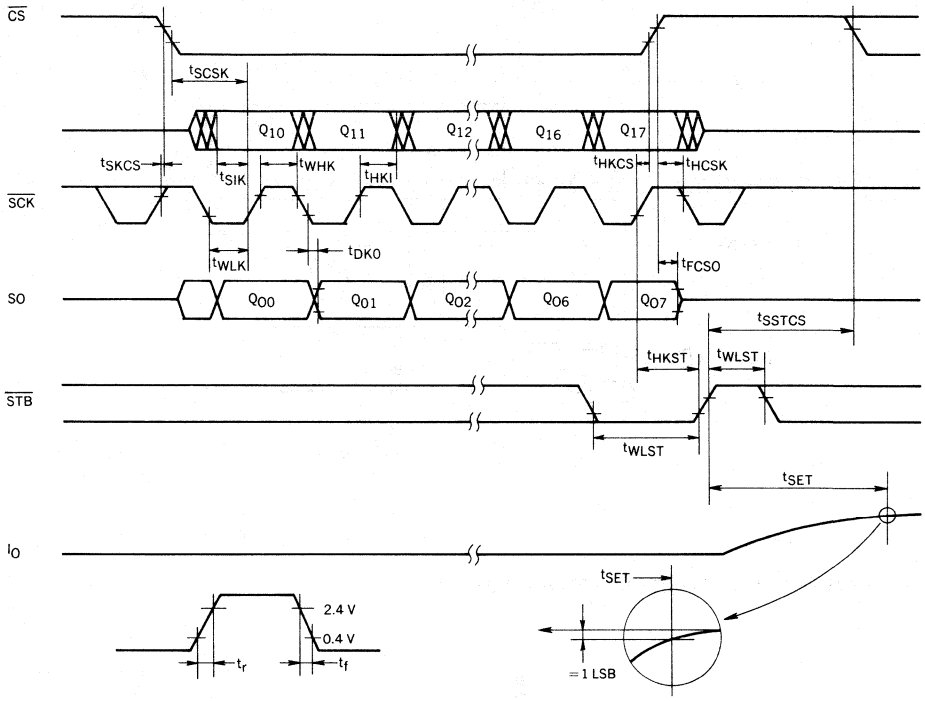
Notes: 1. $R_L \leq 2\ k\Omega$; $C_L \leq 20\ pF$.
2. $R_L = 2\ k\Omega$; $C_L \leq 20\ pF$.

TIMING CHART

1. Parallel Mode (MODE = L)

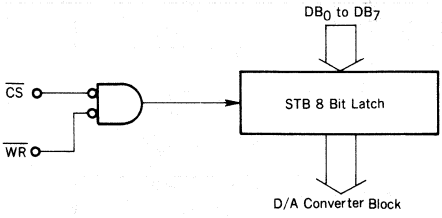


2. Serial Mode (MODE = H)

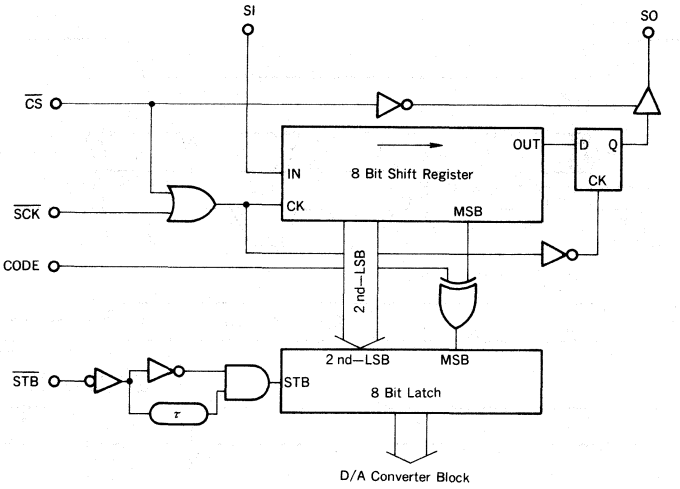


CONTROL BLOCK OPERATION

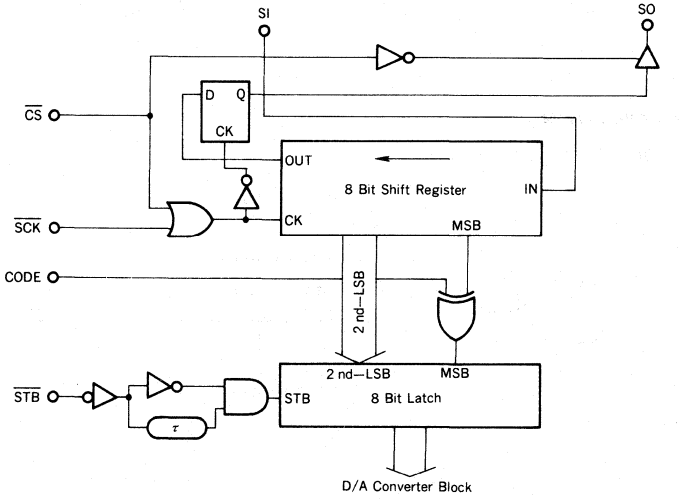
1. Parallel Mode (MODE = LOW)



2. Serial Mode, MSB First (SHIFT = MODE = High)

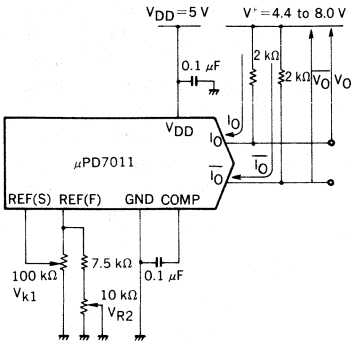


3. Serial Mode, LSB First (SHIFT = Low, MODE = High)



TYPICAL APPLICATIONS

Correction Diagram



(V_{DD} = 5 V, V^+ = 5 V)

Digital Input MSB LSB	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)	V_O(V)	$\overline{V_O}$(V)
1 1 1 1 1 1 1 1	0.996	0.004	1.992	0.008
1 1 1 1 1 1 1 0	0.992	0.008	1.984	0.016
⋮ ⋮ ⋮	⋮	⋮	⋮	⋮
1 0 0 0 0 0 0 1	0.504	0.496	1.008	0.992
1 0 0 0 0 0 0 0	0.500	0.500	1.000	1.000
0 1 1 1 1 1 1 1	0.496	0.504	0.992	1.008
⋮ ⋮ ⋮	⋮	⋮	⋮	⋮
0 0 0 0 0 0 0 1	0.004	0.996	0.008	1.992
0 0 0 0 0 0 0 0	0.000	1.000	0.000	2.000

Adjustment Procedure

a. Set $V_{REF}(F)$ = 2.7 V by V_{R1}

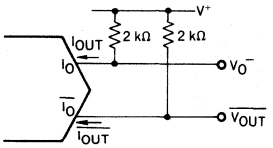
b. After latching full-scale digital input, set V_O = 2.0 V by V_{R2}

Notes: 1. Both I_O and $\overline{I_O}$ must use pull-up resistors.

2. Use resistors of 1 % accuracy.

3. Capacitive load at $V_{REF}(F)$ pin should be less than 15 pF.

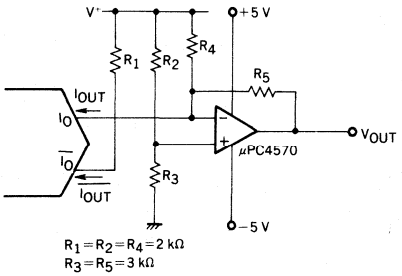
(1) V_{OUT} = 3 to 5 V, $\overline{V_{OUT}}$ = 5 to 3 V



(V_{DD} = V^+ = 5 V)

Digital Input MSB LSB	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)
1 1 1 1 1 1 1 1	0.996	0.004	3.008	4.992
1 1 1 1 1 1 1 0	0.992	0.008	3.016	4.984
⋮ ⋮ ⋮	⋮	⋮	⋮	⋮
1 0 0 0 0 0 0 0	0.500	0.500	4.000	4.000
⋮ ⋮ ⋮	⋮	⋮	⋮	⋮
0 0 0 0 0 0 0 1	0.004	0.996	4.992	3.008
0 0 0 0 0 0 0 0	0.000	1.000	5.000	3.000

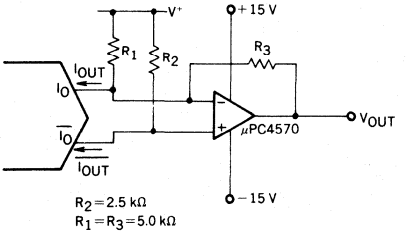
(2) V_{OUT} = 0 to 3 V



(V_{DD} = V^+ = 5 V)

Digital Input MSB LSB	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)	V_{OUT} (V)
1 1 1 1 1 1 1 1	0.996	0.004	2.988
1 1 1 1 1 1 1 0	0.992	0.008	2.976
⋮ ⋮ ⋮	⋮	⋮	⋮
1 0 0 0 0 0 0 0	0.500	0.500	1.500
⋮ ⋮ ⋮	⋮	⋮	⋮
0 0 0 0 0 0 0 1	0.004	0.996	0.012
0 0 0 0 0 0 0 0	0.000	1.000	0.000

(3) V_{OUT} = 0 to 10 V

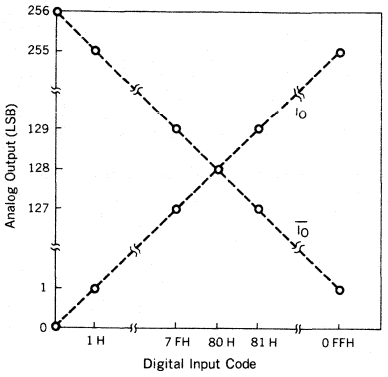


(V_{DD} = V^+ = 5 V)

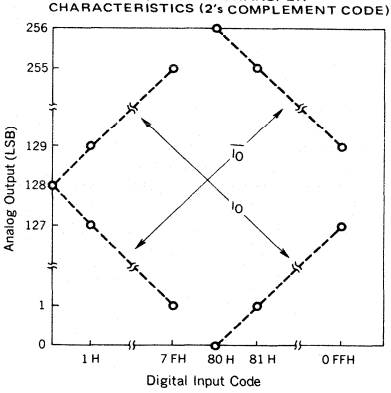
Digital Input MSB LSB	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)	V_{OUT} (V)
1 1 1 1 1 1 1 1	0.996	0.004	9.96
1 1 1 1 1 1 1 0	0.992	0.008	9.92
⋮ ⋮ ⋮	⋮	⋮	⋮
1 0 0 0 0 0 0 0	0.500	0.500	5.00
⋮ ⋮ ⋮	⋮	⋮	⋮
0 0 0 0 0 0 0 1	0.004	0.996	0.04
0 0 0 0 0 0 0 0	0.000	1.000	0.00

OPERATING CHARACTERISTICS (T_a = 25 °C)

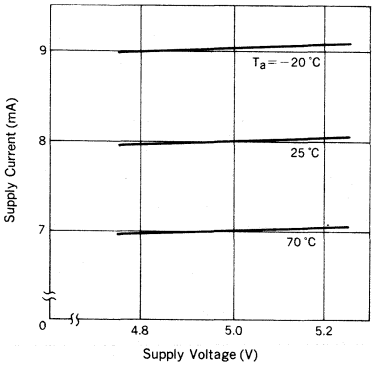
IDEAL INPUT/OUTPUT TRANSFER CHARACTERISTICS (BINARY CODE)



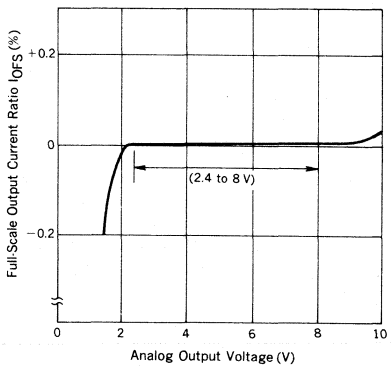
IDEAL INPUT/OUTPUT TRANSFER CHARACTERISTICS (2's COMPLEMENT CODE)



SUPPLY VOLTAGE vs. CURRENT CHARACTERISTICS



FULL-SCALE OUTPUT COMPLIANCE



Home automation

Section 3 - Home automation

D2B (Domestic Digital Bus) Interface IC

The μPD6316 is a D2B interface integrated circuit used to transfer data between various types of one-chip microcomputers.

A D2B is a two-wire serial bus interface that transfers data between electronic units such as television sets, VCRs and audio equipment.

Some of its applications are in home automation bus interfaces and automobile electronics control bus interfaces.

3

FEATURES

- D2B interface LSI device (Supports modes 0, 1 and 2)
  Mode 0: 209 bytes/second
  Mode 1: 2457 bytes/second
  Mode 2: 7760 bytes/second
- Internal D2B driver/receiver
- Interface with Microcomputer
  Three-wire serial interface ($\overline{SCK}$, SO, SI)
- Transmit data buffer: 4 bytes
- Receive data buffer: 20 bytes
- Operating clock: 12 MHz (crystal/ceramic oscillator)
- Operating voltage range: 5 V ±5 %

ORDERING INFORMATION

Order Code	Package
μPD6316CX	16-pin plastic DIP (300 mil)
μPD6316GS	16-pin plastic SOP (300 mil)

1. OPERATIONAL DESCRIPTION

1.1 Operational Overview

The μPD6316 is a D2B interface CMOS LSI device. It is a data transfer system whose purpose is to transfer data between electronic equipment such as television sets, VCRs and audio equipment. The μPD6316 links up with the one-chip microcomputers internal to this electronic equipment. For link up, it uses a three-wire serial interface.

The data and commands required to transmit data from the host controller (microcomputer) travel through the serial interface. During data transmission, signals are output from the D2B interface pins (D2B- and D2B+) by placing data in the μPD6316 from the host interface through the serial interface. In addition, data received from the D2B pins can be read through the serial interface.

1.2 D2B Interface System

The D2B interface is a two-wire data transmission system. Because a D2B interface uses a multiple master bus system, data can be transmitted from an optional electronic unit to another electronic unit. Three transmission speeds can also be used, mode 0 (209 bytes/second), mode 1 (2457 bytes/second) and mode 2 (7760 bytes/second). When using the low-noise twisted pair cables with the D2B interface, maximum length is 150 meters and the maximum number of units that can be connected together is 50.

1.2.1 Bus Priority determination (Arbitration)

When an electronic unit connected to the D2B interface controls another electronic unit, an operation to occupy the bus takes place. This operation is called arbitration. With arbitration, processing, if a number of electronic units attempted to transmit simultaneously, only one of the devices would be given permission to transmit. In order for an electronic unit to get permission to occupy the bus through arbitration, the following conditions must be met.

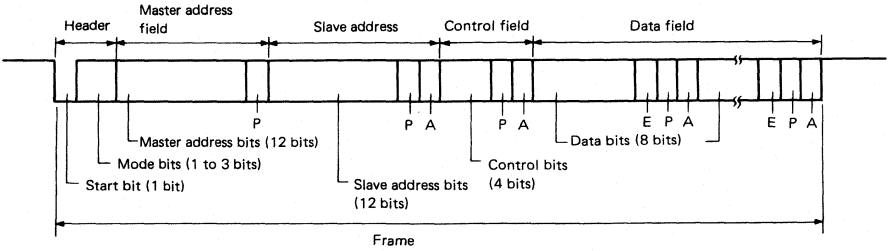
① The mode of the device must be lower than the other devices. For example, mode 0 has priority over mode 1.

② If the modes of the devices are the same, the master address of one of the devices must be lower than that of the other to gain priority. For example, the master address is composed of 12 bits, which makes address 000H the highest priority and address FFFH the lowest priority.

1.2.2 Transmission protocol

The D2B interface transmission signal format is shown in the following section. The data is transmitted as a series of signals called frames. The amount and speed of the data transmitted will vary with the mode.

Fig. 1-1 The D2B Signal Format



P = parity bit, A = Acknowledge bit, E = end of data bit

(1) The start bit

The start bit is a signal which tells the other units that data transmission will start. The unit that is about to start data transmission will output a low level signal (the start bit) at a specified time and then shift to the mode bit. If another piece of equipment is already outputting a start bit, the unit will not output the start bit. It will wait until the end of the current start bit and then shift to the mode bit. Units other than that about to transmit will detect this start bit and shift to the receive mode. The start bit output timing is the same for modes 0, 1 and 2.

(2) The mode bits

The mode bit is a signal that transmits the data transmission speed to the other electronic units. The D2B interface has communications modes with three different transmission speeds. The transmission speed is selected by the mode bits. After the mode bit output, there is a shift to the master address field output. The values of the mode bits are shown in the following table.

Table 1-1 Mode Bits

Communications modes	Mode bits	Transmission speed (Bytes/second)		Maximum number of transmission bytes (Bytes/frame)	
		Master/ slave	Slave/ master	Master/ slave	Slave/ master
0	0 (1 bit)	209	198	2	2
1	10 (2 bits)	2457	1497	32	16
2	110 (3 bits)	7760	5355	128	64

Devices in the receive mode will enter the standby mode (monitoring) when they detect that the value of the transmission mode is higher than the value they are able to support. The number of modes that compose the mode bit will vary according to the communications mode established for a unit. After mode bit has been set, transmission will take place at the speed of the specified transmission mode.

(3) Master address field

The purpose of the master field is to allow an electronic unit to transmit its unit address (master address) to other electronic units. The master address field is composed of 12 master address bits and a parity bit. If two or more electronic units begin transmission at the same time in the same mode, arbitration will take place in the master address field. In the master field, for each bit it transmits, the device compares the data it outputs with the data in the bus. If the results of this comparison shows that the device is outputting a master address different from the data in the bus, this will mean that the unit was unsuccessful at arbitration and it will stop transmitting. Because the D2B interface is configured with a wired AND, among the devices that participate in arbitration (arbitration masters), that with the first master address will win at arbitration. After outputting a 12-bit master address, only one device will remain in the transmit condition as the master unit. The master unit will next output a parity bit, ascertain the master addresses of the other units and shift to slave field output. The master address is composed of 12 bits and it is output from the most significant bits.

* Odd parity is used. When the number of 1 bits within the master address is even, the parity bit is 1.

(4) Slave address field

The purpose of the slave address field is to transmit the address (slave address) of the unit that wishes to transmit (slave address). The slave address field is composed of 12 slave address bits, a parity bit and an acknowledge bit. The slave address is composed of 12 bits and is output from the most significant bits. After the transmission of a 12-bit slave address, the parity bit is output as a means of preventing the slave address from accidentally receiving data. Next, in order to check whether the slave unit exists at the bus, the master unit will detect an acknowledge signal from the slave unit. If it detects such a signal, it will then shift to control field output. When the slave unit detects that there is agreement with the slave address and that both master and slave addresses are odd parity, it will output an acknowledge signal. If the slave unit is even parity, it will determine that either the master address or the slave address was not received accurately and it will not output an acknowledge signal. At this time, the master unit will go on standby (monitor) and communications will cease. If slave unit specified by the master unit and capable of receiving does not exist on the bus, the master unit will enter the standby mode and communications will cease because that is no unit to return an acknowledge signal to it.

(5) The control field

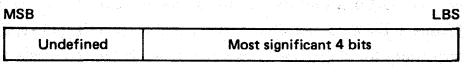
The purpose of the control field is to transmit the type and direction of the next data field. The control field is composed of 4 control bits, a parity bit and an acknowledge bit. The control bit is composed of 4 bits and is output from the most significant bits.

A parity bit is output after the control bits. When there is odd parity and the master unit's requested function can be executed by the slave, the slave unit transmits an acknowledge signal. The slave unit will not transmit an acknowledge signal even though the parity is odd if it cannot execute the master unit's request or if the parity is even. After the master unit confirms the acknowledge signal, it shifts to the output of the next data field. If the acknowledge signal cannot be confirmed, the master unit enters the standby mode and communication ends. The functions of the control bits are listed in the table below.

Table 1-2 Control Bit Functions

Bit 3	Bit 2	Bit 1	Bit 0	Functions
0	0	0	0	Reads slave status
0	0	0	1	Undefined (for future expansion)
0	0	1	0	Reads and locks the slave status
0	0	1	1	Reads and locks data
0	1	0	0	Reads lock address (least significant 8 bits)
0	1	0	1	Reads lock address (most significant 4 bits)*
0	1	1	0	Release of slave status reading and lock
0	1	1	1	Release of data read and lock
1	0	0	0	Memory address write lock
1	0	0	1	Undefined (for future expansion)
1	0	1	0	Command write lock
1	0	1	1	Data write lock
1	1	0	0	Undefined (for future expansion)
1	1	0	1	Undefined (for future expansion)
1	1	1	0	Command write and lock release
1	1	1	1	Data write and lock release

* The lock address is transmitted in 1-byte units (8 bits).
The most significant 4 bits are as indicated below.

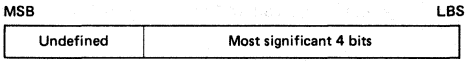


A unit that has been locked by another unit acting as a master unit will not output an acknowledge bit acting as a slave unit if the values of the control bits received from units other than the one that requested the lock are not those listed in the following table. However, the unit will output an acknowledge bit, operating as a slave unit, in response to the control bit it received from the master unit requesting the lock.

Table 1-3 Control Fields for Locked Slave Units

Bit 3	Bit 2	Bit 1	Bit 0	Functions
0	0	0	0	Reading of slave status
0	1	0	0	Reading of lock address (least significant 8 bits)
0	1	0	1	Reading of lock address (most significant 4 bits)*

* The lock address is transmitted in 1-byte units (8 bits).
As a result, the most significant 4 bits are as indicated below.



(6) The data fields

The data fields are the fields in which data is read from and written to the slave units. That is, the master unit uses the data fields to write data to the slave units and read data from the slave units. The data field is composed of 11 bits, 8 data bits, an end of data (EOD) bit, a partiy bit and an acknowledge bit. The data bits are 8 bits that are output from the most significant bits. The EOD bit is output right after the data bits. Behind the EOD bit, the parity bit and the acknowledge bit are output from both the master unit and the slave unit. The processing of the parity bit and the acknowledge bit will differ depending on whether it is during the write operation or during the read operation of the master unit.

① Writing from the master unit to the slave unit

When writing from the master unit to the slave unit, the master unit transmits data bits, an EOD bit and a parity bit to the slave unit. The slave unit receives the data bits, EOD bit and parity bit. If the parity is odd parity, it will send an acknowledge signal. If parity is even, the slave unit will reject the corresponding data and EOD bits and not output an acknowledge signal.

If an acknowledge signal is not output by the slave unit, the master unit will once again output to the slave unit the same data bits and EOD bit. This operation will continue until an acknowledge signal is detected from the slave unit or until the data reaches it maximum transmittable number of bytes. The master unit will transmit the next data if the parity is odd and an acknowledge signal has not been detected from the slave unit, and if the data has not been written somewhere nor exceeded the maximum transmittable number of bytes. The EOD bit will be transmitted from the master unit.

If the master unit still has data to be transmitted and the transmit data is less than the maximum transmittable bytes per frame, the EOD bit will be 1. If the master has no data to be transmitted or if the number of bytes in the data transmitted is equivalent to the maximum transmittable bytes per frame, the EOD bit will be 0.

② Reading the slave unit from the master unit

When the master unit reads the slave unit, the master unit will output a synchronous signal that corresponds to all of the bits to be read. The slave unit will check the content of the data, parity and EOD bits in response to the synchronous signal from the master unit and output them to the bus. The master unit will read the data, parity and EOD bits that are output by the slave unit to check parity. If the parity is even, the master unit will reject the data and EOD bits. The master unit will repeat the read operation if the data is within the maximum transmittable bytes per frame. It will continue to repeat this operation until the data and EOD bits are accepted or until the maximum transmittable bytes per frame has been exceeded. In the case of odd parity, the master unit will accept the data and EOD bits. If the EOD bit is 1 and the data is within the maximum transmittable bytes per frame, the master unit will go on to read the next data.

(7) The end of data (EOD) bit

The EOD bit is a signal that identifies whether the transmitted data is the final data of the message or not. The EOD bit is used to indicate the end of a transmission that has an optional amount of data that is within the maximum permissible bytes per frame. When the EOD bit is 0, it indicates that the data is the last data of that frame. When the EOD bit is 1, it indicates that the data is not yet at the end of the frame.

(8) The parity bit

The parity bit is used to confirm that there are no errors in the data. A parity bit is added to master address bits, slave address bits, control bits, data bits and the EOD bit. Odd parity is used. If the number of 1 bits within the data is even, the parity bit will be at 1. If the number of 1 bits within the data is even, the parity bit will be at 0.

(9) The acknowledge bits

There are three types of acknowledge bits, the one at the end of the slave address, the one at the end of the control field and the one at the end of the data field. The status of the acknowledge bit is defined as follows. If at 0, it indicates acknowledgement of the data (ACK). If at 1, it indicates that the data has not been acknowledged (NAK).

① The acknowledge bit at the end of the slave field

If the acknowledge bit at the end of the slave field satisfies any of the following conditions, it will not acknowledge the data and transmission will stop.

- Inaccurate parity in the master address bits or the slave address bits.
- A higher (faster) mode than the mode for the unit in question.
- Generation of a timing error.
- Nonexistence of a slave unit.

② The acknowledge bit at the end of the control field

If the acknowledge bit at the end of the control field satisfies any of the following conditions, it will not acknowledge the data and transmission will stop.

- Inaccurate control bit parity.
- If bit 3 of the control bits is at 1 (write) when the receive buffer is full.
- If the data buffer is empty and bit 3 of the control bits is at 0 (read) and the control bits are not set to read the slave status or the lock address.
- If the slave unit is locked by another master unit, except for a request to read the slave status or the lock address.
- If the master unit attempts to tranmit a memory address when the slave unit has no memory.
- If there is a lock address read request when the slave unit is not locked.
- If a timing error occurs.
- If an undefined bit meant for future expansion is used.

③ The acknowledge bit at the end of the data field

If the acknowledge bit at the end of the data field satisfies any of the following conditions, it will not acknowledge the data and transmission will stop. In such a case, if the transmitting side is within the maximum transmittable bytes per frame, the transmission of the data field will be executed again.

- If the parity of data bit and the EOD bit are inaccurate.
- If a timing error occurred from the point of previous acknowledge bit transmission or later.
- If the receiver buffer is full and unable to accept anymore data.

1.2.3 Transmit data

(1) The slave status

The master unit can determine why the slave unit did not return an acknowledge bit by reading the status of the slave unit. The status of the slave unit is determined by the results of the last communication conducted by the slave unit. All slave units are able of offer slave status information. The meanings of the slave statuses are shown in the table below.

Fig. 1-2 The Bit Configuration of Slave Unit Statuses

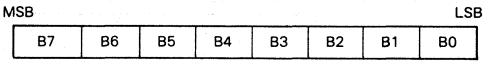


Table 1-4 Description of the Slave Unit Statuses

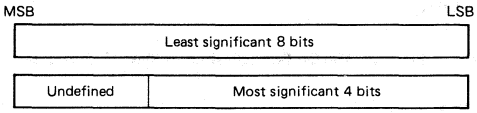
Bit	Value	Description of meanings	
B0*1	0	Slave transmit buffer empty	
	1	Slave transmit buffer is not empty	
B1*2	0	Slave receive buffer empty	
	1	Slave receive buffer is not empty	
B2	0	Unit is not locked	
	1	Unit is locked	
B3*3	0	Unit has no memory	
	1	Unit has memory	
B4*4	0	Slave transmission ended	
	1	Slave	
B5	0	Always 0	
B7, B6	00	Mode 0	Indicates the highest mode the unit will support.*4
	01	Mode 1	
	10	Mode 2	
	11	For future expansion	

*1: The slave transmit buffer is the buffer accessed during slave read processing.
*2: The slave receive buffer is the buffer accessed during slave write processing.
*3: The values of B3 and B4 can be set by an initialization command.
*4: The μPD6316 can support up to mode 3. Therefore, B6 and B7 are fixed at 0 and 1, respectively.

(2) Lock address

For reading a lock address, the address (12 bits) of the master unit that issued the lock command is read at the bit array shown below.

Fig. 1-3 Lock Address Configuration



(3) Memory addresses

If the slave unit receives memory address write control bits, processing will be executed in the following sequence:

- The slave transmit buffer bit showing the slave status will reset to 0 (slave transmit buffer empty).
- After the memory address has been set, data that corresponds to the address will be placed in the buffer at that memory address. (The host controller that controls the μPD6316 will place it there.)
- If data is already in the data buffer, the slave transmit buffer bit showing the slave status will set to 1 (slave transmit buffer is not empty).

A 4-byte slave transmit buffer is built in the μPD6316.

(4) Data

When the control bits read data, the data in the slave unit data buffer is read to the master unit. When the control bits write data, the data received by the slave unit is processed according to the operating specifications of the slave unit.

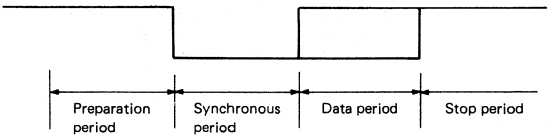
(5) The execution of lock and unlock

A slave unit that has received control bits specifying a lock (2H, 3H, 8H, AH and BH) will set the bit (B2) within the slave status byte that indicates lock to 1 when the first acknowledge bit in the data field is set to 0. A slave unit that has received control bits specifying the locked condition (6H, 7H, EH and FH) will reset the bit (B2) within the slave status byte to 0 when the first acknowledge bit in the data field is set to 1.

1.2.4 The bit format

The D2B interface bit format is shown in the diagram below.

Fig. 1-4 D2B Interface Bit Format

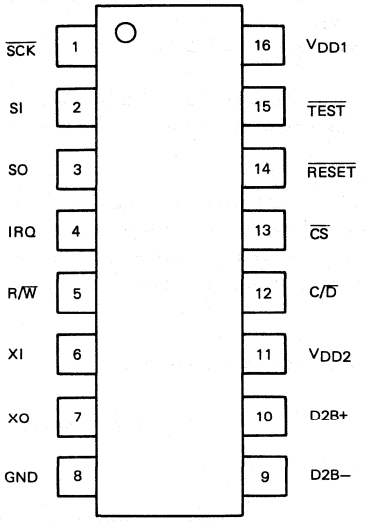


Preparation period	: The first high level period (logic level 1)
Synchronous period	: The next low level period (logic level 0)
Data period	: The period that expresses the bit value
Stop period	: The last high level period (logic level 1)

The specifications for total bit time and the periods allocated to the bits will vary according to the mode, the type of transmission bit and whether the unit is the master unit or the slave unit. The synchronous period and data period will be twice as long during arbitration. Master units involved in arbitration can use this extended period of time to ascertain the status of the bus.

2. PIN FUNCTIONS

2.1 Pin Layout



2.2 Description of Pin Functions

Pin number	Pin symbol	Pin function	Description	Input/ Output
1	$\overline{SCK}$	Serial clock input	Input pin for the serial clock used to interface with the microcomputer.	CMOS input
2	SI	Serial data input	Input pin for the serial data used to interface with the microcomputer.	CMOS input
3	SO	Serial data output	Output pin for the serial data used to interface with the microcomputer	CMOS output
4	IRQ		The output pin used by interrupt request signals generated by the communications and command execution results. Used for the operation start request signal to the microcomputer. The interrupt request output time is about 10 microseconds.	CMOS output
5	R/$\overline{W}$	Read/write switching input pin	The serial interface read/write mode switching input pin. When at the high level, it is in the read mode. When at the low level, it is in the write mode. By putting this pin at the low level and fixing the C/D pin at the high level, switching between the read and write modes is possible with the command input from the serial interface.	CMOS input
6 7	XI XO	System clock vibrator connection pin	Connection pin for the system clock vibrator. Use a 12 MHz liquid crystal vibrator or a ceramic vibrator. Also, the oscillating accuracy should be within ±0.5 %.	CMOS input
8	GND	Grounding pin	The grounding pin	
9 10	D2B− D2B+	D2B interface pin	Pin that connects to the D2B interface	
11	V_{DD2}	D2B interface positive voltage supply pin	D2B interface bus driver positive voltage pin. Connect to V_{DD1}.	
12	C/$\overline{D}$	Command/data switching pin	The pin used to switch between processing data input from the serial interface as commands or data. At the high level, data is processed as commands; at the low level data is processed as data. Switching between the read and write modes is possible through commands input from the serial interface by setting this pin at the high level and fixing the R/$\overline{W}$ pin to the low level.	CMOS input

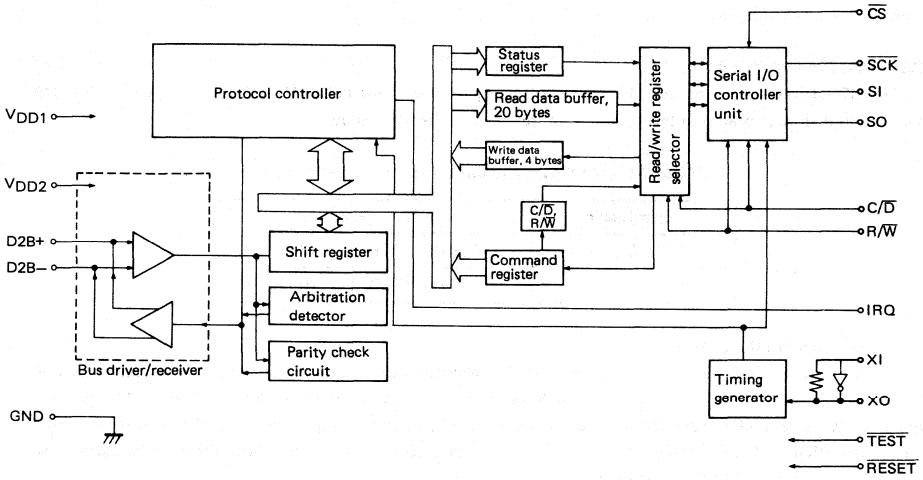
Pin number	Pin symbol	Pin function	Description	Input/ Output
13	$\overline{CS}$	Chip select pin	At the low level, serial interface input is effective. At the high level, serial clock interface input ($\overline{SCK}$) is ineffective and high impedance is put on the SO pin. The serial clock counter also resets. The status of the $\overline{CS}$ pin is not influenced by D2B interface transmit and receive operations.	CMOS input
14	$\overline{RESET}$	Reset input pin	The system reset signal input pin. At low level input, it resets. After turning on the power, always input the low level one time. During normal usage, input the high level.	CMOS input
15	$\overline{TEST}$	Test pin	Connect this pin to the V_{DD1} pin.	CMOS input
16	V_{DD1}	Positive voltage pin	The positive voltage pin. Use 5 volts ±5 %.	

3. INTERNAL CONFIGURATION

The μPD6316 is composed of the following three blocks:

(1) Data link layer controller
(2) Physical Layer controller
(3) Host interface controller

Fig. 3-1 μPD6316 Internal Blocks



3.1 Data Link Layer Controller

The data link layer controller generates a return code that gives the status of the processing of the D2B protocol data link layer (frame composition and resolution, communication error detection, etc.) and a return code that gives the execution status of communication commands established by the host controller and the status of communications to the host controller.

3.2 Physical Layer Controller

The physical layer controller generates bit timing and resolution as well as converts the signals between bus lines through the driver/receiver.

3.3 D2B Driver/Receiver

The D2B driver/receiver converts between the logic signals within the μPD6316 and the D2B signals. The D2B signals and their relationship to the logic statuses are shown in the table below.

Table 3-1 D2B Signals and Correlation to Logical Statuses

Logical static	D2B bus signals
0	(D2B+) − (D2B−) $\geqq$ 120 mV
1	(D2B+) − (D2B−) $\leqq$ 20 mV

3.4 Host Interface Controller

The host interface controller is a block that controls the transmission and reception of data with the host controller. It accepts communications control commands, passes on return codes and forwards transmit data. The forwarding of transmit data takes place through the FIFO buffers, 4 bytes of write data buffer (WDB) and 20 bytes of read data buffer (RDB). It also absorbs the differences between the D2B transmission speed and the serial interface transmission speed with μPD6316 host controller.

4. INTERFACING WITH THE HOST CONTROLLER

The section will explain the interfacing that occurs between the μPD6316 and the host controller.

4.1 Accessible Buffers and Register from the Host Controller

The host controller, which controls the μPD6316, can access the write data buffer (WDB), the read data buffer (RDB), the command register (CMR) and the status register (STR) within the μPD6316.

4.1.1 The write data buffer (WDB)

The write data buffer is a 4 byte FIFO buffer where the host controller transmit data and the parameters of the communications control commands are written.

4.1.2 The read data buffer (RDB)

The read data buffer is a 20 byte buffer for storing the receive data of the data link layer controller, which is located within the μPD6316. The host controller reads the μPD6316 received data from the read data buffer.

4.1.3 Command register (CMR)

The command register is an 8-bit register for writing control commands for the μPD6316. As indicated in Table 4-1, the host controller establishes the reset mode for the most significant 4 bits and establishes the host interface mode. It also establishes the command codes of the communications control commands for least significant 4 bits.

Table 4-1 Content of Command Register

Bit	Value	Description	
B7	1	Entering the reset mode.	
	0	Exiting the reset mode.	
B6	1	Data of least significant command register 4 bits is valid.	
	0	Data of least significant command register 4 bits is not valid.	
B5, B4	00	Change between mode through pin control	Switches the host interface modes.
	01	Data write mode	
	10	Data read mode	
	11	Status read mode	
B3 B2 B1 B0		Sets the communications control codes.	

4.1.4 The status register

The status register is an 8-bit register for determining the status of the μPD6316. The statuses of the write data buffer and the read data buffer and the status of interrupts can be read from the most significant 4 bits. The return code, which indicates results of communications, can be read from the least significant 4 bits.

Table 4-2 Content of Status Register

Bit	Value	Meaning	Description
B7	1	Write data buffer full	Tells if data can be written to data buffer.
	0	Write data buffer not full	
B6	1	Read data buffer is empty	Tells if data can be read from the read data buffer.
	0	Read data buffer is not empty	
B5	1	Write data buffer is empty	Tells if data is in the write data buffer.
	0	Write data buffer is not empty	
B4	1	Interrupt requested	Tells if interrupt is being requested.
	0	Interrupt not requested	
B3 B2 B1 B0		Return code	Return code will be read.

4.2 Host Controller Interface Modes

The host controller can access the write data buffer, read data buffer, command register and status register within the μPD6316 through the three-wire serial interface ($\overline{SCK}$, SI, SO). There are four modes for accessing the serial interface, as indicated in the table below. For switching between these four host interface modes there are two methods. In one method switching takes place by using the C/$\overline{D}$ pin and the R/$\overline{W}$ pin. In the other method switching takes place by writing data to the command register (soft error control).

Table 4-3 Host Interface Modes

Mode	Operation
Data write mode	At the rise of the serial clock, which is input through the $\overline{SCK}$ pin, the data at the SI pin will be placed into the write data buffer from the most significant bits. At the eighth serial clock, the placement of the data will be complete.
Data read mode	At the fall of the serial clock, which is input through the $\overline{SCK}$ pin, the read data buffer data at the SO pin will be output from the most significant bits. By inputting the serial clock eight times, the reading of the data will be complete. At this time, the data at the SI pin will be ignored.
Command write mode	At the rise of the serial clock, which is input through the $\overline{SCK}$ pin, the data at the SI pin will be taken from the command register's most significant bits. At the eighth serial clock, the placement of the data will be complete.
Status read mode	At the fall of the serial clock, which is input through the $\overline{SCK}$ pin, the status register data at the SO pin will be output from the most significant bits. By inputting the serial clock eight times, the reading of the data will be complete. At this time, the data at the SI pin will be ignored.

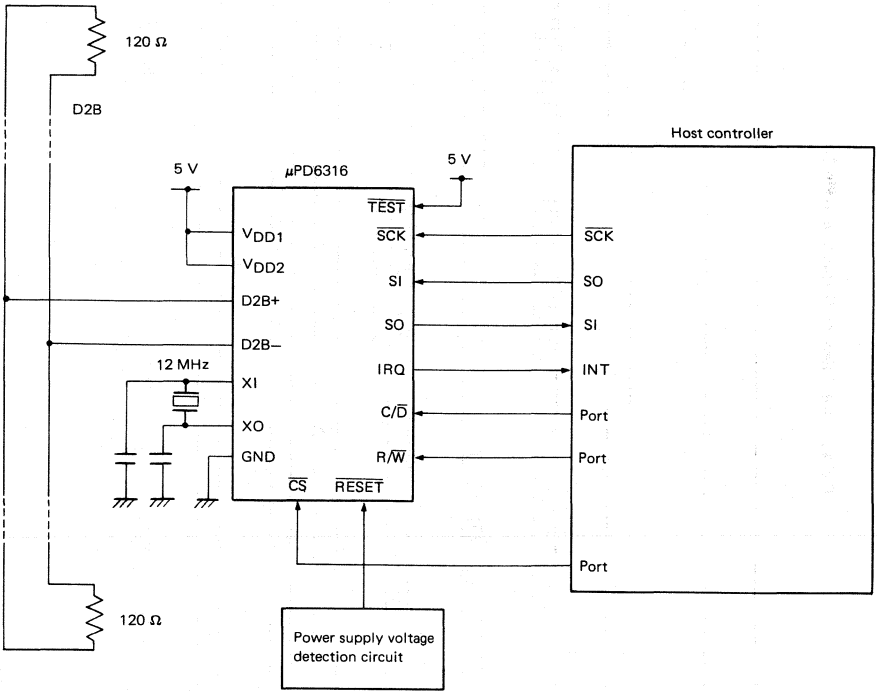
4.2.1 Switching through pin control

With B5 and B4 of the command register both at 0, the host interface mode can be switched by setting the C/$\overline{D}$ pin and the R/$\overline{W}$ pin at the values indicated in Table 4-4.

Tabel 4-4 Switching Host Interface Modes Through Pin Control

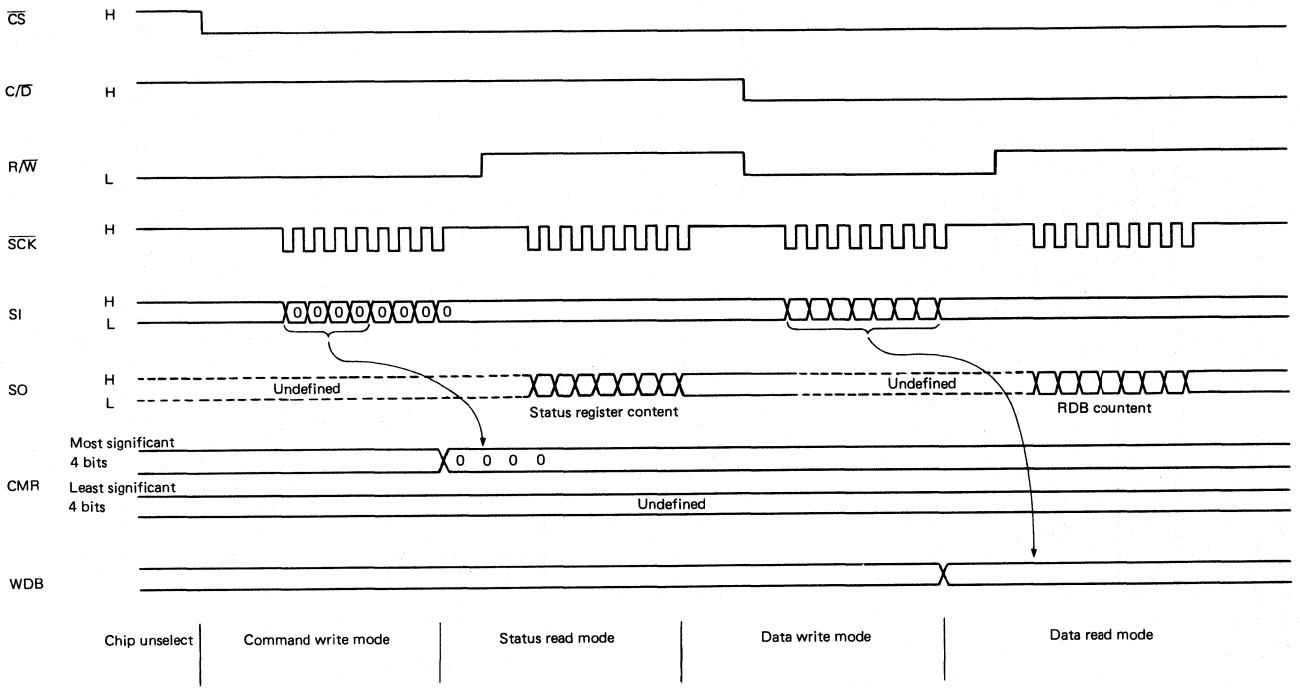
C/$\overline{D}$	R/$\overline{W}$	Host interface mode
0	0	Data write mode
0	1	Data read mode
1	0	Command write mode
1	1	Status read mode

Fig. 4-1 Host Controller Connections Due to Pin Control



Note: If the power supply voltage moves out of the 5 V ±5 % range, the Not Reset pin must be placed at the low level for 6 microseconds or more in order to reset the μPD6316.

Fig. 4-2 Host Interface Timing Due to Pin Control



4.2.2 Switching through software control

With the C/$\overline{D}$ pin at the high level and the R/$\overline{W}$ pin at the low level, the host interface mode can be switched by setting B5 and B4 of the command register at the values indicated in Table 4-5.

Table 4-5 Switching Host Interface Modes Through Software Control

B5	B4	Host interface mode
0	0	Mode switching for pin control
0	1	Data write mode
1	0	Data read mode
1	1	Status read mode

After one byte of data has been forwarded, the host interface mode will become the command write mode, which is controlled by the C/$\overline{D}$ and R/$\overline{W}$ pins.

Fig. 4-3 Host Controller Connections Due to Software Control

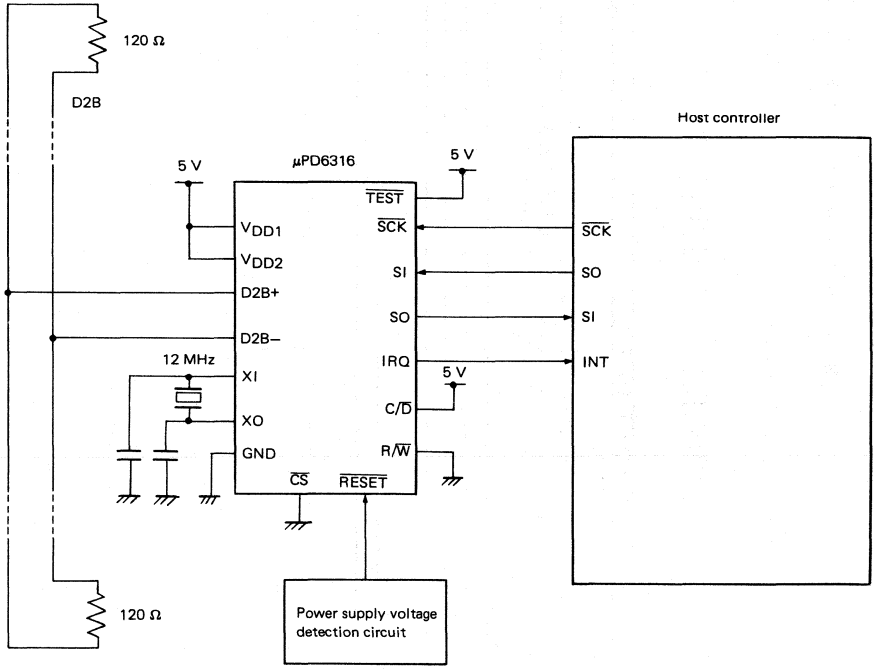
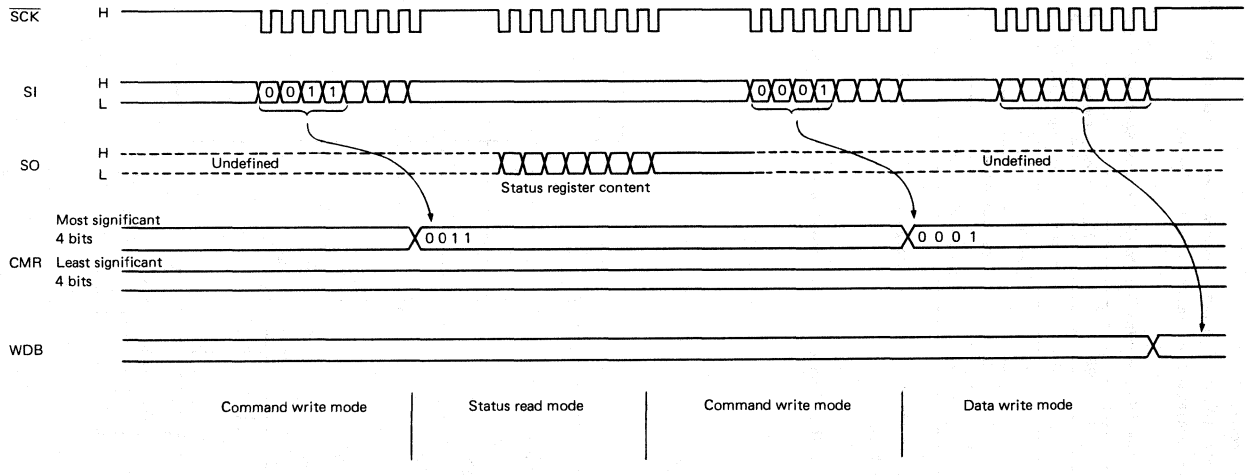


Fig. 4-4 Host Interface Timing Due to Software Control

Fix C/$\overline{D}$ pin to V_{DD} and R/$\overline{W}$ pin to ground.



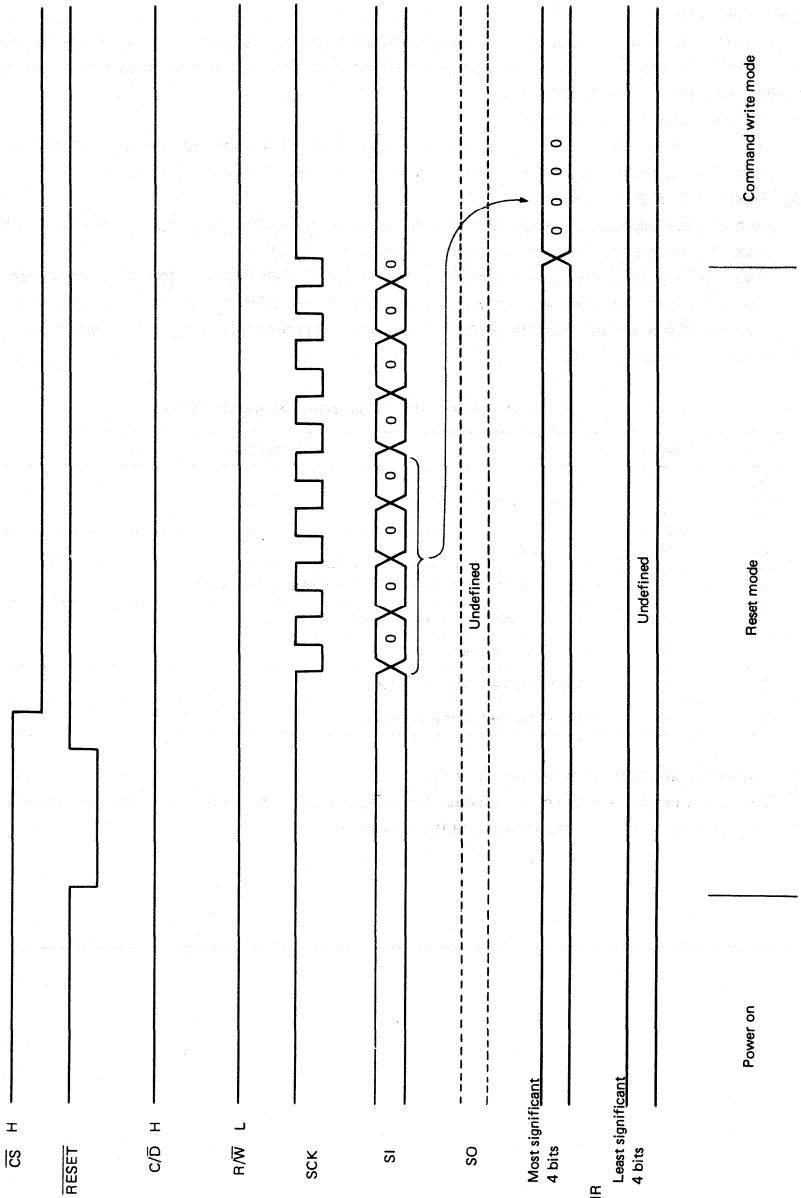


Fig. 4-5 Example of not Reset Control at Power on

4.3 The Rset Mode

If the Not Reset pin is set at the low level, the μPD6316 goes to the reset mode. To cancel the reset mode the Not Reset pin has to be set at the high level and a reset cancellation command has to be input. The follwoing two methods are used to reset the μPD6316.

(1) Resetting with the not reset pin

If the Not Reset pin is set at the low level, the μPD6316 will enter the reset mode. To get out of the reset mode, the Not Reset pin is set at high and bit B7 in the command register is set to 0.

(2) Resetting through the software

With the Not Reset pin fixed at the high level and bit B7 of the command register set at 1, the μPD6316 will enter the reset mode. To get out of the reset mode, set bit B7 to 0.

When turning the power on, it is necessary always to set the Not Reset pin to the low level once to establish the reset mode. In addition, at power shutoff, place the μPD6316 in the reset mode in order to keep noise from the D2B bus. The μPD6316 will be in the following condition after canceling the reset mode.

① D2B slave status initialized.

Table 4-6 Slave Status Values after Leaving Reset Mode

Bit	Value	Description
B7	1	Up to mode 2 is supported.
B6	0	
B5	0	Always 0
B4	0	The slave transmission section has stopped operating.
B3	0	Memory address has been allocated.
B2	0	Unit is not locked.
B1	0	Slave receive buffer is empty.
B0	0	Slave transmit buffer is empty.

② The address of the unit has been set to FFFH.

③ The option functions (message continuation function, group receive function) have not been specified.

④ The write data buffer and the read data buffer are empty.

5. COMMUNICATIONS CONTROL COMMANDS

The operating conditions of the μPD6316 can be specified by giving a command to it from the host controller. The communications control command is composed of a 4-bit command code and multiple-byte control parameters. The procedures for issuing a communications command are as follows:

① Read the status register to confirm that the write data buffer is empty.
② Write the command parameters to the write data buffer in the data write mode.
③ Write the command code to the least significant 4 bits of the command register in the command write mode.

Communications commands are executed during periods when communications are not taking place (the start bit monitor status). It can be determined if a specified communications command has executed by reading the status register and by determining if the write data buffer is empty. In addition, in the case of a GETLOCK command, a return code will be placed in the least significant 4 bits of the status register and an interrupt request will be returned from the μPD6316 after the command has been executed.

5.1 Overview of Communications Control Commands

Table 5-1 Overview of Communication Control Commands

Command name	Description
INIT (Initialize)	Sets local address and initializes.
SETSA (Set slave address)	Sets the slave address.
MREQ1 (Master request 1)	Communicates as a master unit.
MREQ2 (Master request 2)	Continues in previous condition as the master unit.
ABORT (Abort)	Aborts communications.
SETSD (Set slave data)	The slave unit places transmit data into the master unit.
GETLOCK (Get lock condition)	Check of whether or not lock by another unit.
SETOP (Set option)	Can use for an optional function.

Table 5-2 lists the communications control commands and the accompanying command codes and command parameters.

Table 5-2 Communication Commands and Accompanying Command Codes and Parameters

Command name	Least significant 4 bits of the command register	Command parameters (WDB)					
		First byte		Second byte		Third byte	Fourth byte
INIT	0000	Unit address (12 bits) MSB LSB		Status when a slave unit			
SETSA	0001	Slave address (12 bits) MSB LSB		Communications mode			
MREQ1	0010	Control bit	0000	Transmit data and bytes of the master*1		Transmit data and bytes of the master*1 (First byte)	Transmit data and bytes of the master*1 (Second byte)
MREQ2	0011						
ABORT	0100						
SETSD	0101	Number of slave transmit data bytes		Slave transmit data (first byte)		Slave transmit data (second byte)	Slave transmit data (third byte)
GETLOCK	0110						
SETOP	0111	Options	0000				

*1: Not required when bit 3 of the control bits has been set to 0.

Note: Even if the host controller mistakes the number of bytes of the command parameters, in the μPD6316 no error message will be returned and the command will be processed as though it were an accurate command. Please be aware of this.

5.2 Communications Control Command Functions

5.2.1 Initialization (INIT) command (Command code: 0H)

(1) Functions

① This command sets up the unit address (12 bits). The unit address will be used as a master address during transmission and a slave address during reception.

② The conditions of this command are set up during the slave unit time. It sets the conditions of bit B4 and B3 of the D2B slave status.

- It enables the operation and nonoperation (B4) of the slave transmission section. (It specifies the data transmission function for the master unit.)
- It establishes the allocation or nonallocation (B3) of a memory address. (It sets the allocation on nonallocation of the memory address for storing data to be transmitted to the master unit.)

Table 5-3 Setting Conditions for the Slave Unit

Slave transmitter	Memory address allocation	Command parameter value
Stop	None	0
Enabled	None	2
Enabled	Allocated	3

The unit address and slave unit conditions set up by the INIT command will remain at the specified values unless reset.

③ It initializes the slave status. The slave status is initialized as indicated in Table 5-4.

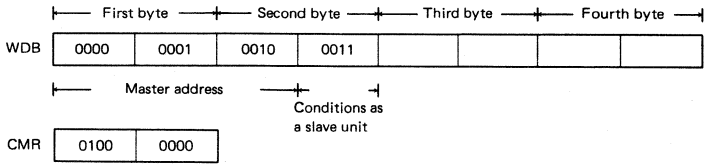
Table 5-4 Slave Statuses afte Executing the INIT Command

Bit	Value	Description
B2	0	Unit is not locked.
B1	0	Slave receive buffer empty.
B0	0	Slave transmit buffer is empty.

④ It clears the write data buffer after reading the 2-byte command parameters (the conditions of the master and slave addresses) from the write data buffer.

(2) Examples

The content of the write data buffer and the command register are as indicated below when the INIT command specifies that the master address is 012H and the slave data transmission section is operable and memory has been allocated.



5.2.2 SETSA command (Command code: 1H)

(1) Functions

① Sets up the slave address (12 bits)

② Sets up the communications mode (mode 0, mode 1, mode 2)

Table 5-5 Communications Mode and Settings

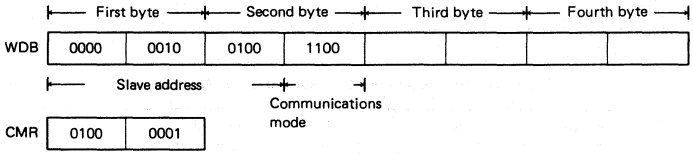
Communications mode	Value of command parameter
0	0H
1	8H
2	CH

The slave address and communications mode established by the SETSA command will remain at the specified values as long as a reset is not sent through the Not Reset pin. (Even in the case of a reset through the software, the slave address and communications mode will remain at the specified values.)

③ It will clear the write data buffer after the 2-byte command parameters (slave address and communications mode) have been read from the write data buffer.

(2) Examples

The content of the write data buffer and the command register are as indicated below when the INIT command specifies that the slave address is 024H and the communications mode is mode 2.



5.2.3 MREQ1 command (Command code: 2H)

(1) Functions

This command executes master communications (transmissions or receptions). After execution of the command, master unit communications will begin. As long as it does not lose at arbitration, the master unit will communicate with the slave unit at the slave address specified by the SETSA command.

① Sets up the control bits (4 bits)

② Sets up the number of transmit data bytes (8 bits, during transmission)

Table 5-6 Number of Transmit Data Bytes Settings

Number of transmit data bytes	Command parameter
1 byte	1H
2 bytes	2H
⋮	⋮
255 bytes	FFH
256 bytes	00H

Note: The maximum number of transmit data bytes will vary with the communications mode. If the transmission of the number of data bytes specified by the MREQ1 command does not finish within one frame, a communications error will be generated and communications will stop.

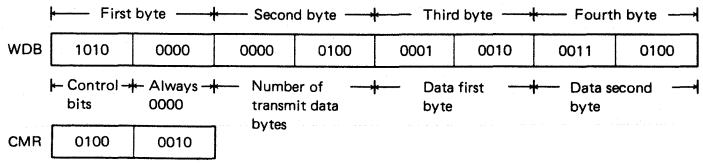
③ It establishes the transmit data (during transmission)

(2) Command execution conditions

The read data buffer must be empty. If the read data buffer receives data from another unit and a command is sent there while that data is still in the buffer, the MREQ1 command will be ignored and will not execute.

(3) Examples

The content of the write data buffer and the command register when the control bit is AH (command write and lock), when 4 bytes of data will be transmitted, and when the transmitted data will be placed at 12H, 34H, 56H and 78H by the MREQ1 command is as indicated below.



Note: Setup transmit data 56H and 78H when the above parameters are read and the write data buffer is empty.

5.2.4 MREQ2 command (Command code: 3H)

(1) Functions

The command re-executes a master communication (transmission or reception). If a master communication was stopped for the following reasons, this command will re-execute the command from the stopped condition.

① The generation of a master communications error.

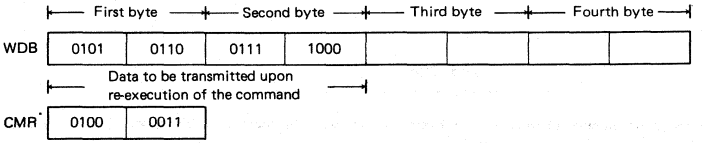
② The cancellation of a master communications command (MREQ1, MREQ2)

(2) Command execution conditions

The read data buffer must be empty. If the read data buffer receives data from another unit and a command is sent there while that data is still in the buffer, the MREQ2 command will be ignored. It will not execute.

(3) Examples

The content of the write data buffer and the command register are as indicated below when the MREQ2 command executes once again an MREQ1 commmand in a communications halted condition when generating a transmission timing error after the transmission of 2 bytes (12H and 23H) in mode 1.



The control bit and number of transmit data bytes can be the same as those for the previously specified MREQ1 command.

5.2.5 ABORT command (Command code: 4H)

(1) Functions

This command aborts master communications and slave unit transmissions.

① It resets a master request.

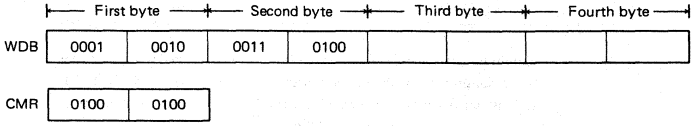
② It clears the data from the write data buffer.

③ It cancels slave transmit data.

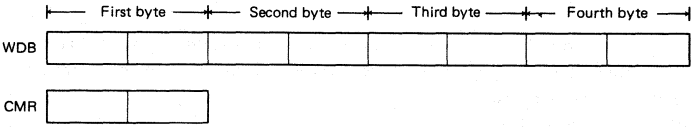
(2) Examples

The content of the write data buffer and the command register are as indicated below when the master unit begins communications as in the MREQ1 command example, generates a communications error and the 2 bytes of transmit data (12H, 34H) remaining in the write data buffer are canceled by the ABORT command.

Before execution of the ABORT command



After execution of the ABORT command



The data in the write data buffer will be cleared out.

5.2.6 SETSD command (Command code: 5H)

(1) Functions

This command specifies the data to be transmitted to the master unit when a data read and lock (control bit 3H) or a data read and cancel lock (control bit 7H) are received from the master unit.

① Specifies the number of transmit data bytes (8 bits).

Table 5-7 Number of Transmit Data Bytes

Number of transmit data bytes	Command parameter
1 byte	1H
2 bytes	2H
⋮	⋮
64 bytes	40H

Note: The maximum number of transmit data bytes will vary with the communications mode. If the transmission of the number of data bytes specified by the MREQ1 command does not finish transmitting within one frame, a communications error will be generated and communications will stop.

② Specifying transmit data

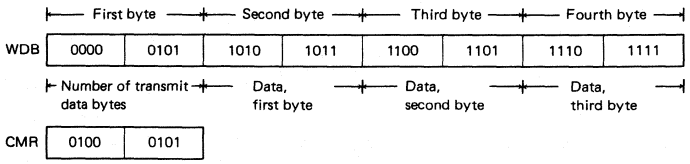
When the SETSD command is executed, the content of the command remains as is except in the following situations:

- If 1 byte or more of data is transmitted to the master unit and the communication ended.
- If a memory address write and lock (control bit 8H) are received from the master unit and the memory address is 1 byte or larger.
- When a reset takes place.

Note: If a slave transmission stop is specified by the INIT command, do not execute a SETSD command.

(2) Examples

The content of the write data buffer and the command register when the number of transmit data bytes is 5 bytes and when the transmit data will be placed at ABH, CDH, EFH, 14H and 25H by the SETSD command is as indicated below.



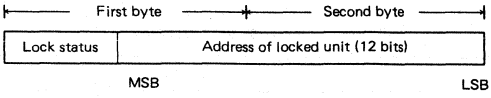
Note: Setup transmit data 14H and 25H when the above parameters are read and the write data buffer is empty.

5.2.7 GETLOCK command (Command code: 6H)

(1) Functions

① Places the slave unit lock status in the read data buffer.

② Places the address (12 bits) of a locked unit in the read data buffer. This data is meaningless when the slave unit is not locked.



When locked, the bit value is 1. When not locked, it is 0.

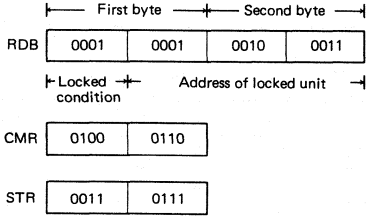
③ When the command execution (return code 7H) is placed in the least significant 4 bits of the status register, an interrupt generation request is issued at the same time.

(2) Command execution conditions

The read data buffer must be empty. If the read data buffer receives data from another unit and a command is sent there while that data is still in the buffer, the command will be ignored and will not execute.

(3) Examples

The content of the write data buffer and the command register are as indicated below when the address is the slave unit locked at 123H and the GETLOCK command is executed.



5.2.8 SETOP command (Command code: 7H)

(1) Functions

This command setup the optional functions, the group receive function and the message continuation function. When the SETOP command is not specified, these optional functions will be executed. For the content of these optional functions, refer to Section 7, Optional Functions. The values of the commands and parameters for specifying these optional functions are shown in Table 5-8 and 5-9.

Table 5-8 Commands and Parameters

Bit	Value	Functions
B7	1	No group receive in the locked condition.
	0	Group receive even if locked.
B6	1	Uses group receive function.
	0	Does not use group receive function.
B5	1	Uses message continuation function.
	0	Does not use message continuation function.
B4 B3 B2 B1 B0	0	Be sure to specify a 0.

Table 5-9 Optional Function Settings

Command/parameter (B7 to B0)	Group receive function	Message continuation function
00000000 (00H)	X	X
00100000 (20H)	X	○
01000000 (40H)	○	X
11000000 (C0H)	○	X

6. RETURN CODES

The μPD6316 places a return code in the least significant 4 bits of the status register and requests an interrupt. As a result of the interrupt, the host controller can determine the communications result by reading the return code in the status read mode.

6.1 Communication Execution Return Codes

Return codes generated as a result of the exectuion of communications between the master units and the slave units are given in the table below.

Table 6-1 Description of Return Codes

Return code name	Value	Description
Master receive start	0H	Indicates that the master unit has started receiving data, slave status and lock address from the slave unit.
Master receive end	1H	Indicates that the master unit received 1 frame of data, slave stutus and lock address from the slave unit without generating a communications error and the communication ended.
Slave receive start	2H	Indicates that slave unit has started to receive data, commands and memory address from the master unit.
Slave receive end	3H	Indicates that the slave unit received 1 byte or more of data, commands and memory address from the master unit.
Transmit end	6H	① Indicates that the master unit was able to transmit accurately the transmit data bytes of data, commands and memory address specified by the MREQ1 command. ② Indicates that the slave unit was able to transmit accurately the transmit data bytes specified by the SETSD command.

In addition, if the message continuation function or the group receive function have been specified by the SETOP command, return codes 4H and 5H will be specified as indicated in the following.

(1) Message continuation specified

Table 6-2 Return Codes when Message Continuation Function Specified

Return code name	Value	Description
Message continuation start	4H	Indicates that the message continuation condition has been established and the slave unit has started to receive the continuation of data and command messages from the master unit.
Message continuation end	5H	Indicates that the message continuation condition has been established and the slave unit has started to receive the continuation of 1 byte or more of data and command messages from the master unit.

(2) Group receive function specified

Table 6-3 Return Codes when Group Receive Function Specified

Return code name	Value	Description
Group receive start	4H	Indicates that the group receive condition has been established and the units which have the slave unit group address have started to receive data, commands and memory addresses from the master unit.
Group receive end	5H	Indicates that the group receive condition has been established and the units having the slave unit group address have received 1 byte or more of data, commands and memory address from the master unit and the communication ended.

6.2 Communications Error Return Codes

The returns codes generated when there is a communication error between the master unit and the salve unit are shown below.

(1) Slave unit communication error return codes

Table 6-4 Slave Unit Communication Error Return Codes

Return code name	Value	Description
Slave communication error	8H	Indicates that one of the following errors occurred during slave communication: ① Timing error was generated. ② During communication, the setup of transmit data in write data buffer did not occur in time.

(2) Master unit communication error return codes

Table 6-5 Master Unit Communication Error Return Codes

Return code name	Value	Description
Arbitration error	AH	Generates when three unsuccessful arbitrations occur.
Address error	BH	Generates in the slave address field when a not acknowledged signal comes from the slave unit.
Control error	CH	Generates in the control field when a not acknowledged signal comes from the slave unit.
Data error	DH	① Generates when transmitting data, commands and memory address and the number of transmit bytes of data, commands and memory address specified by the MREQ1 command could not be transmitted within the maximum transmittable bytes per frame. ② Generates when receiving data, slave status and lock address and the number of receive bytes of data, slave status and lock address that can be received within the maximum transmittable bytes per frame could not be received.

Table 6-5 Master Unit Communication Error Return Codes (Cotn'd)

Return code name	Value	Description
Timing error	EH	Generates when a timing error occurs in any of the fields.
Buffer error	FH	① Generates when transmitting data, commands and memory address and when transmitting the setup of the transmit data for the write data buffer does not occur in time. ② Generates when receiving data, slave status and lock address and these cannot be received because the read data buffer is full.

6.3 Command Execution Return Codes

A command execution return code is returned when a GETLOCK command is executed.

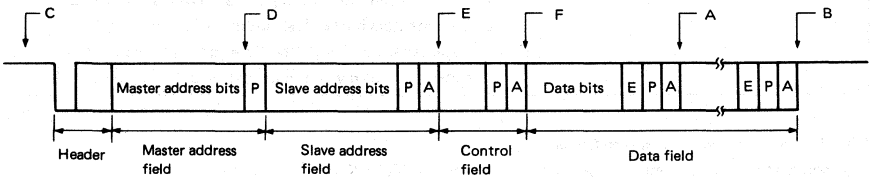
① Return code : 7, an interrupt request
② Condition for generation : read data buffer empty
③ Period of generation : during the start bit monitor period (Period in which the D2B signal is at the high level)

A return code is not returned for commands other than the GETLOCK command.

6.4 Return Code Generation Periods

Return codes are placed in the least significant 4 bits of the status register. Each time a new return code is generated, this location will be updated even if the register is not read.

Fig. 6-1 Return Code Generation Areas



Note: P = parity bit; A = acknowledge bit; E = end of data bit.

Table 6-6 Return Code Generation Areas

Return code name	Area	Description
Status receive start, slave receive start, message continuation start, group receive start	A	When the acknowledge bit first become 0 in a data field.
Master receive end, slave receive end, message continuation end, group receive end, transmit end	B	When transmitting the acknowledge bit of the last data in the data field.
Command execution	C	The start bit monitor period
Arbitration error	D	When receiving the master address of the master address field after three unsuccessful arbitration attempts
Address error	E	When the acknowledge bit is set at 1 in the slave address field.
Control error	F	When the acknowledge bit is set at 1 in the control field.

7. OPTIONAL FUNCTIONS

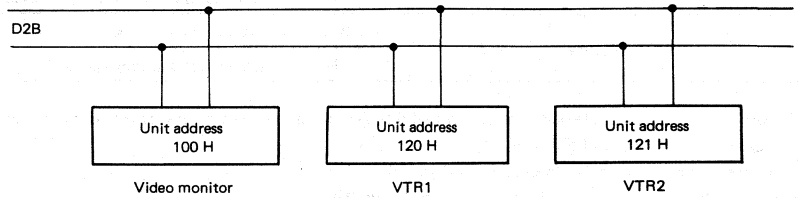
With the μPD6316, there are two types of optional functions, the message continuation function and the group receive function. These optional functions can be selected by using the SETOP command.

7.1 The Group Receive Function

This is a function in which the unit that has the group address of the slave address transmitted for the master unit monitors the content of the master and slave unit communications. However, if a slave address matches that of the unit, it will conduct normal reception as a slave unit.

* The group address indicates an address equivalent to the most significant 9 bits (service code, unit code) of a unit address (12 bits).

Example



If the video monitor becomes the master unit and communicates with VTR1 as a slave unit, VTR2 can use the group receive function to monitor the content of the communication between the video monitor and VTR1.

Note: A unit that conducts a group receive will not output an acknowledge bit to any of the fields.

7.1.1 Conditions for executing a group receive

(1) Data conditions transmitted from the master unit
- The group address portion of the slave address must match the group address of the unit concerned. However, if the unit address matches the slave address, the communication will be given priority as a slave unit.
- In addition, there must be a control bit (8H, AH, BH, EH, FH) from the master unit specifying the data, commands and memory address to the slave unit.

(2) Conditions for a unit to undertake a group receive
- The group receive function must be specified by the SETOP command.
- In addition, if the SETOP command parameter is COH, it must not have been locked by another unit. If the SETOP command is 80H, it does not matter if it has been locked by another unit.
- The read data buffer must be empty when an acknowledge signal is received in the control field.

7.2 The Message Continuation Function

To allow the slave unit to receive the data, command and memory address transmitted from the master unit, the read data buffer must be empty before these are received. When the slave unit has been locked by the master unit and the slave unit receives multiple frames of messages (data and commands), the message continuation function will allow the slave unit to receive from the second from onward even if the slave unit's read data buffer is not empty. By using this function, the read data buffer can be used efficiently. In addition, the slave unit can read slowly from the read data buffer the data and commands it has received.

7.2.1 Conditions for executing the message continuation function

(1) Conditions for a unit to conduct a message continuation

- The message continuation function must be specified by the SETOP command.
- In addition, the unit must be locked.

(2) Conditions concerning control bits sent from a locked master unit

The control bits currently received from a locked master unit and the control bits previous to that must meet the following conditions.

Table 7-1 Message Continuation Control Bit Conditions

Previously received control bits		Newly received control bits	
Value	Functions	Value	Functions
AH	Command write and lock	AH	Command write and lock
		EH	Command write and lock released
BH	Data write and lock	BH	Data write and lock
		FH	Data write and lock released

However, the previously received control bits in Table 7-1 above must not be any of the four indicated below.

- Slave status read (control field 0H)
- Slave status read and lock release (control field 2H)
- Lock address least significant 8 bits read (control field 4H)
- Lock address most significant 4 bits reas (control field 5H)

(3) Exceptions

A message will not continue regardless of whether the conditions of sections (1) and (2) above are both established, if the following data is placed in the read data buffer.

- If the unit conducting the message continuation executes a GETLOCK command.
- If the unit conducting the message continuation becomes a master unit and receives data, slave status and a lock address.

8. COMMUNICATING WITH THE HOST CONTROLLER

Here the flow of data between the μPD6316 and the host controller during communications will be explained.

8.1 Master Transmit

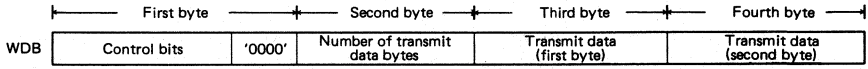
A master transmit is the communication data exchange that takes place when a unit becomes a master unit by specifying 8H, AH, BH, EH and FH as control bits, executing an MREQ1 or MREQ2 command, and then transmitting data, commands and memory addresses to slave units.

8.1.1 MREQ1 command master transmit

(1) The control bits, number of transmit data bytes and transmit data are placed in the write data buffer and an MREQ1 command (command code 2H) is executed.

(2) Transmission starts and when the data in the write data buffer is read, the remaining data is placed in the write data buffer and the specification of data amounting to the number of transmit data bytes is made.

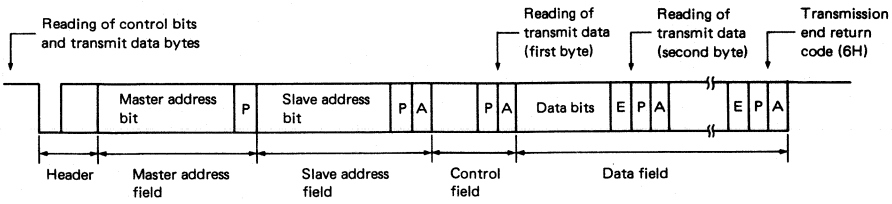
Fig. 8-1 Data Exchange During Master Transmissions



(3) If a transmit data byte amount of data, commands and memory addresses is transmitted accurately, a transmission end return code will be placed in the status register and an interrupt request will be generated.

(4) If an error occurs and data transmission ends, a communication error return code will be placed in the status register and an interrupt signal will be generated. (The return code is that discussed in Section 6.2 (2).) Fig. 8-2 and Table 8-1 show the timings at which the μPD6316 reads command parameters and transmit data from the write data buffer.

Fig. 8-2 Command Parameter and Transmit Data Read Timings



Note: P = parity bit; A = acknowledge bit; E = end of data bit

Table 8-1 Areas where Command Parameters and Transmit Data Read

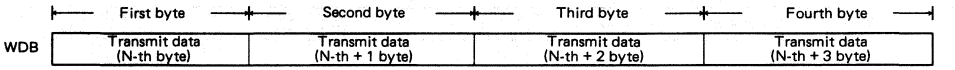
Parameter/communications data	Areas where write data buffer read
Control bits	When μPD6316 processes MREQ1 command (start bit in monitoring condition)
Number of transmit data bytes	
Transmit data (first byte)	When acknowledge bit received in the control field
Transmit data (second byte)	When first acknowledge bit read in the data field
Transmit data (n-th byte)	When the n-th acknowledge bit is read in the data field

8.1.2 MREQ2 command master transmit

If a an MREQ1 command is executed and a communications error occurs during the transmission of data, command and memory address and all data does not transmit, or if the MREQ1 or MREQ2 command is canceled, the MREQ2 command can be executed so that the remaining data is transmitted.

(1) The remaining data is placed in the write data buffer as command parameters, as indicated in Fig. 8-3, and the MREQ2 command (command code 3H) is executed.

Fig. 8-3 Data Handling During Master Transmission (Content of write data buffer)



The remaining operations are the same as those for the MREQ1 command as described in Section 8.1.1.

8.2 Slave Transmit

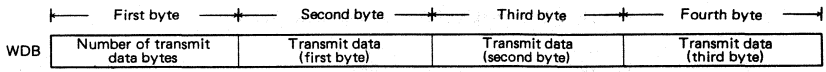
8.2.1 During data transmissions

When the slave unit receives control bits 3H or 7H from the master unit, it transmits data as indicated in the following:

(1) It places the number of transmit data bytes and the transmit data in the write data buffer as command parameters, as shown in Fig. 8-4, and executes an SETSD command (command code 5).

(2) When transmission starts and the data placed in the write data buffer is read from the buffer, it places the remaining data in the write data buffer and sets up an amount of data equivalent to the number of transmission bytes.

Fig. 8-4 Handling of Slave Transmit Data (Write data buffer content)



(3) If an amount of data equivalent to the number of transmit data bytes has been accurately transmitted, the transmission end code will be placed in the status register and an interrupt will be requested.

(4) If the transmission ends because of an error during transmission and all of the data is not transmitted, the slave communication error return code (8H) will be placed in the status register and an interrupt will be requested. At this time, an ABORT command will be executed and the transmit data remaining in the write data buffer will be cleared out. The times in which the μPD6316 will read the number of transmission data bytes and the transmit data from the write data buffer are as indicated below in Table 8-2.

Table 8-2 Reading of Transmit Data and Number of Bytes

Parameter/communications data	Areas where write data buffer read
Number of communication data bytes	μPD6316 processes SETSD command (start bit in monitor condition)
Transmit data (first byte)	When acknowledge bit transmitted in control field
Transmit data (second byte)	When first acknowledge bit received in data field
Transmit data (N-th byte)	When the N-th − 1 byte received in data field

8.2.2 Transmitting slave status and lock address

When the μPD6316 receives bits 0H, 2H, 4H, 5H and 6H as control bits from the master unit, the salve status and lock address are generated automatically and transmitted to the master unit. As a result, there is no necessity for the host controller to be involved in the transmission of the slave status and lock address.

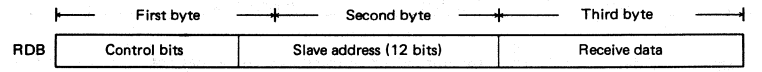
8.3 Master Receive

When a unit sets up bits 0H, 2H, 3H, 4H, 5H, 6H and 7H, executes an MREQ1 or an MREQ2 command, becomes a master unit and receives the data, slave status and lock address from the slave unit, the following will occur:

(1) When the 1 byte of data, slave status and lock address is received from the slave unit, the control bits, slave address and transmit data specified by the MREQ1 command will be placed in the read data buffer. In addition, the master reception end return code (1H) will be placed in the status register and an interrupt will be generated.

However, if the first byte of data is the end data (EOD = 0), the master reception end return code (1H) will be placed in the status register, not the master reception start return code, and an interrupt request will be generated.

Fig. 8-5 Handling of Data During Master Receive



(2) Receive data is placed in the read data buffer each time data is received.

(3) After one frame of end data is placed in the read data buffer, a master receive end return code (1H) is placed in the status register, generating an interrupt request.

(4) If an error occurs during reception and communication stops without receiving all of the data transmitted from the slave unit, a master communication error return code will be placed in the status register, generating an interupt request. The times when the μPD6316 will setup the receive data are as shown in Table 8-3 below.

Table 8-3 Placing Receive Data in Read Data Buffer

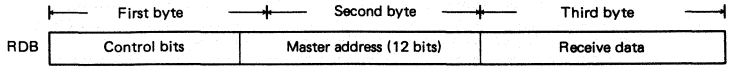
Parameter/communications data	Areas where write data buffer read
Control bits	When the master receive start return code generated (When receive data is 2 bytes or more)
Slave address	When the master receive end return code generated (When receive data is 1 byte)
Receive data (first byte)	When first acknowledge bit received in data field
Receive data (second byte)	When second acknowledge bit received in data field
Receive data (N-th byte)	When the N-th acknowledge bit received in data field

8.4 Slave Receive

If the slave unit receives either of the 8H, AH, BH, EH, or FH bits as a control bit from the master unit and also receives data, commands and a memory address, the following will occur:

(1) When it receives 1 byte of data composed of data, a command and a memory address, the control bits, master address and receive data will be placed in the read data buffer from the master unit. In addition, a slave receive start return code (2H) will be placed in the status register to generate an interrupt request. However, if the one byte of data is end data (EOD = 0), the slave receive end return code (3H), not the slave receive start return code, will be placed in the status register to generate an interrupt request.

Fig. 8-6 Handling of Data During Slave Receive



(2) Receive data is placed in the read data buffer each time data is received.

(3) After one frame of end data is placed in the read data buffer, or if a communication error is generated and one frame of communications ends, a slave receive end return code (3H) will be placed in the status register, generating an interrupt request. The times when the μPD6316 will place data in the receive data are as shown in Table 8-4 below.

Table 8-4 Placing Receive Data Read Data Buffer

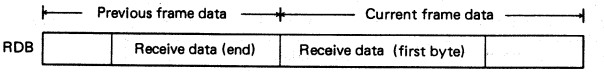
Parameter/communications data	Areas where write data buffer read
Control bits	When the slave receive start return code is generated (When receive data is 2 bytes or more)
Master address	When the slave receive end return code is generated (When receive data is 1 byte)
Receive data (first byte)	When first acknowledge bit received in data field
Receive data (second byte)	When second acknowledge bit received in data field
Receive data (N-th byte)	When the N-th acknowledge bit received in data field

8.5 The Message Continuation Function

If the message continuation coditions have been met and the remaining data and commands are to be received from the master unit, the following will take place:

(1) When the first byte of data and commands are received from the master unit, the receive data will be placed in the read data buffer, as indicated in Fig. 8-7, and a message continuation return code (4H) will be placed in the status register, generating an interrupt request. However, if the first byte of data is end data (EOD=0), a message continuation end return code (5H) will be placed in the status register, instead of a message continuation start return, and an interrupt request will be generated.

Fig. 8-7 Handling of Message Continuation Data



Data and commands can still be received during message continuation even if the read data buffer is not empty. In such a case, the first byte of the current data frame is placed after the end data received in the previous frame.

(2) Receive data will be placed in the read data buffer each time it is received.

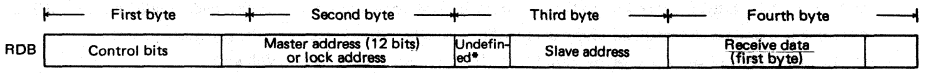
(3) After one frame of end data has been placed in the read data buffer, or if a communication error is generated and one frame of communication ended, a message continuation end return code (5H) will be placed in the read data buffer and an interrupt request generated. The times when the μPD6316 places received data in the read data buffer are the same as those for slave data.

8.6 Group Receive

If the group receive conditions have been established and a unit which has the group address of a slave address receives data, commands and memory addresses from the master unit, the following will take place:

(1) When the first byte of data, commands and memory addresses are received from the master unit, the least significant four bits of the control bits, master address and slave address and the receive data will be placed in the read data buffer, as indicated in Fig. 8-8, and a group receive start return code (4H) will be placed in the status register, generating an interrupt request. However, if the first byte of data is end data (EOD = 0), a group receive end return code (5H) will be placed in the status register, instead of a group receive start return code, and an interrupt request will be generated.

Fig. 8-8 Handling of Group Receive Data (Read data buffer content)



* The most significant 4 bits of the third byte of the read data buffer will become undefined.

(2) Receive data will be placed in the read data buffer each time one byte is received.

(3) After one frame of end data has been placed in the read data buffer, or if a communication error was generated and one frame of communication ended, a group receive end return code (5H) will be placed in the read data buffer and an interrupt request generated. The times when the μPD6316 places received data in the read data buffer are the same as those for slave data.

9. HOST CONTROLLER PROCESSING

9.1 Host Controller Responses During Interrupts

The return code is placed in the least significant 4 bits of the status register and an interrupt is requested of the host controller. The host controller should respond to interrupt requests in the sequence indicated in the following:

(1) Interrupts from the μPD6316 are prohibited.
(2) The return code is read.
(3) Interrupts from the μPD6316 are permitted.
(4) The cause of the interrupt is processed.

Processing to respond to the return code read at step (2) will take place. If the return gives notification of a receive start or end, the following processing will take place:

- If the return code notifies of a receive start (codes 0H, 2H, 4H), the data placed in the read data buffer and the content of the status register are read and a check is done for a receive end return code (codes 1H, 3H, 5H). If a receive end code is detected, all of the data in the read data buffer is read and the processing ends.
- If the return code notifies of a receive end (codes 1H, 3H, 5H), the processing will end.
  - Mode 0: about 5.5 ms
  - Mode 1: about 1.5 ms
  - Mode 2: about 1.0 ms

9.2 Flags Used in the Process Flow

During process flow, various flags are used in the host controller for controlling the μPD6316. These flags have been allocated to the RAM resident in the host controller. (See Fig. 9-1 and 9-2)

Fig. 9-1 Example of μPD6316 Control Flag Allocation

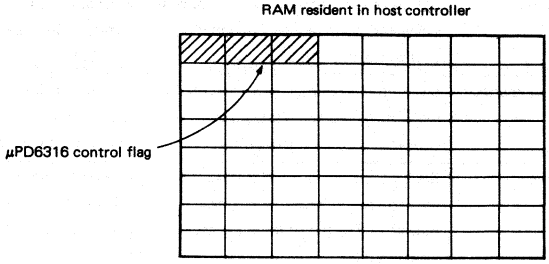
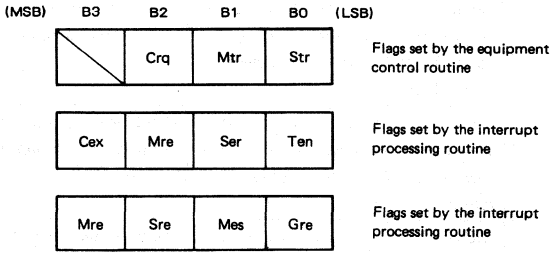


Fig. 9-2 Example of process flow flag; position of μPD6316 control flag bits



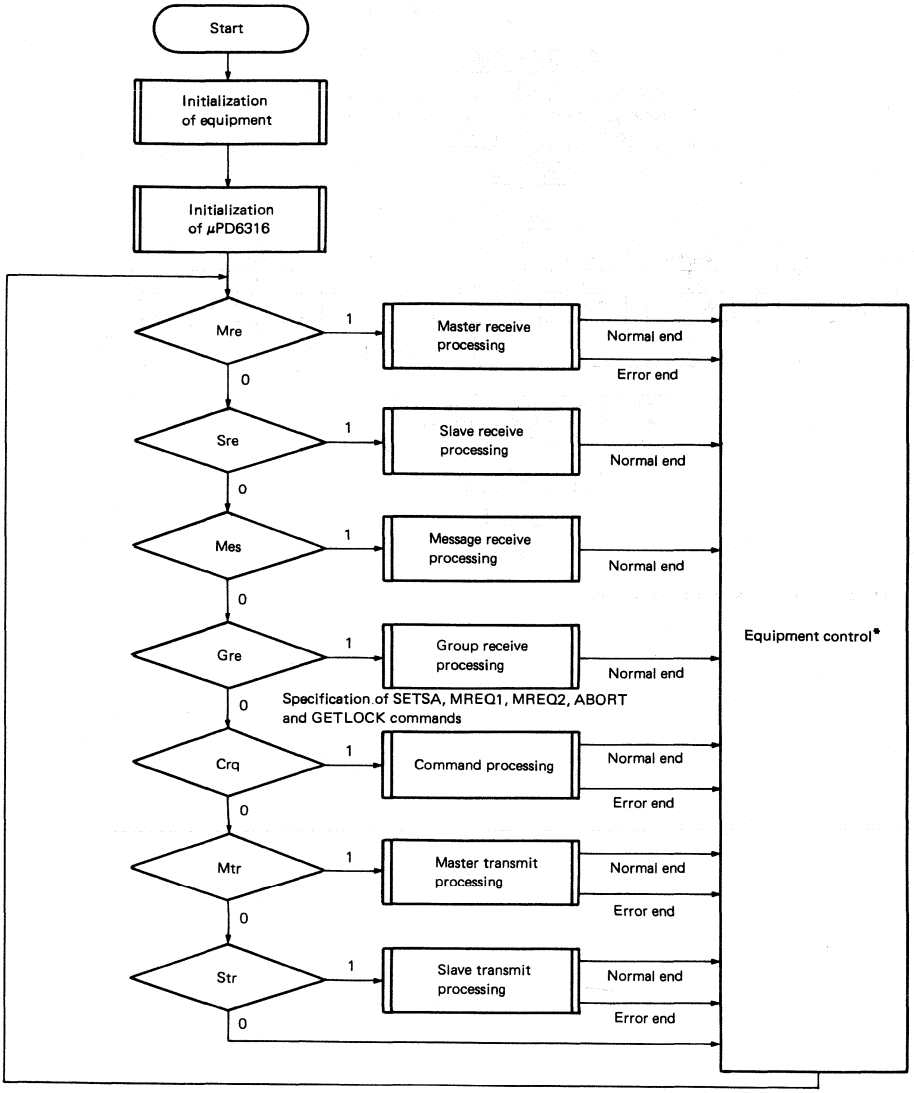
Descriptions of the intentions of these flags are shown in Table 9-1.

Table 9-1 Flag Descriptions

Flag name	Purpose	Setting conditions	Resetting conditions
Crq	Command request	Set by the equipment control routine when the μPD6316 requests a communication command execution.	Reset by the command routine when the normal processing of a μPD6316 communication command ends.
Mtr	Master transmit request	Set by the equipment control routine when there is a request by a master unit to transmit to a slave unit.	Reset by the master transmit request routine at the end of normal master transmit processing.
Str	Slave transmit request	Set by the equipment control routine when there is a request by a slave unit to transmit to a master unit.	Reset by the slave transmit request routine at the end of normal slave transmit processing.
Mre	Master receive start	Set by the interrupt processing routine when a return code starts a master receive (code 0H) or ends a master receive (1H).	Reset by the master receive routine at the end of normal master receive processing.
Sre	Slave receive start	Set by the interrupt processing routine when a return code starts a slave receive (code 2H) or ends a slave receive (3H).	Reset by the slave receive routine at the end of normal slave master receive processing.
Mes	Message continuation start	Set by the interrupt processing routine when a return code starts a message receive (code 4H) or ends a message receive (code 5H).	Reset by the message receive routine at the end of a message receive.
Gre	Group receive start	Set by the interrupt processing routine when a return code starts a group receive (code 2H) or ends a group receive (code 3H).	Reset by the group receive routine at the end of a group receive.
Ten	Transmit end	Set by the interrupt processing routine when a return code is a transmit end (code 6H).	Reset by the master/slave transmit routine at the end of normal processing.
Mer	Master error generated	Set by the interrupt processing routine when a return code is a master communications error (codes AH-FH).	Reset by the master communication error routine at the end of the error.
Ser	Slave error generated	Set by the interrupt processing routine when a return code is a slave communications error (codes 8H).	Reset by the slave communication error routine at the end of the error.
Gex	GETLOCK command execution successful	Set by the interrupt processing routine when a return code is the end of a GETLOCK command execution (code 7H).	Reset by the command routine at the end of the GETLOCK command processing.

9.3 Main Routine

This routine is the host controller main routine, which is used to control the μPD6316. Flags that control communications are set by means of the interrupt processing routines or the equipment control routines and the routines that correspond to the flags that are called up.

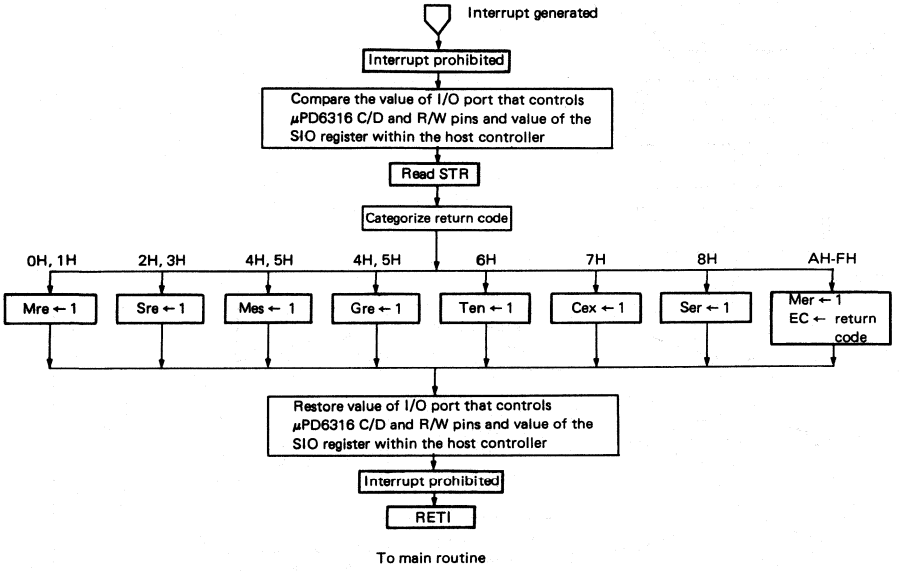


* The equipment routine is the routine that does the application processing of the host controller. In order to control the μPD6316, the following processing must take place:

- Setting of the Crq flag when there is a command request.
- Setting of the Mtr flag when there is a master transmit request.
- Setting of the Str flag when there is a slave transmit request.
- Error processing during master communications and slave transmit.

9.4 Interrupt Processing Routines

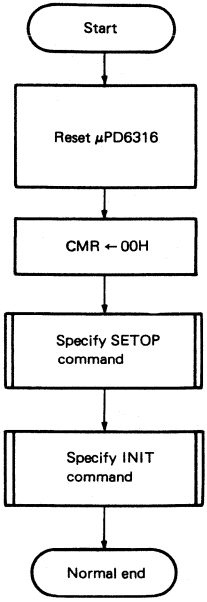
This routine operates when there is and interrupt request (IRO=H) from the μPD6316. It reads the content of the return codes and sets various flags in response.



EC: stores communication error return code

9.5 Other Routines

9.5.1 The μPD6316 initialization routine



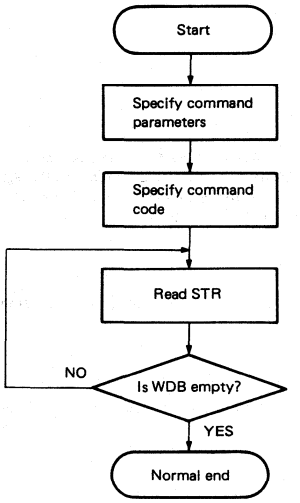
After being set at low for 6 microseconds, the host controller port which controls the μPD6316 Not Reset pin, is returned to the high level.
(However, this is not required if a reset is done with the hardware, such as a power on reset.)

Place 00H in the command register to cancel the reset mode.

To use the optional commands, the SETOP command has to be specified.

The INIT command is used to specify the unit address slave unit conditions.

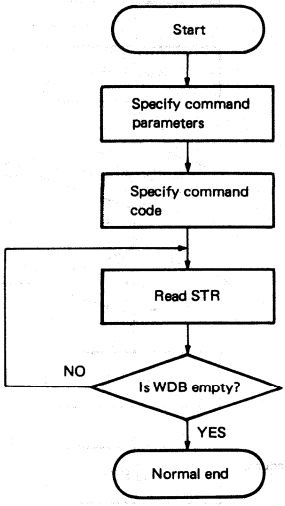
Setup flow of INIT and SETOP commands.



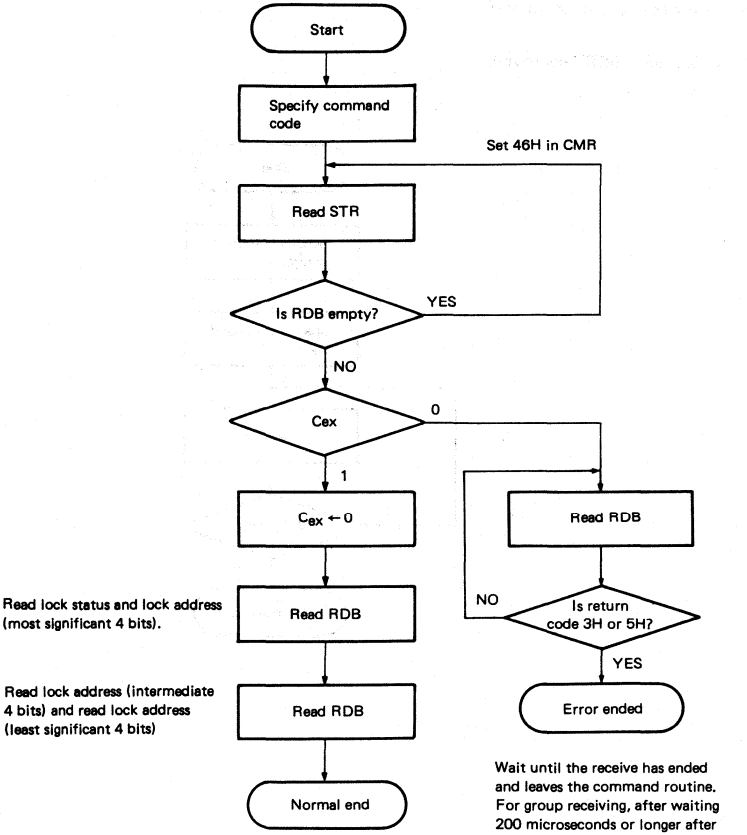
9.5.2 Command routine

The command routine is the routine that sets up the SETSA, MREQ1, MREQ2 (receive), ABORT and GETLOCK commands, all of which control μPD6316 communications. When there is a request in the equipment control routine, the processing starts at (Crq=1).

(1) SETSA and ABORT commands

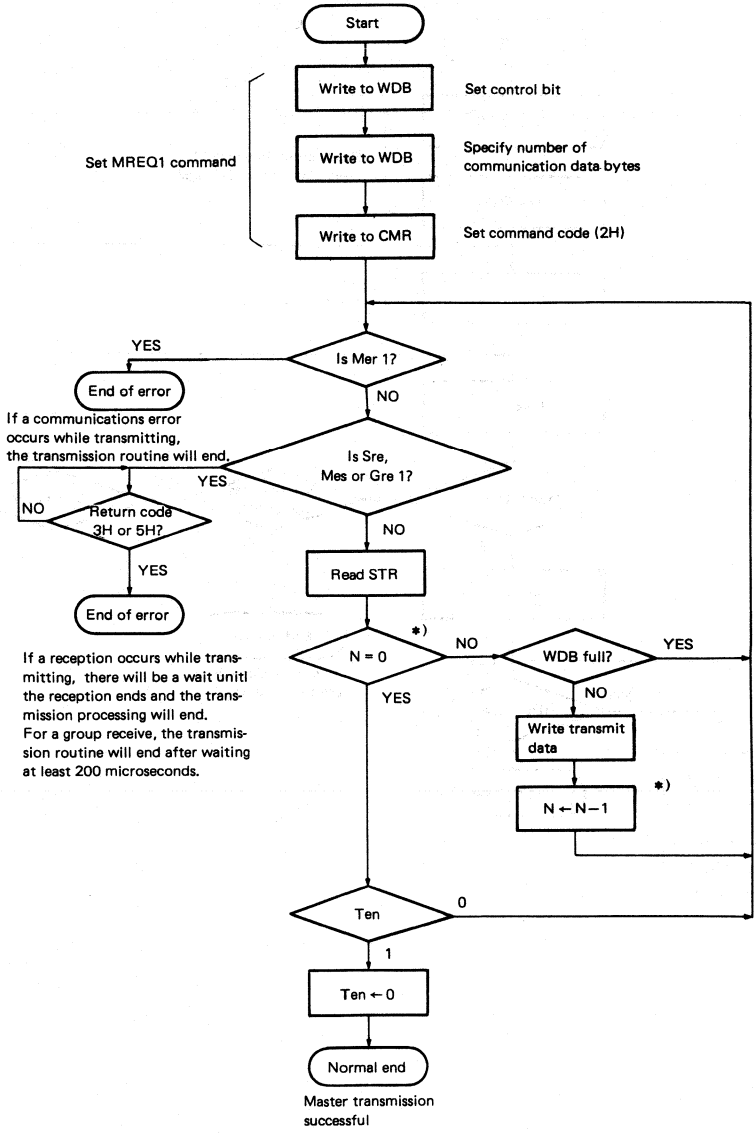


(2) GETLOCK command



9.5.3 Master transmit routine

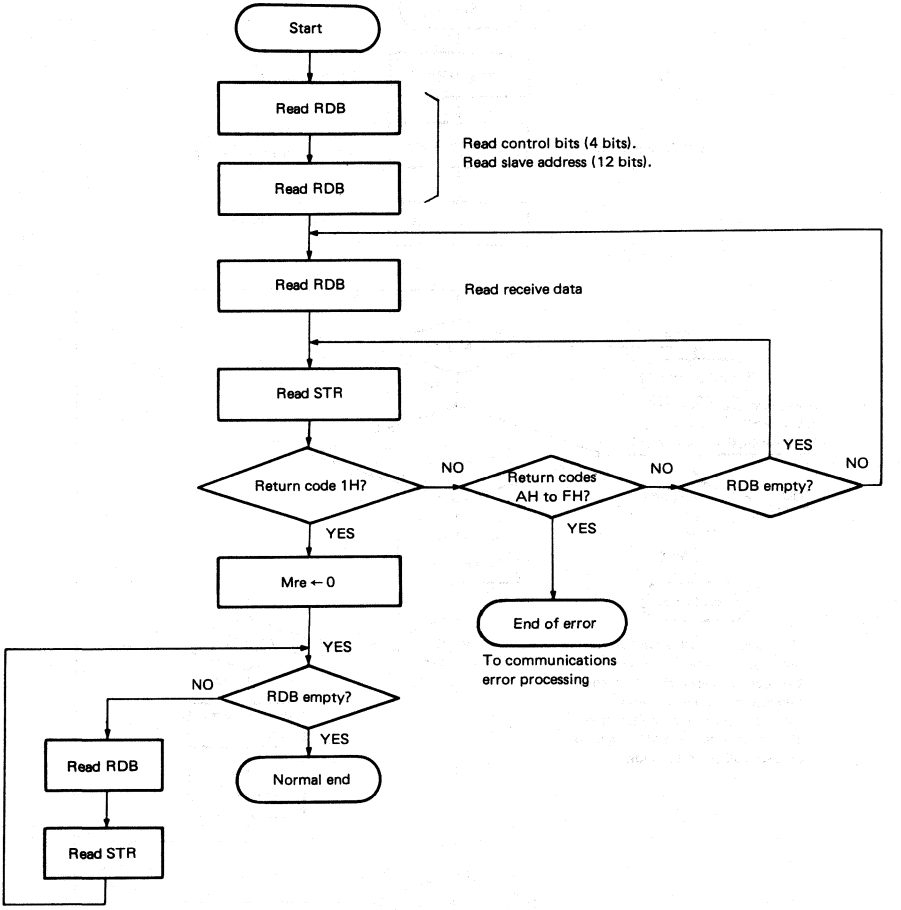
This routine executes the MREQ1 command, and the unit becomes a master unit, transmitting data, commands and memory addresses to the slave unit. With this routine, a check is done of the setup of transmit data, the end of transmission and error generation. In addition, release from this routine occurs when a receive (slave receive, message continuation, group receive) is generated while transmitting.



*) N: Number of transmit data bytes

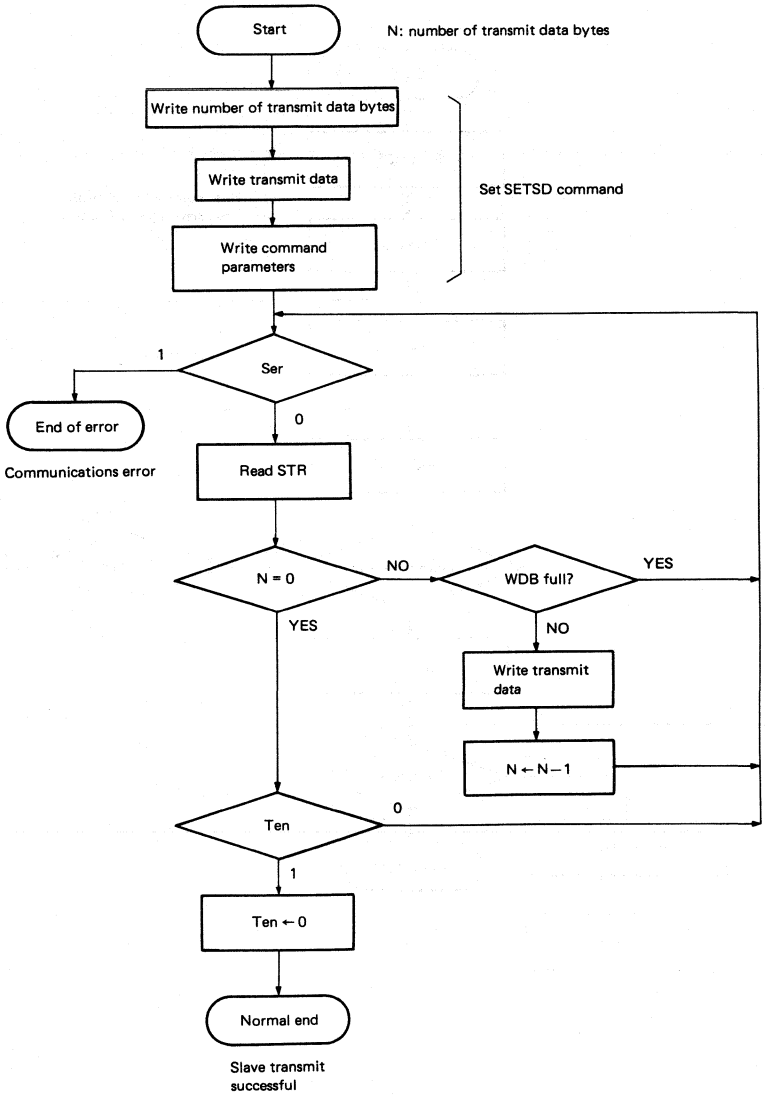
9.5.4 Master receive routine

The routine operates when the master unit executes an MREQ1 command and the data, slave status and lock addresses are received from the slave unit. The processing starts when a master receive start return code (return code 0) or a master receive end return code (return code 1) is returned.



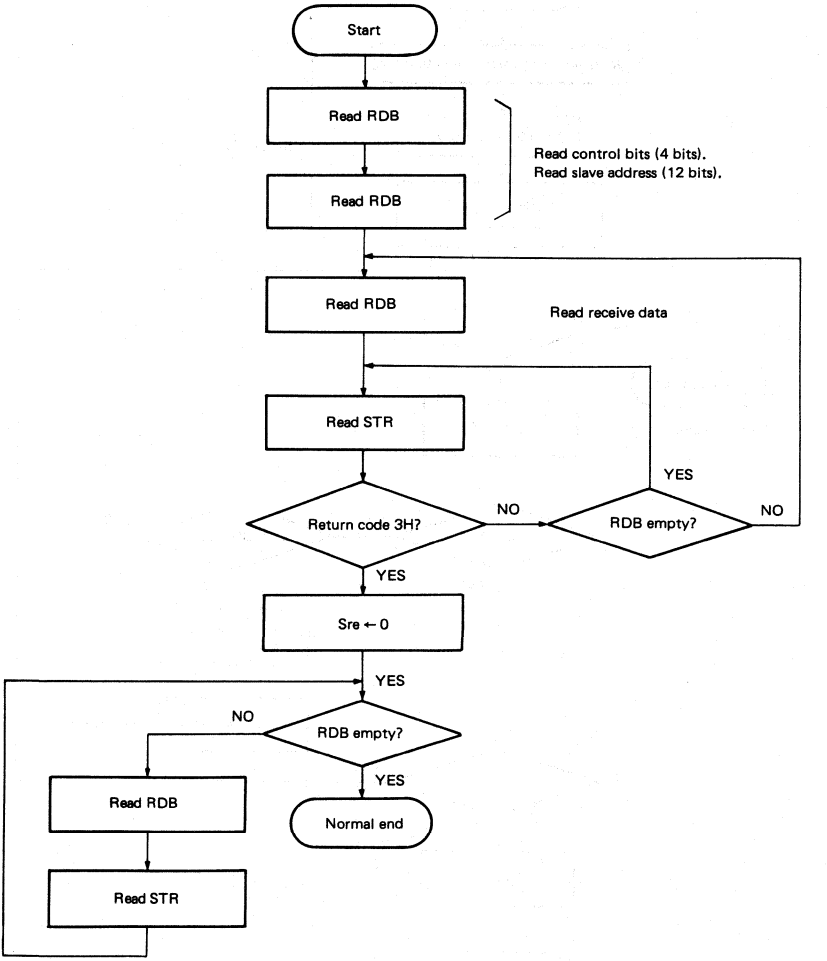
9.5.5 Slave transmit routine

This routine operates when the slave unit executes an SETSD command and transmits data to the master unit. Using this routine, the transmit data specification and communication errors are checked.



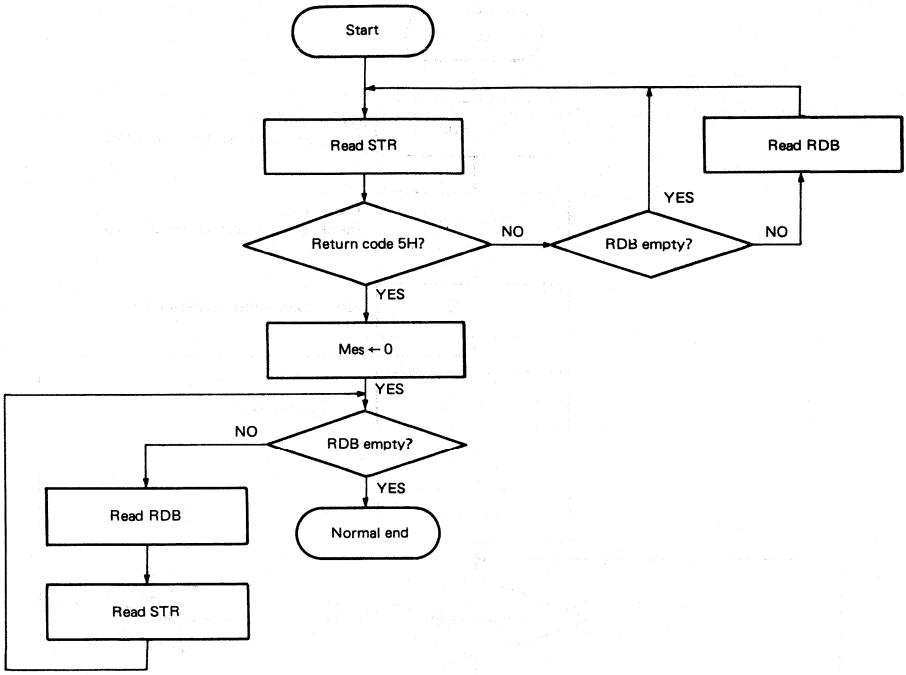
9.5.6 Slave receive routine

This reoutine processes the data, commands and memory addresses when the slave unit receives these from the master unit. The processing starts when a slave receive start (return code 2) or a slave receive end (return code 3) is returned.



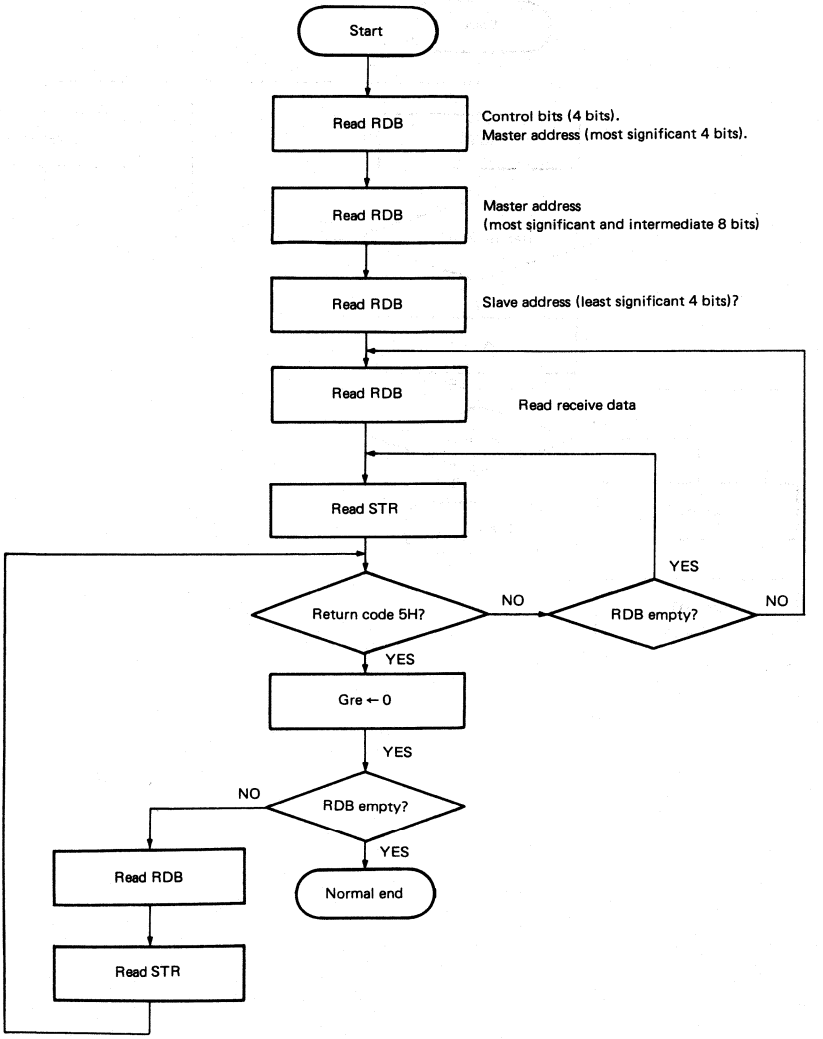
9.5.7 Message continuation routine

This routine operates when a station that specified the message continuation function by means of the SETOP command receives several packets of messages from the master unit. The processing starts after a message continuation start code (return code 4) or a message continuation end code (return code 5) has returned.



9.5.8 Group receive routine

This routine operates when a unit that specified the group receive function by executing the SETOP command receives the data commands and memory addresses of other units with the same group address from the master unit. Processing starts after a group receive start code (return code 4) or a group receive end code (return code 5) is returned.



10. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Power Supply Voltage	V_{DD}	−0.5 to 7.0	V
Logic Input Voltage	V_I	−0.5 to V_{DD} +0.3	V
Logic Output Voltage	V_O	−0.5 to V_{DD} +0.3	V
Bus Input Voltage	V_{BI}	−0.5 to 6.0	V
Bus Output Voltage	V_{BO}	−0.5 to 6.0	V
Operating Temperatures	V_{OUT}	−40 to +85	°C
Storage Temperatures	V_{STG}	−65 to +150	°C

DC CHARACTERISTICS (T_a = −40 to +85 °C; V_{DD} = ±5 %)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH}	0.8 V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	0.0		0.2 V_{DD}	V	
High Level Output Voltage	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 2.5 mA
High Level Input Leak Current	I_{LIH}			10	μA	$V_I = V_{DD}$
Low Level Input Leak Current	I_{LIL}			−10	μA	V_I = 0 V
High Level Output Leak Current	I_{LOH}			10	μA	$V_O = V_{DD}$
Low Level Output Leak Current	I_{LOL}			−10	μA	V_O = 0 V
Power Supply Voltage	I_{DD1}		3.5	10	mA	Carrier sensing time
	I_{DD2}		1.2	3	mA	Reset mode time

CAPACITANCE (T_a = 25 °C; V_{DD} = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_I			15	pF	f_C = 1 MHz
Input/Output Capacitance	C_{IO}			15	pF	0 V

RECOMMENDED CERAMIC VIBRATORS

Maker	Product name	External capacitance [pF]	
		C1	C2
Murata Mfg Co. Ltd.	CSA12.00MX241	22	22
Kyocera Corp.	KBR-12.0M*	33	33

RECOMMENDED LIQUID CRYSTAL VIBRATORS

Maker	Product name	External capacitance [pF]	
		C1	C2
Kinseki Ltd.	HC-49/U	22	22

* The Kyocera KBR-12.0M is a custom product. Please contact Kyocera directly concerning this product.

AC CHARACTERISTICS (T_a = −40 to +85 °C; V_{DD} 5 V = ±5 %)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
System Clock		11.94	12.00	12.06	MHz	
$\overline{SCK}$ Cycle Time	t_{KCY}	0.8			μs	
$\overline{SCK}$ High Level Width	t_{KH}	0.4			μs	
$\overline{SCK}$ Low Level Width	t_{KL}	0.4			μs	
SI Setup Time	t_{SIK}	100			ns	Relative to SCK ↑
SI Hold Time	t_{KSI}	400			ns	Relative to SCK ↑
SO Output Delay Time	t_{KSO}			300	ns	Relative to SCK ↓
$\overline{CS}$, C/$\overline{D}$, R/$\overline{W}$ Setup Time	t_{SA}	0			ns	Relative to SCK ↓
$\overline{CS}$, D/$\overline{D}$, R/$\overline{W}$ Hold Time	t_{HA}	400			ns	Relative to SCK ↑
IRQ Output High Level Width		8		11	μs	
$\overline{RESET}$ Low Level Width		6			μs	
Oscillation Stable Time	t_{OS}	20			ms	

D2B DRIVER/RECEIVER CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Output Current	I_{OH}	2.73		6.22	mA	R_L = 60 Ω ±5 %
Low Level Output Current	I_{OL}			1.0	μA	
In-Phase Output Voltage	V_{OCOM}	2.25	2.50	2.75	V	High level, low level times
High Level Input Voltage	V_{IH}	120			mV	
Low Level Input Voltage	V_{IL}			20	mV	
Input Hysteresis Voltage	V_{IHYS}		25		mV	
High Level In-Phase Input Voltage	V_{IHCOM}	1.00		3.75	V	
Low Level In-Phase Input Voltage	V_{ILCOM}	0		V_{DD}	V	
Driver Output Resistance	R_O	100			kΩ	Between (D2B+) and (D2B−)
Receiver Input Resistance	R_I	1.0			MΩ	Between (D2B+) and (D2B−)
		2.5			MΩ	Between (D2B+) and (GND)
						Between (D2B−) and (GND)
Driver Output Capacitance	C_O			25	pF	Between (D2B+) and (D2B−)
Receiver Input Capacitance	C_I			25	pF	Between (D2B+) and (GND)
						Between (D2B−) and (GND)
Driver Transition Time	t_R			1.60	μs	R = 60 Ω, C = 8000 pF
Receiver Delay Time	t_D			0.75	μs	

Surround Sound ICs

Section 4 - Surround Sound ICs

MATRIX SURROUND-SOUND PROCESSOR

The μPC1891A is a specific IC to reproduce surround-sound by using a signal matrix.

The IC is based on a unique high-speed and low-noise bipolar process and high-precision on-chip filter technology, and provides ideal sound-field effects by using the minimum number of parts.

The IC provides wide, sound with two speakers and rich, stereophonic sound with three speakers.

In the case of stereo signal, the IC has the movie mode to reproduce real human voices, the music mode to permit the listeners to experience the expanse of a music hall, and it has the monaural mode to make monaural signal into wide, deep sound. The modes can be selected freely by using 2-bit parallel control pins.

The package of the IC is a reliable, standard 20-pin DIP.

FEATURES

- Built-in high-precision filter
- Built-in output adjusting attenuator and mute circuit
- 2-bit parallel mode select
- Three modes are available: movie, music, and monaural modes
- Low power consumption: 12 V/20 mA TYP.

APPLICATIONS

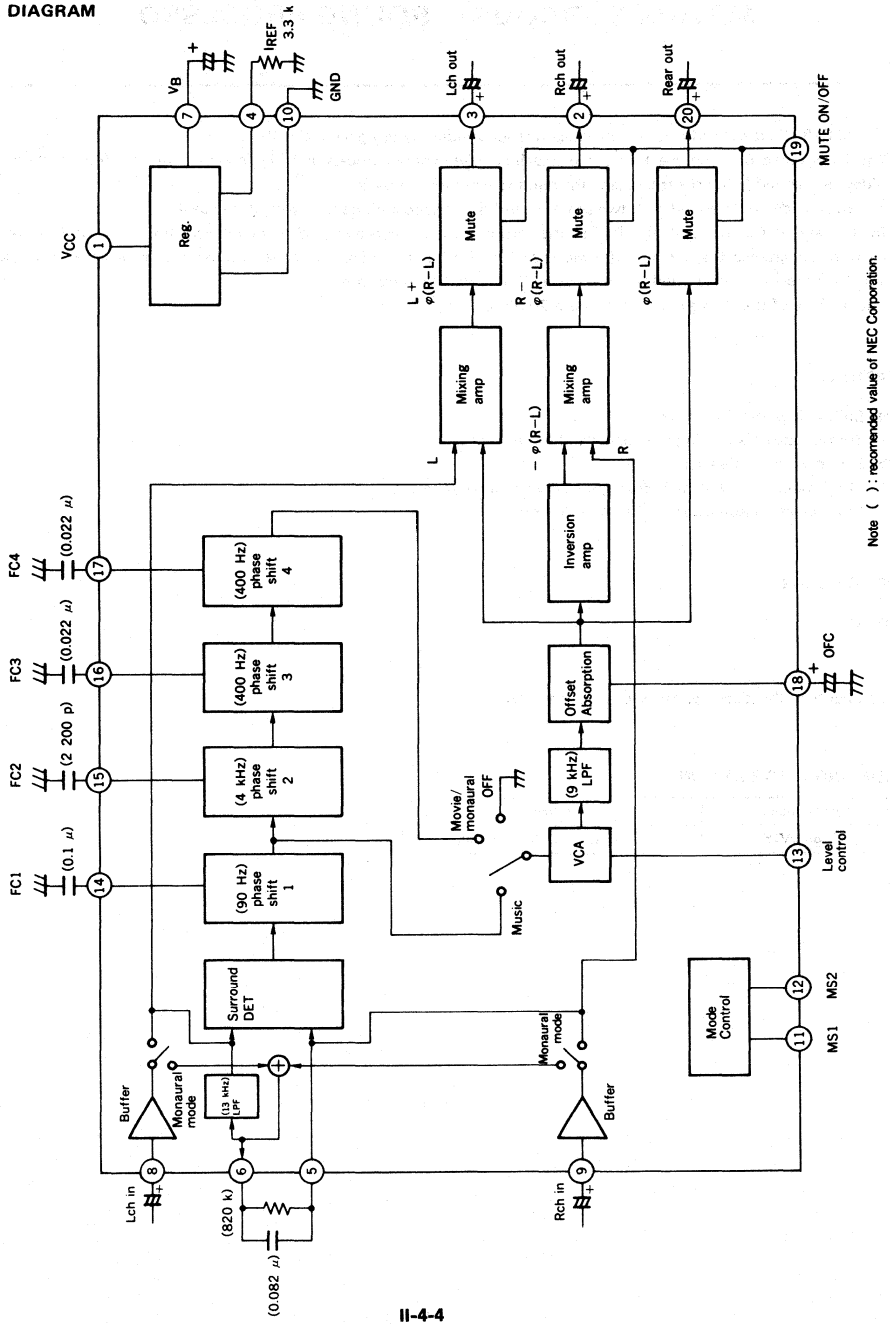
- TV

The contents of this document may change some day.

ORDERING INFORMATION

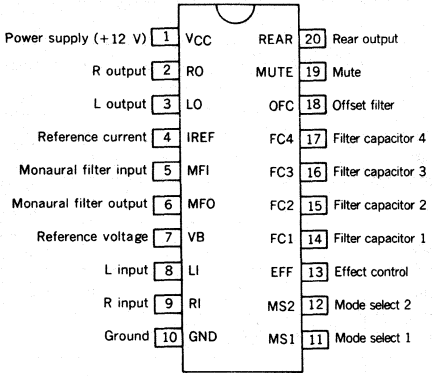
Part Number	Package
μPC1891ACY	20 PIN PLASTIC DIP (400 mil)

BLOCK DIAGRAM



Note ( ): recomended value of NEC Corporation.

PIN CONFIGURATION (Top view)



4

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

ITEM	SYMBOL	RATING	UNIT	CONDITION
Supply Voltage	V_{CC}	+14	V	No signal
Input Pin Voltage	V_{IN}	V_{CC}	V	Voltage applied to pins 8, 9, 11, 12, 13, and 19
Output Pin Current	I_{OUT}	±10	mA	Current to and from pins 2, 3, and 20
Storage Temperature	T_{stg}	−40 to +125	°C	
Package Allowable Loss	P_D	600	mW	T_a = 75 °C

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage (1) (Good Characteristic Range)	$V_{CC}1$	11	12	13	V	
Supply Voltage (2) (Surround Operating Range)	$V_{CC}2$	9		14	V	
Input Signal Amplitude	$V_{L1, R1}$		1.4	2.5	V_{p-p}	Signal voltage input to pins 8 and 9
Mode Select Pin Voltage (High)	V_{MSH}	4	5	V_{CC}	V	High voltage at pins 11 and 12
Mode Select Pin Voltage (Low)	V_{MSL}	0	0	2	V	Low voltage at pins 11 and 12
Mute Pin Voltage (High)	V_{MVTEH}	4	5	V_{CC} −3	V	High voltage at pin 19
Mute Pin Voltage (Low)	V_{MVTEL}	0	0	2	V	Low voltage at pin 19
Effect Pin Voltage (High)	V_{EFFH}		5	V_{CC} −3	V	Upper voltage at pin 13
Effect Pin Voltage (Low)	V_{EFFL}	−	0	−	V	Lower voltage at pin 13
Load Impedance	Z_L	10			kΩ	Output from pins 2, 3, and 20
Ambient Operating Temperature	T_{opt}	−20		+75	°C	

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, RH ≤ 70%, V_{CC} = 12 V)

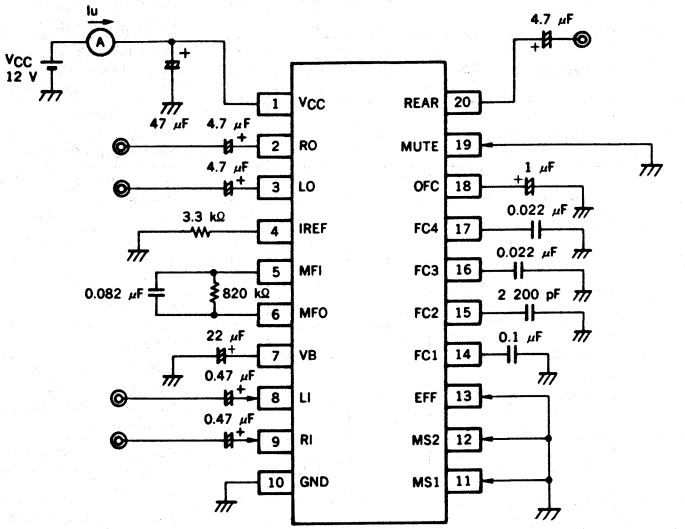
NO.	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	MEASURING CIRCUIT NO.
1	Supply Current	I_{CC}		20	30	mA	Without input: I_{REF} pin resistance: 3.3 kΩ	1
2	Bias Potential	V_B	$\frac{V_{CC}}{2}$–0.2	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}$+0.2	V	Voltage at pin 7	2
3	Reference Current Pin Potential	V_{IR}	1.10	1.20	1.30	V	I_{REF} pin resistance: 3.3 kΩ	2
4	Mode Select Pin Current (1)	I_{MS1}		110	160	μA	Voltage applied to pins 11 and 12: 12 V	3
5	Mode Select Pin Current (2)	I_{MS2}		45	70	μA	Voltage applied to pins 11 and 12: 5 V	3
6	Mode Select Pin Current (3)	I_{MS3}			12	μA	Voltage applied to pins 11 and 12: 0.8 V	3
7	Effect Control Pin Current	I_{EFF}		0.3	1.0	μA	Voltage applied to pin 13: 0.0 to 5.0 V	4
8	Input Pin Voltage	V_I	$\frac{V_{CC}}{2}$–0.2	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}$+0.2	V	Voltage applied to pins 8 and 9	2
9	Output Pin Voltage	V_{OUT}	4.6	5.1	5.6	V	Voltage applied to pins 2, 3, and 20	2
10	In-phase Gain (OFF)	G_{OFF}	–0.2	0.8	1.8	dB	Mode OFF, Input signal of 1 kHz, 1.4 V_{p-p}, Rin → Rout, Lin → Lout	5
11	LR In-phase Gain Difference (OFF)	DG_{OFF}	–1	0	+1	dB	Mode OFF, input signal of 1 kHz, 1.4 V_{p-p} (Rin → Rout) – (Lin → Lout)	5
12	In-phase Gain (Movie 1)	G_{MOV1}	2	7	12	dB	Movie mode, V_{EFF} = 2.5 V Input signal of 1 kHz, 1.4 V_{p-p} Rin → Rout, Lin → Lout	5
13	In-phase Gain (Movie 2)	G_{MOV2}	3	8	13	dB	Movie mode, V_{EFF} = 5.0 V Input signal of 1 kHz, 1.4 V_{p-p} Rin → Rout, Lin → Lout	5
14	LR In-phase Gain Difference (Movie)	DG_{MOV}	–2	0	+2	dB	Movie mode, V_{EFF} = 5.0 V Input signal of 1 kHz, 1.4 V_{p-p} (Rin → Rout) – (Lin → Lout)	5
15	In-phase Gain (Music 1)	G_{MUS1}	4	6	8	dB	Music mode, V_{EFF} = 2.5 V Input signal of 1 kHz, 1.4 V_{p-p} Rin → Rout, Lin → Lout	5
16	In-phase Gain (Music 2)	G_{MUS2}	5.5	7.5	9.5	dB	Music mode, V_{EFF} = 5.0 V Input signal of 1 kHz, 1.4 V_{p-p} Rin → Rout, Lin → Lout	5
17	LR In-phase Gain Difference (Music)	DG_{MUS}	–2	0	+2	dB	Music mode, V_{EFF} = 2.5 V Input signal of 1 kHz, 1.4 V_{p-p} (Rin → Rout) – (Lin → Lout)	5
18	Monaural L Output 1	L_{MON1}	2.5	4.5	6.5	dB	Monaural mode, V_{EFF} = 2.5 V Input signal of 250 kHz 1.4 V_{p-p}, Rin and Lin → Lout	5
19	Monaural L Output 2	L_{NON2}		–4.0	0.0	dB	Monaural mode, V_{EFF} = 2.5 V Input signal of 1 kHz, 1.4 V_{p-p}, Rin and Lin → Lout	5
20	Monaural L Output 3	L_{MON3}	4.5	7.0	9.5	dB	Monaural mode, V_{EFF} = 2.5 V Input signal of 3.6 kHz, 1.4 V_{p-p}, Rin and Lin → Lout	5

NO.	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	MEASURING CIRCUIT NO.
21	Monaural R Output 1	R_{MON1}		−4.5	0.0	dB	Monaural mode, V_{EFF} = 2.5 V Input signal of 250 kHz, 1.4 V_{p-p}, Rin and Lin → Lout	5
22	Monaural R Output 2	R_{MON2}	1.8	3.8	5.8	dB	Monaural mode, V_{EFF} = 2.5 V Input signal of 1 kHz, 1.4 V_{p-p}, Rin and Lin → Lout	5
23	Monaural R Output 3	R_{MON3}		−20	−8	dB	Monaural mode, V_{EFF} = 2.5 V Input signal of 3.6 kHz, 1.4 V_{p-p}, Rin and Lin → REARout	5
24	Rear Output Gain 1	G_{REA1}		−30		dB	Music mode, V_{EFF} = 0.0 V Input signal of 1 kHz, 1.4 V_{p-p}, Rin or Lin → REARout	6
25	Rear Output Gain 2	G_{REA2}	−12	−9.4	−8.0	dB	Music mode, V_{EFF} = 2.5 V Input signal of 1 kHz, 1.4 V_{p-p}, Rin or Lin → REARout	6
26	Rear Output Gain 3	G_{REA3}		−8.2	−5.0	dB	Music mode, V_{EFF} = 5 V Input signal of 1 kHz, 1.4 V_{p-p}, Rin or Lin → Lout	6
27	Maximum Output	V_{OM1}	7.8	8.2		V_{p-p}	Mode OFF, V_{CC} = 12 V, Input signal of 1 kHz T.H.D. = 3 %, Rout and Lout measurement	7
28	Distortion Factor	T.H.D.		0.1	0.5	%	Mode OFF, Input signal of 1 kHz, 1.4 V_{p-p}, Rin → Rout, Lin → Lout	7
29	Output Noise (OFF)	$N_{O(OFF)}$		0.2	0.4	$mV_{r.m.s.}$	Mode OFF, Input termination Using DIN/AUDIO, Rout and Lout measurement	8
30	Output Noise (Movie)	$N_{O(MOV)}$		0.2	0.4	$mV_{r.m.s.}$	Movie mode, Input termination Using DIN/AUDIO, Rout and Lout measurement	8
31	Output Noise (Music)	$N_{O(MUS)}$		0.2	0.4	$mV_{r.m.s.}$	Music mode, Input termination Using DIN/AUDIO, Rout and Lout measurement	8
32	Output Noise (Monaural)	$N_{O(MON)}$		0.2	0.4	$mV_{r.m.s.}$	Monaural mode, Input termination Using DIN/AUDIO, Rout and Lout measurement	8
33	Mute Attenuation	D_M		−80	−70	dB	Mode OFF, V_{EFF} = 2.5 V, V_{MUTE} = 5 V Input signal of 4 kHz, 1.4 V_{p-p}, Rin → Rout, Lin → Lout	9
34	Crosstalk	S_x		−60	−50	dB	Mode OFF, V_{EFF} = 2.5 V Input signal of 4 kHz, 1.4 V_{p-p}, Rin → Lout, Lin → Rout	9
35	Inter-mode Offset	V_{OSM}	−150	0	150	mV	Difference among values in each modes Rout, Lout and REARout	10
36	Mute offset	V_{OSD}	−150	0	150	mV	Difference between mute-on/off values Rout, Lout, and REARout measurement	10
37	Signal Input Pin Impedance	Z_{IN}	20	40		kΩ	Rin and Lin measurement	11
38	Output Pin Impedance	Z_{OUT}		20	60	Ω	Rout, Lout, and REARout measurement	

Note: Rin : pin 9
Lin : pin 8
Rout : pin 2
Lout : pin 3
REARout : pin 20

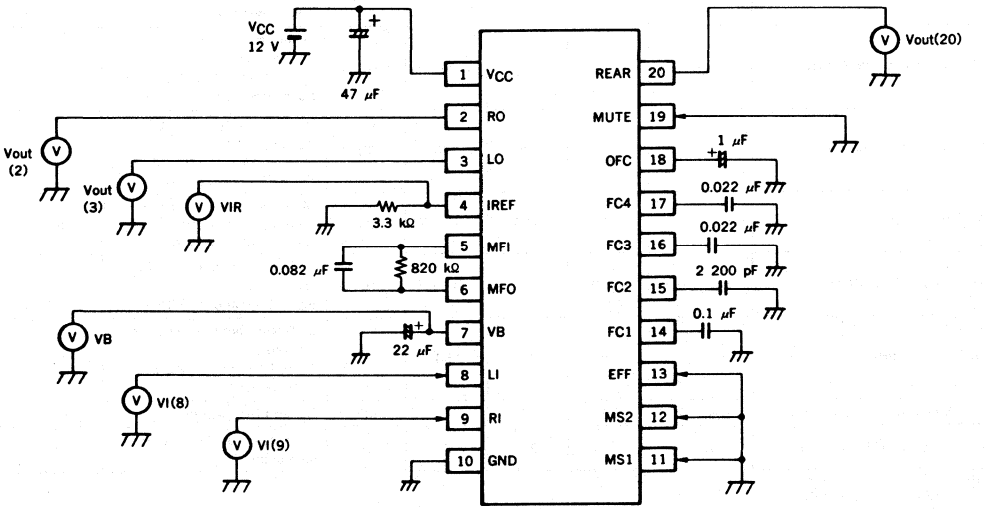
Measuring Circuit 1

Power supply Current (I_{CC})



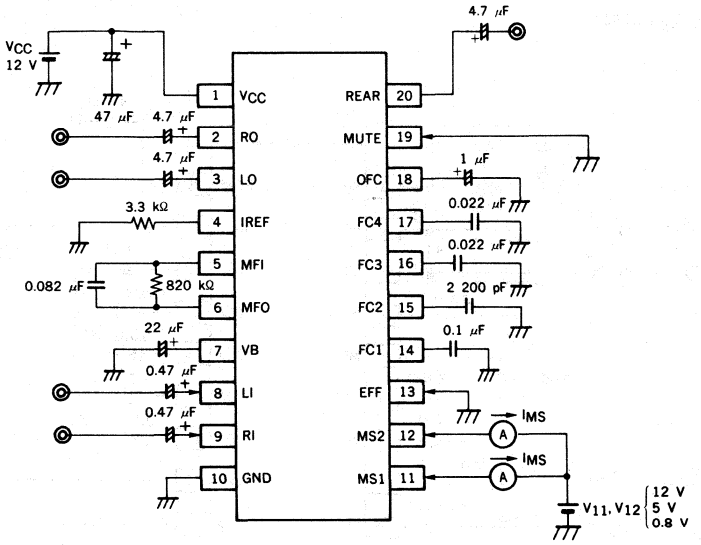
Measuring Circuit 2

Bias potential input/output pin potential and reference current pin potential



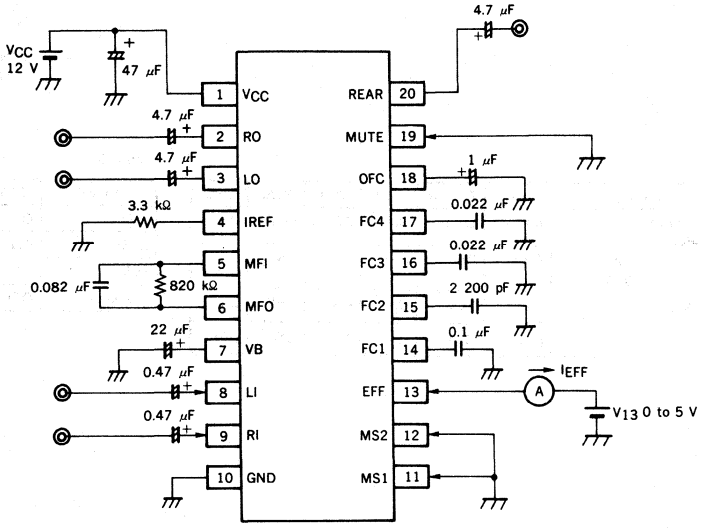
Measuring Circuit 3

Mode select pin current (I_{MS})



Measuring Circuit 4

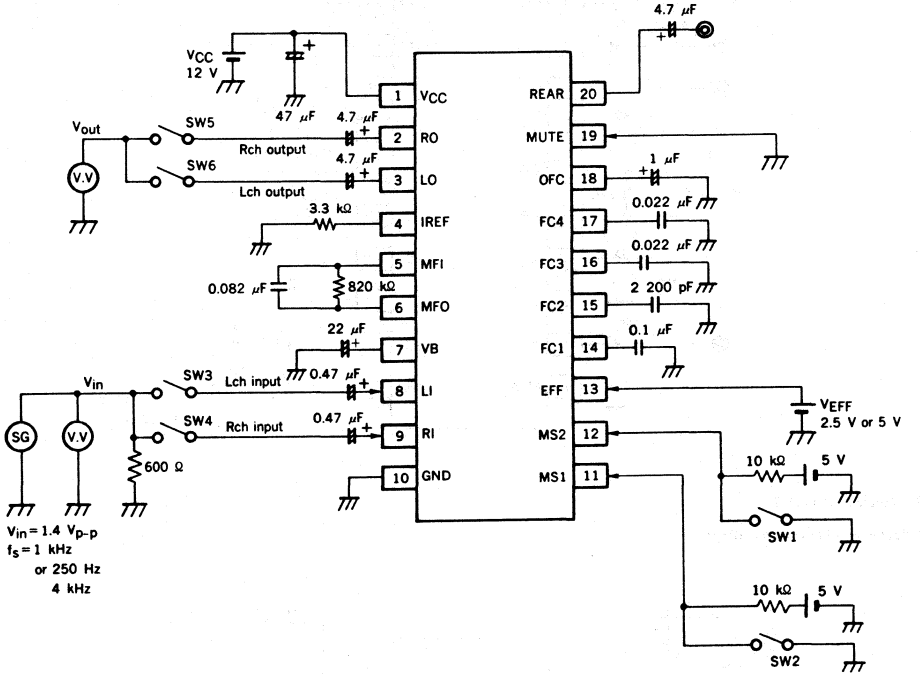
Effect control pin current (I_{EFF})



Measuring Circuit 5

In-phase gain and monaural output

$$\text{Gain} = 20 \log \left(\frac{V_{out}}{V_{in}}\right)$$



Item	Input	Output	SW3	SW4	SW5	SW6
In-phase gain Mode: Off Music Movie	Lin	Lout	ON	OFF	OFF	ON
	Rin	Rout	OFF	ON	ON	OFF
Monaural output	Lin and Rin	Lout	ON	ON	OFF	ON
		Rout	ON	ON	ON	OFF

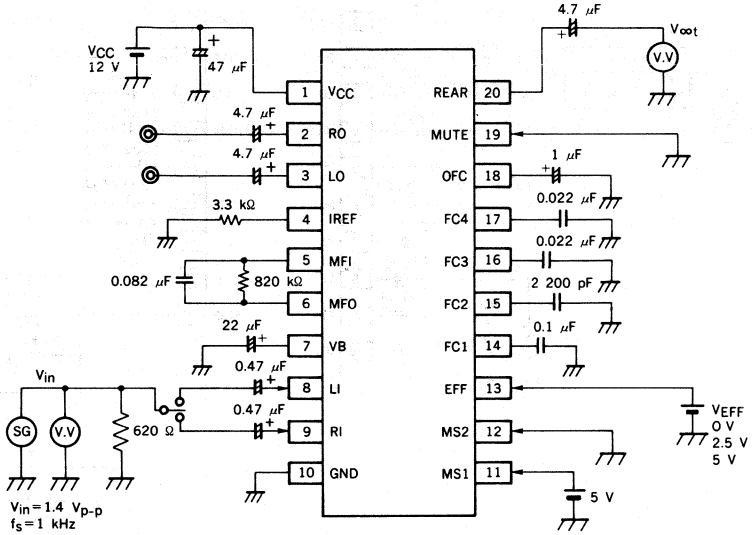
Mode Select

Mode	SW1	SW2
OFF	ON	ON
Music	ON	OFF
Movie	OFF	ON
Monaural	OFF	OFF

Measuring Circuit 6

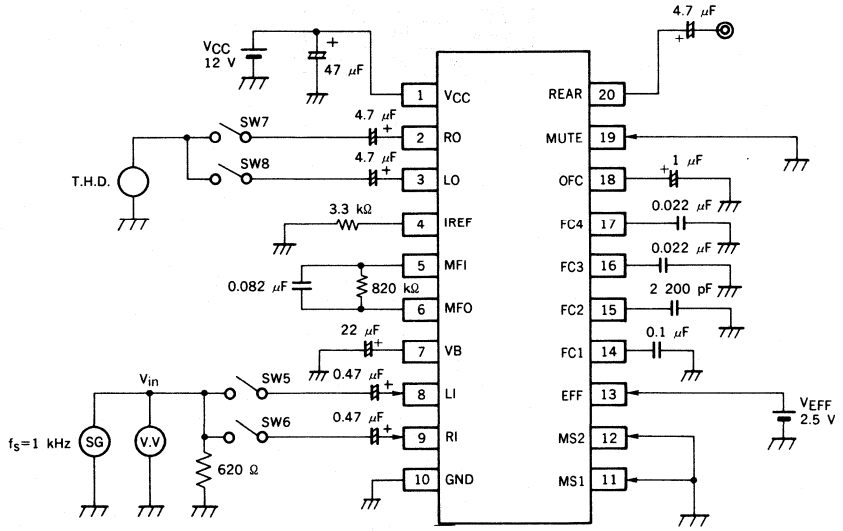
Rear output gain (G_{REA})

$$\text{Gain} = 20 \log \left(\frac{V_{out}}{V_{in}} \right)$$



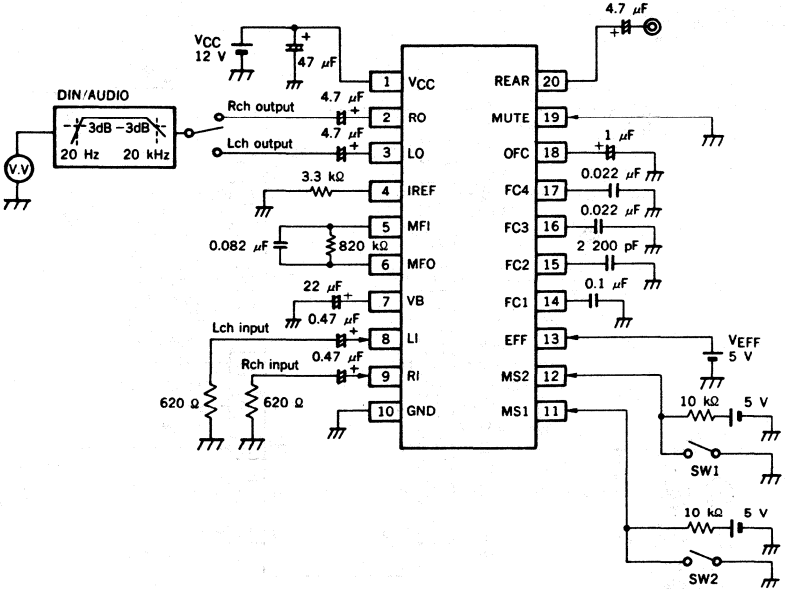
Measuring Circuit 7

Maximum output and distortion factor (V_{OM}, T.H.D.)



Measuring Circuit 8

Output noise (N_O)

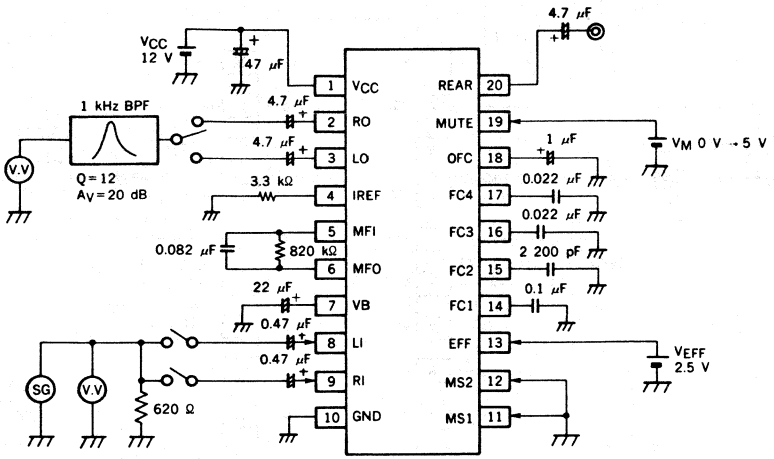


Mode select

Mode	SW1	SW2
OFF	ON	ON
Music	ON	OFF
Movie	OFF	ON
Monaural	OFF	OFF

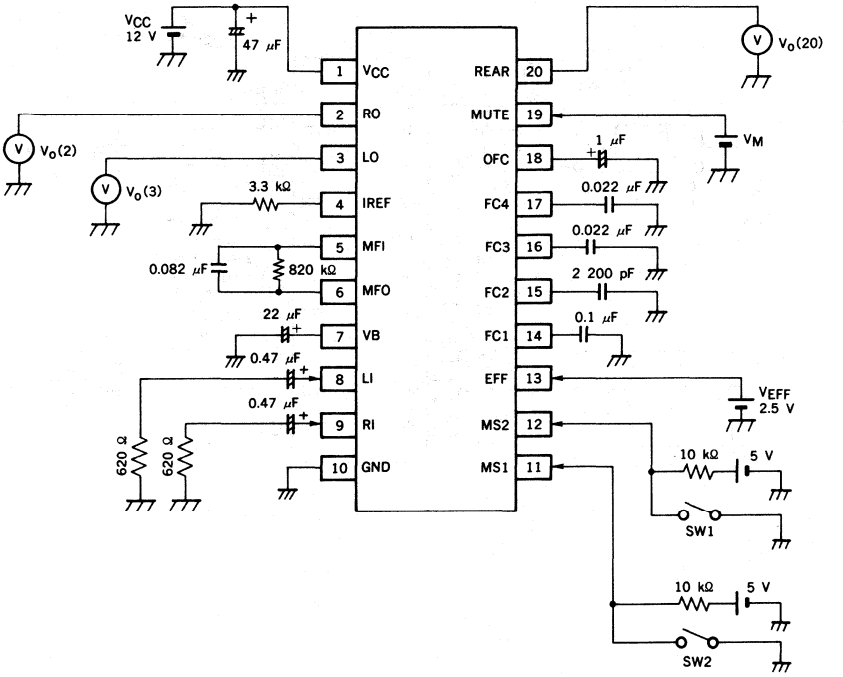
Measuring Circuit 9

Mute attenuation (DM) and crosstalk (SX)



Measuring Circuit 10

Inter-mode and mute offsets



- Inter-mode offset (V_{OSM})
  Between V_o (in each mode) and V_o (in OFF mode)
  (Note: V_M = 0 V)
- Mute offset (V_{OSD})
  Between V_o (V_M = 0 V) and V_o (V_M = 5 V)
  (Note: Mode OFF)

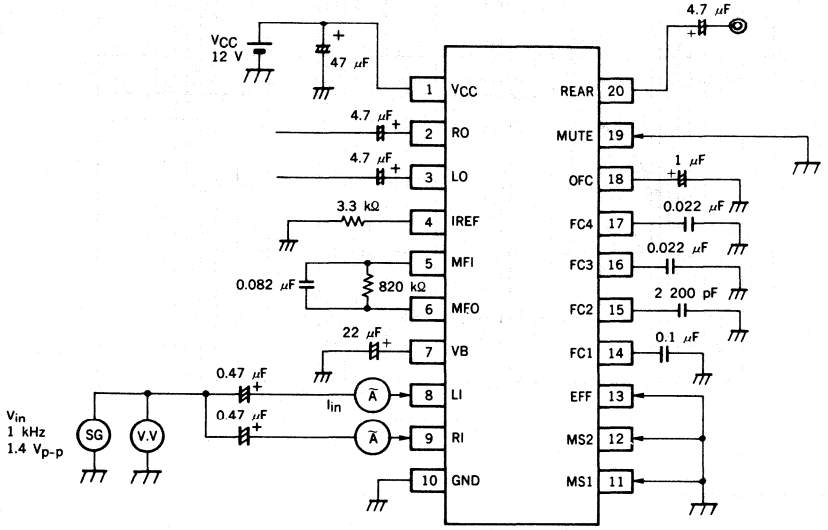
Mode Select

Mode	SW1	SW2
OFF	ON	ON
Music	ON	OFF
Movie	OFF	ON
Monaural	OFF	OFF

Measuring Circuit 11

Signal input pin impedance (Z_{in})

$$Z_{in} = \frac{V_{in}}{I_{in}}$$



Mode Control

The μPC1891A allows four types of surround effects in the movie, music, monaural and OFF modes to be selected according to their respective combinations of H and L levels of pins No. 11 (MS1) and No. 12 (MS2).

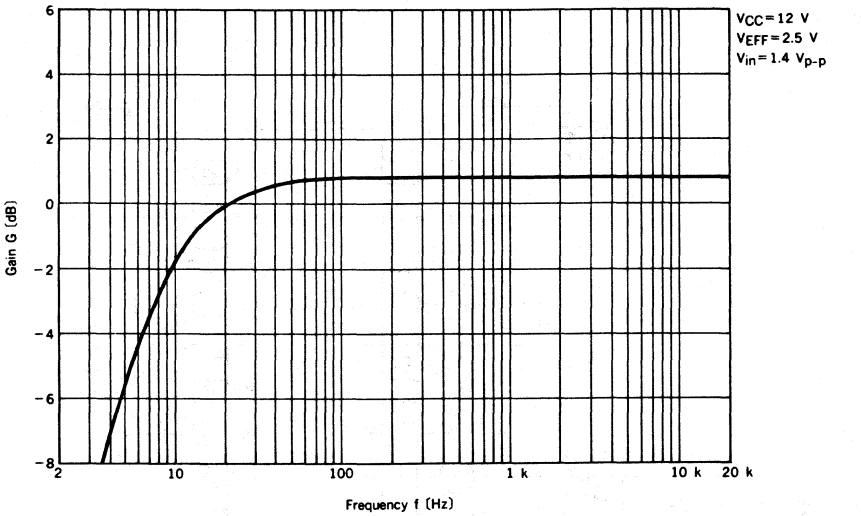
Mode Select Code

Code / Mode	MS1 (11)	MS2 (12)
OFF	L	L
Music	H	L
Movie	L	H
Monaural	H	H

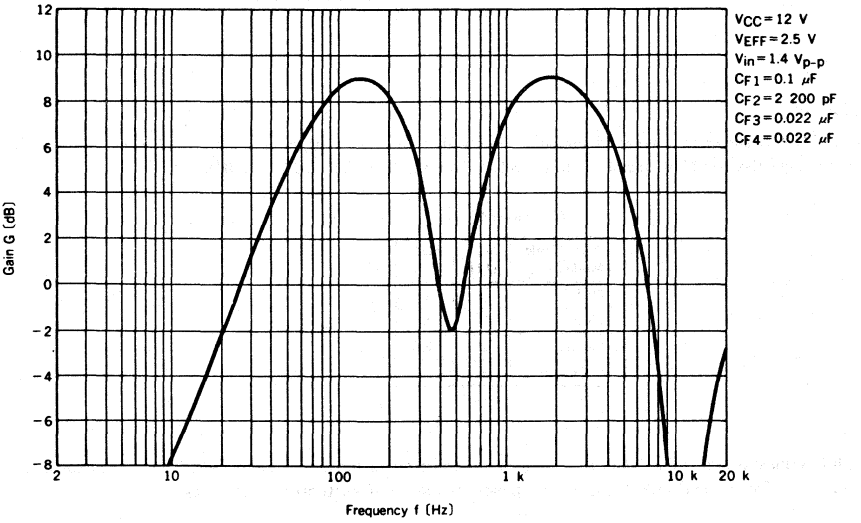
The following shows reference data for frequency response characteristics in each mode. It will help explain each type of surround effect. For the characteristics of the IC, please see the list of electrical characteristics.

Frequency Response Characteristics in Each Mode (T_a = 25 °C)

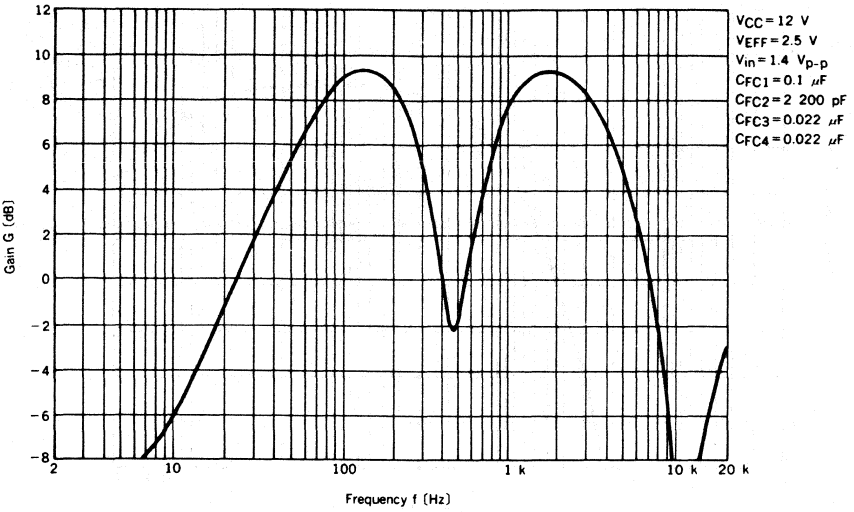
1. **OFF Mode (Lch, Rch)**



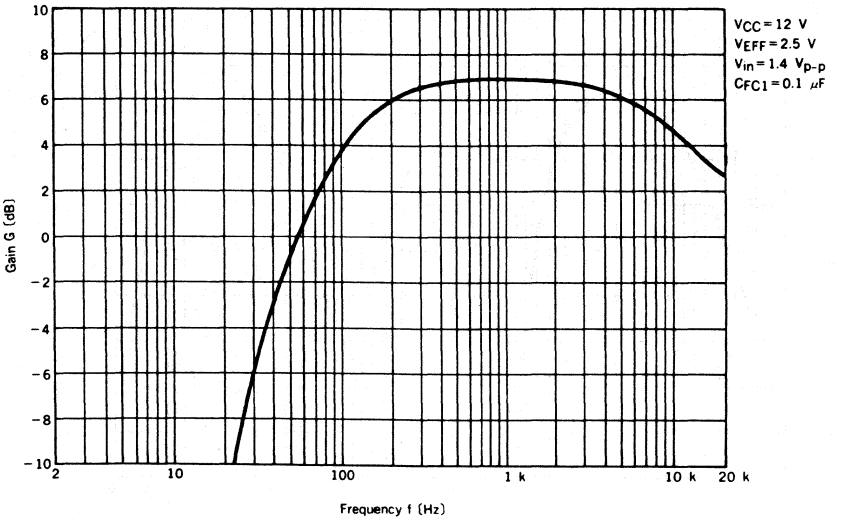
2. **Movie Mode (Lch)**



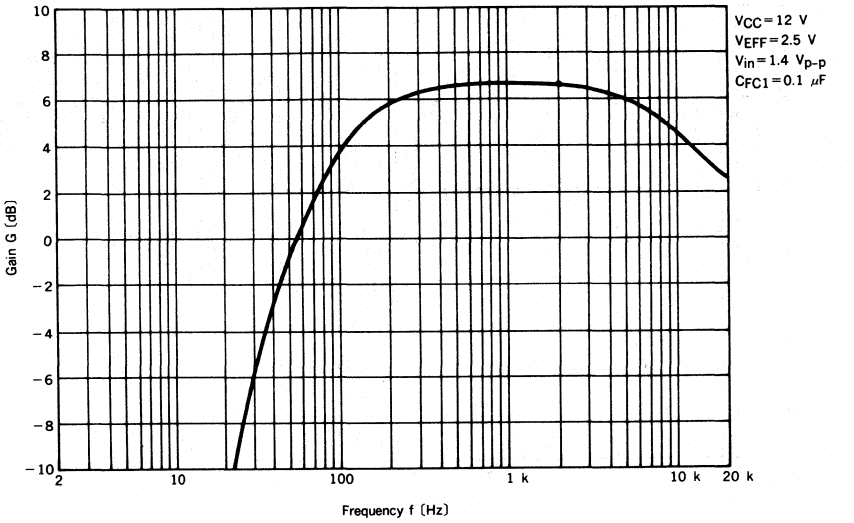
3. Movie Mode (Rch)



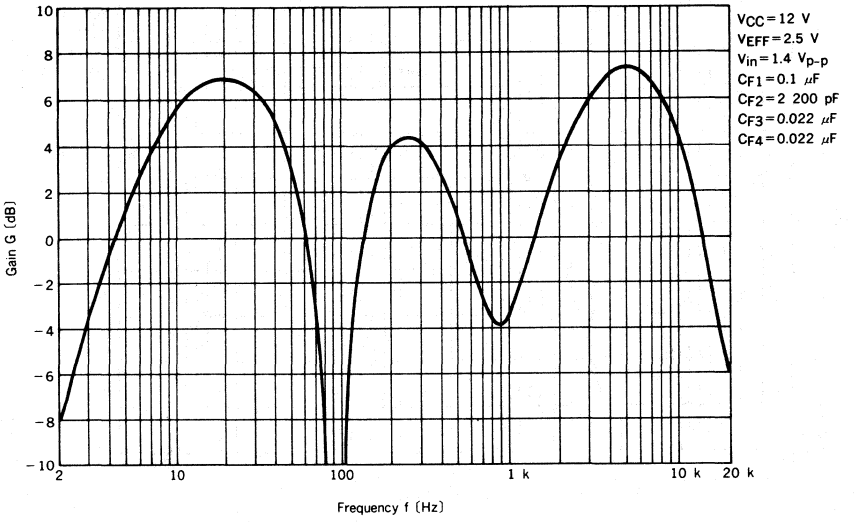
4. Music Mode (Lch)



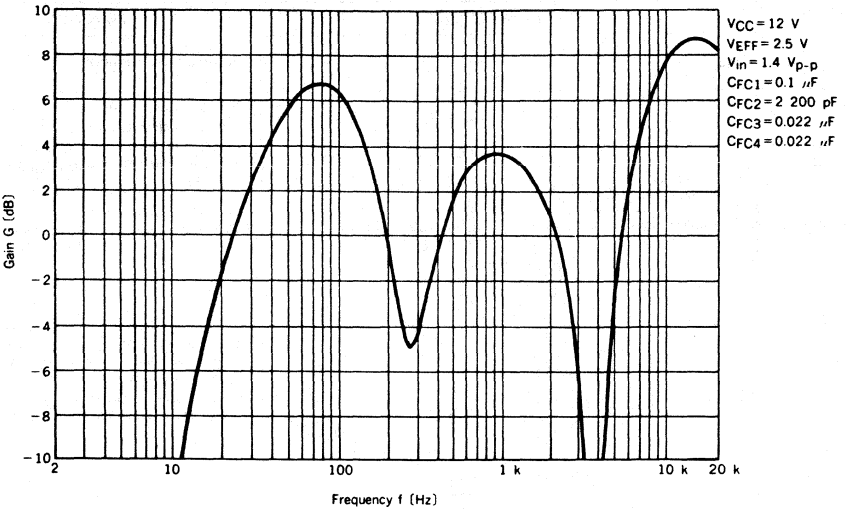
5. Music Mode (Rch)



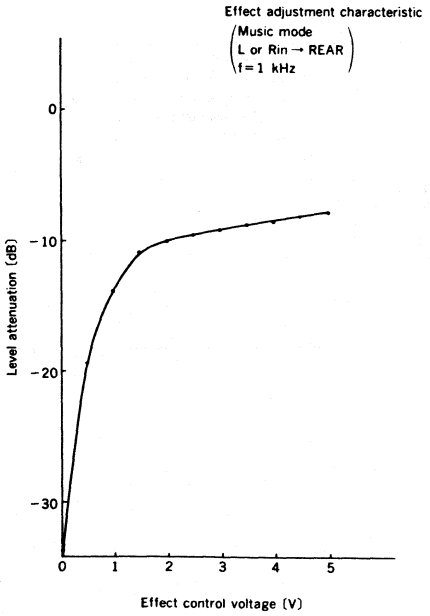
6. Monaural Mode (Lch)



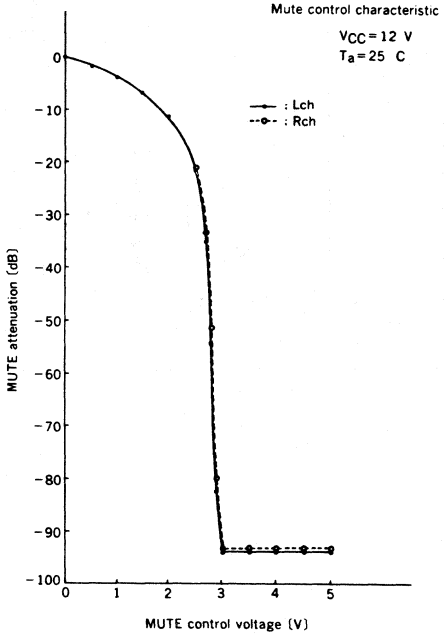
7. **Monaural Mode (Rch)**



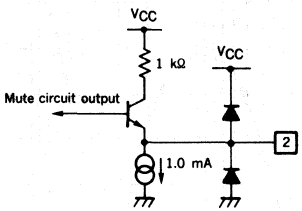
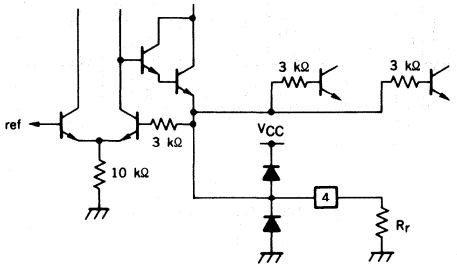
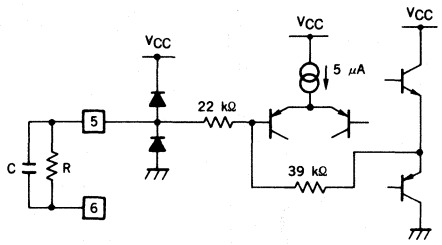
Effect Adjustment Characteristic

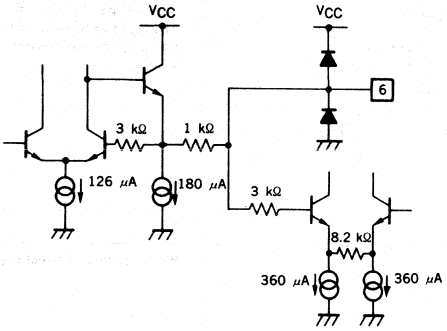
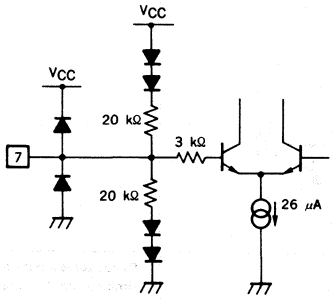
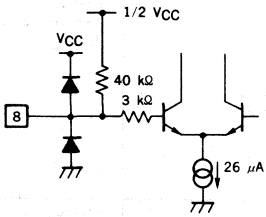


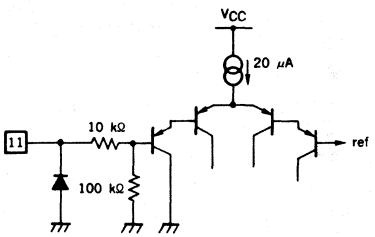
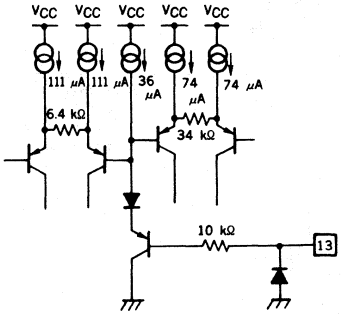
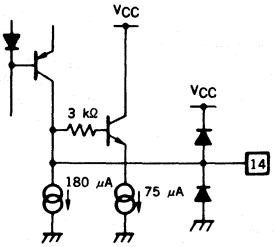
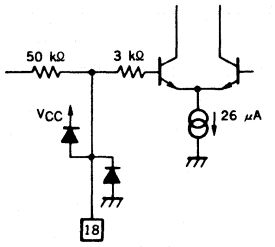
Mute Control Characteristic

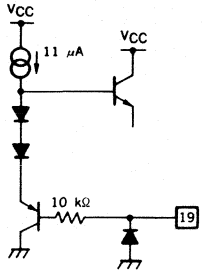


Pin Function

PIN NO.	EQUIVALENT CIRCUIT	FUNCTION
1 (12.0 V)	V_{CC}	Power Supply Terminal
2 3 20 (5.2 V)		Pin 2 : Rch output pin Pin 3 : Lch output pin Pin 20 : Rear channel output pin These pins have DC voltage V_{BE} lower than 1/2 V_{CC}.
4 (1.2 V)		Adjuster pin to determine the time constant (f response characteristic in surround mode) of the phase shifter. Set the current flowing from pin 4. Note: R_r must be 3.3 kΩ.
5 (6.0 V)		Pin for HPF in the monaural mode. Insert CR between pins 5 and 6. Time constant fc: fc = 1/2πC x (R//Z) Z is the input impedance of pin 5: about 61 kΩ.

PIN NO.	EQUIVALENT CIRCUIT	FUNCTION
6 (6.0 V)		Pin for HPF in the monaural mode like the case of pin 5.
7 (6.0 V)		The pin to connect the power supply ripple filter and has: Operating point bias: 1/2 V_{CC}. Impedance: About 10 kΩ.
8 9 (6.0 V)		Pin 8 : Lch input pin Pin 9 : Rch input pin The input impedance is about 40 kΩ.
10 (0.0 V)	GND	Pin for ground of device

PIN NO.	EQUIVALENT CIRCUIT	FUNCTION
11 12		The pins select one of the surround modes. (Two-bit parallel control by pins 11 and 12) The input impedance of each pin is about 110 kΩ. The pin becomes low when it is opened.
13		Pin for surround effect adjustment.
14 15 16 17 (6.7 V)		Capacitor connection pin to determine the time constant of the phase shifter. Pin 14 is for music surround-sound. Pins 14 to 17 are for movie and monaural surround sound. Each pin has DC voltage V_{BE} higher than 1/2 V_{CC}.
18 (6.0 V)		Matrix circuit DC offset absorption pin. The pin absorbs the offset generated from the phase shifter.

PIN NO.	EQUIVALENT CIRCUIT	FUNCTION
19		Pin for mute circuit control.

The μPD6380GC is a fixed-point CMOS digital signal processor that processes audio digital signals in the real time mode.

Since the μPD6380GC has a 19-bit data bus, 16-bit audio data can be processed accurately.

A harbored architecture in which instruction and data memories are allocated separately is employed as a basic architecture, which enables simultaneous execution of ALU operation, data transfer, and pointer operation.

The cycle time of one instruction is 122 ns; the built-in dedicated parallel multiplier (19 x 16 → 31 bits) carries out multiplication in one instruction cycle.

Instruction and coefficient memories are RAMs, that is, multiprocessing is enabled by rewriting data from the host CPU.

Moreover, dedicated hardware is incorporated for controlling the audio serial interface and external delay RAM (256K) and the configuration is designed to facilitate double-precision operation. Therefore, the μPD6380GC is most suitable for audio digital signal processing such as tone quality control and sound field adjustment.

Order information

Order name	Package	Package symbol
μPD6380GC	52-pin QFP	S52GC-100-3BH

Features

The μPD6380GC has the following features:

- The μPD6380GC has an instruction RAM (22 bits x 192 words), a coefficient RAM (16 bits x 128 words), and a data RAM (19 bits x 128 words).

- Horizontal instructions are used so that an ALU operation, data transfer, and memory address updating can be carried out with only one instruction.

- Two serial input ports and two serial output ports are provided to support four channels.

- The host CPU can rewrite the contents of instruction and coefficient RAMs dynamically without discontinuing sound processing.

- A maximum of 370 ms (1 fs x 16K addresses) digital delay was attained by an external 256K DRAM (64K x 4).

- An on-chip dedicated parallel multiplier (19 bits x 16 bits = 31 bits).

- The internal data bus width is 19 bits and the word length of the data RAM is 19 bits; however, up to 31 bits may be used for multiplication and addition. With a shifter, double-precision operations can be performed.

- An on-chip host CPU interface.

- The accumulator and ALU have a high-order 3-bit overflow margin, thus enhancing the operation accuracy.

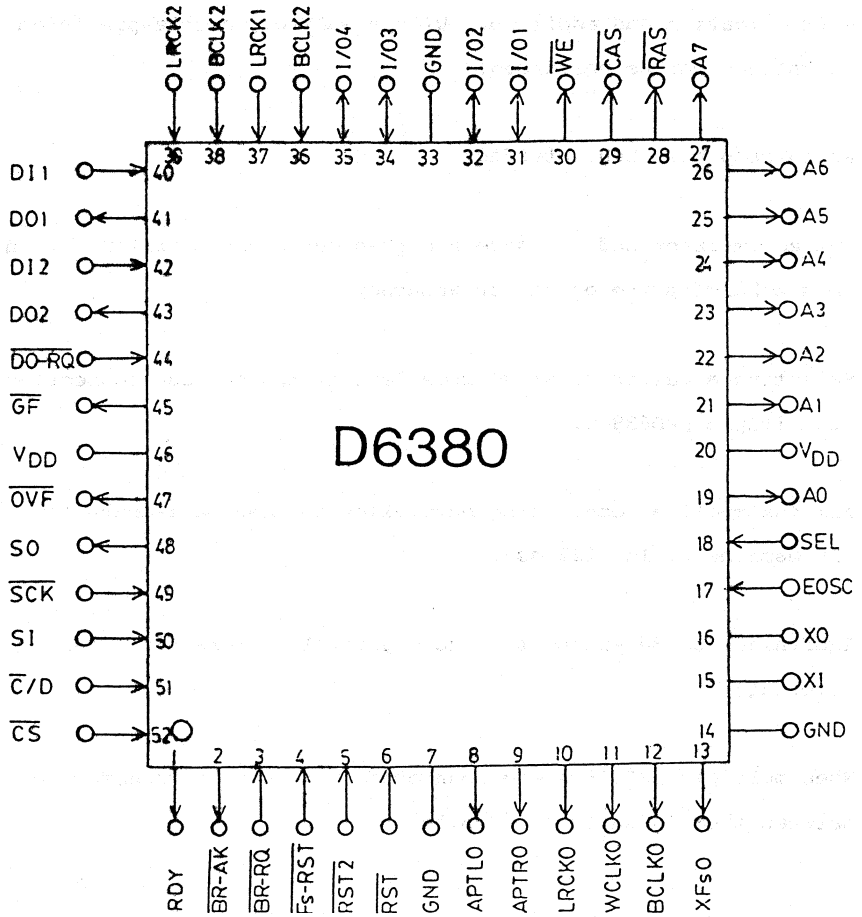
- Selecting a master or slave mode facilitates cascade connection of multiple μPD6380s.

- All instructions containing multiplication can be executed in one machine cycle (122 ns).

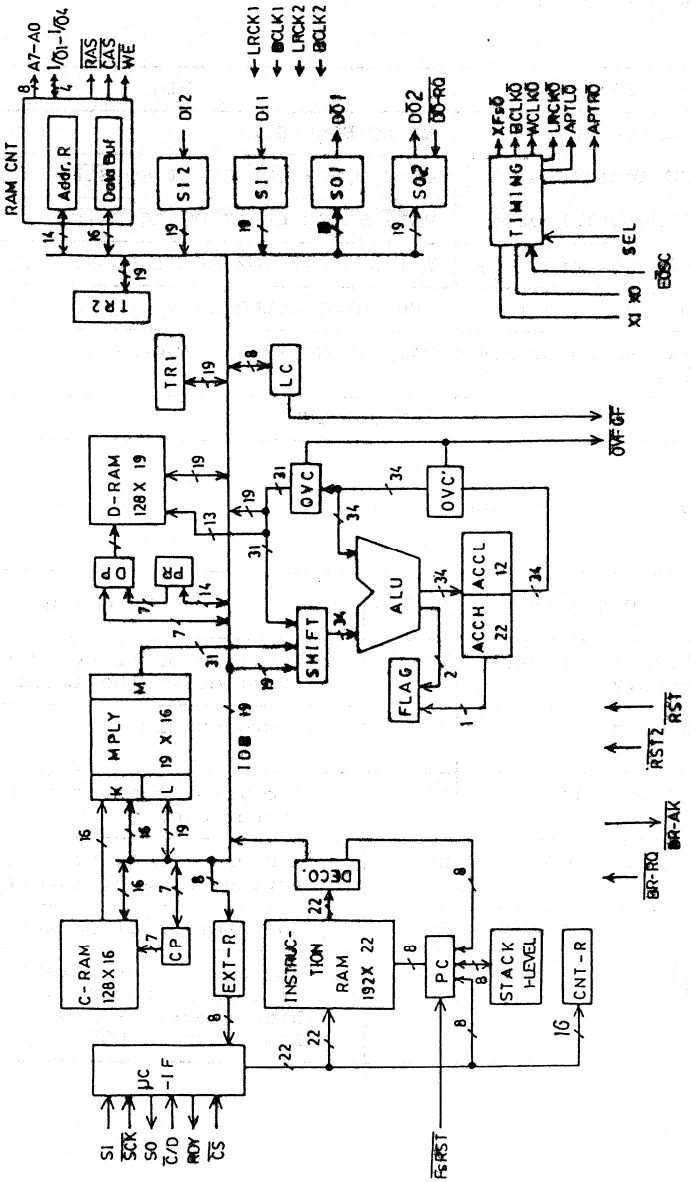
- Equivalent to 30 secondary biquad digital filters (44.1 kHz sampling)

- When multiple μPD6380s are connected, data can be transferred between them in units of 19 bits.

Pin connections



Internal block diagram



1. PIN FUNCTIONS

1.1 Classification of Pins

Classification	Pin
System clock input	XI XO EOSC SEL
Host CPU interface	$\overline{CS}$ C/$\overline{D}$ RDY $\overline{OVF}$ $\overline{GF}$ SI SO $\overline{SCK}$
Emulation mode	$\overline{RST2}$ $\overline{BR\text{-}RQ}$ $\overline{BR\text{-}AK}$ $\overline{DO\text{-}RQ}$ $\overline{Fs\text{-}RST}$
Audio signal interface	DI1 DO1 DI2 DO2 LRCK1 BCLK1 LRCK2 BCLK2
A/D and D/A support	XFs BCLKO WCLKO LRCKO APTLO APTRO
External RAM interface for delay	$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$ A7-A0 I/O4-I/O1
Others	$\overline{RST}$ VDD GND

1.2 Explanation of Pins

Pin No.	Pin name	Symbol	I/O	Function
20 46	Positive power supply	Vdd		Positive power (+5 V ±10%) is supplied to the logic circuit.
7, 14 33	Ground	GND		A ground pin
15	Crystal in	XI		A crystal connection pin (input side of inverter)
16	Crystal out	XO		A crystal connection pin (output side of inverter)
17	External clock	EOSC	I	An external clock input pin
18	Clock selection input	SEL	I	The signal for selecting XI/XO or EOSC is selected. High input: XI/XO Low input : EOSC

Pin No.	Pin name	Symbol	I/O	Function
52	Chip select	$\overline{CS}$	I	A D6380 chip selection signal input pin. When the $\overline{CS}$ signal is active, data can be transferred to/from the host CPU via the SO/SI pin. The signal transferred to the SI pin is latched at the rising edge of the $\overline{CS}$ signal.
51	Command/data input specification	$\overline{C}/D$	I	L: The signal input from the SI pin is a command. H: The signal input from the SI pin is data.
50	Serial data input	SI	I	A command/data is input to the D6380. Serial data is input.
48	Serial data output	SO	O	The contents of the EXT register or program counter are output serially. An N-channel open drain pin.
49	Serial data clock input	$\overline{SCK}$	I	The signal input or output to/from the SI/SO pin is synchronized with this clock pulse.
1	Ready flag output	RDY	O	The SI pin is ready for receiving a command/data. An N-channel open drain pin.
6	Reset input	$\overline{RST}$	I	A D6380 reset signal input pin.
5	Reset 2 input	$\overline{RST2}$	I	A reset signal is input to rewrite the instruction RAM without changing the contents of the register in the D6380.
4	Fs reset input	$\overline{Fs\text{-}RST}$	I	A program counter reset signal input pin. This pin is used in the emulator mode.
3	Break request input	$\overline{BR\text{-}RQ}$	I	A signal is input to issue a break request from the host to the D6380. When this signal is issued, the internal BRRQ flag is set. This pin is used in the emulator mode.

Pin No.	Pin name	Symbol	I/O	Function
2	Break acknowledge output	$\overline{BR\text{-}AK}$	O	A signal is output to indicate that the D6380 operation has been interrupted. This signal is set with an instruction (BRAKST instruction). This signal is used in the emulator mode.
44	Data output request	$\overline{DO\text{-}RQ}$	I	A data output request signal is input from the DO2 pin in the D6380 emulation mode.
47	Overflow output	$\overline{OVF}$	O	A signal is output to indicate that overflow compensation has been made in the D6380. An N-channel open drain pin.
45	General flag output	$\overline{GF}$	O	The contents of the most significant bit of the loop counter in the D6380 are output. The G-flag is set/reset with an instruction.
40	Data input 1	DI1	I	An audio signal serial input pin.
42	Data input 2	DI2	I	
41	Data output 1	DO1	O	An audio signal serial output pin
43	Data output 2	DO2	O	
36	Bit clock input 1	BCLK1	I	Bit clock signals are input for the signals input/output via DI1, DI2, DO1, and DO2. Either BCLK1 or BCLK2 is selected by a control register. (Slave mode)
38	Bit clock input 2	BCLK2	I	
37	LR clock input 1	LRCK1	I	Signals are input to specify L- and R-channels for the signals input/output via DI1, DI2, DO1, and DO2. Either LRCK1 or LRCK2 is selected by a control register. (Slave mode)
39	LR clock input 2	LRCK2	I	

Pin No.	Pin name	Symbol	I/O	Function
27	External RAM address output 7	A7	O	External RAM (for digital delay) addresses are output. A7 is the MSB and A0 is the LSB. Row and column addresses are output.
26	External RAM address output 6	A6		
25	External RAM address output 5	A5		
24	External RAM address output 4	A4		
23	External RAM address output 3	A3		
22	External RAM address output 2	A2		
21	External RAM address output 1	A1		
19	External RAM address output 0	A0		
35	External RAM data input/output 4	I/O4	I/O	External RAM (for digital delay) data is input/output. To send 16-bit data, 4-bit data is sent four times.
34	External RAM data input/output 3	I/O3		
32	External RAM data input/output 2	I/O2		
31	External RAM data input/output 1	I/O1		
30	External RAM write enable	$\overline{WE}$	O	An external RAM (for digital delay) write enable signal is output.
29	External column address strobe output	$\overline{CAS}$	O	An external RAM (for digital delay) column address strobe signal is output.
28	External RAM low address strobe is output	$\overline{RAS}$	O	An external RAM (for digital delay) low address strobe signal is output.

Pin No.	Pin name	Symbol	I/O	Function
13	X-time fs output	XFsO	O	A control signal such as ADC and DAC is output. The D6380 master clock is divided to be output. The division ratio is specified by the control register.
12	Bit clock output	BCLKO	O	A control bit clock such as ADC and DAC is output. When the master mode is set, this clock is used as a bit clock signal.
10	LR clock output	LRCKO	O	A control LR clock signal such as ADC and DAC is output. When the master mode is set, this signal is used as an LR clock.
11	Word clock output	WCKLO	O	A control word clock signal such as ADC and DAC is output. The LRCKO signal is generated by dividing this signal into two halves.
9	Aperture R output	APTRO	O	A signal is output to specify sampling and holding of the right analog output for the DAC and so forth.
8	Aperture L output	APTLO	O	A signal is output to specify sampling and holding of the left analog output for the DAC and so forth.

2. INTERNAL FUNCTIONS

(1) Instruction RAM (I-RAM)

This RAM is used to store a program. It consists of 192 x 22 bits. The instruction RAM address is specified by the program counter (PC).

A program is transferred from the instruction RAM via the host CPU interface block (μC-IF).

(2) Program counter (PC)

This register is used to determine an instruction RAM address. Generally, the contents of this register are incremented each time an instruction is fetched. For a jump or subroutine call instruction, the value in the NEXT ADDRESS field of the instruction is transferred to this register. For a subroutine return instruction, the value of the stack register is transferred to this register. The PC value is cleared to 0s by Fs-RST (generated at the rising edge of LRCK in the normal mode or when Fs-RST is input in the emulator mode).

(3) Stack (STACK)

This register is used to store the return address of a subroutine call instruction. When a subroutine return instruction is executed, the contents of this register are read and transferred to the PC. There are only stack level, that is, nesting is inhibited.

(4) Host CPU interface (μC-IF)

This block provides a serial interface between the external host CPU and μD6380. It consists of an 8-bit shift register and a latch for storing the received data.

When data transfer specified by the host CPU is completed, a rewrite request flag is set to rewrite the instruction RAM (I-RAM) or control register (CNT-R). Also, the external read register (EXT-R) or program counter may be read.

(5) External read register (EXT-R)

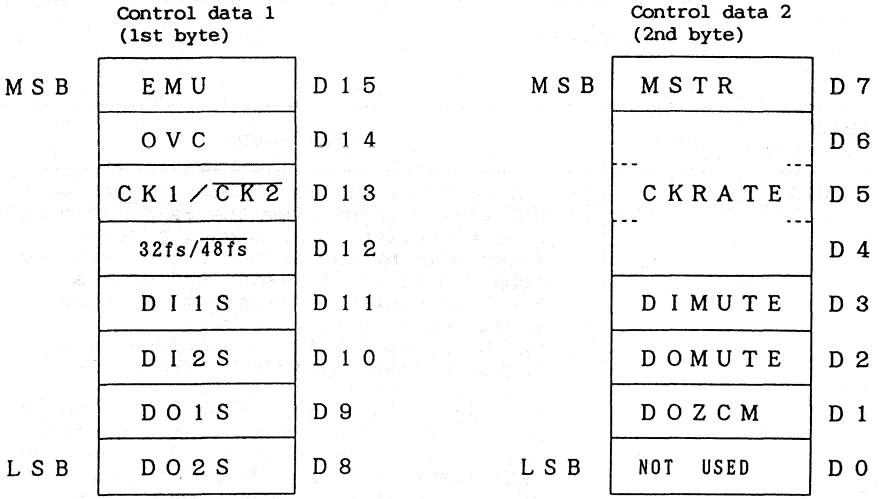
This is an 8-bit register for reading the internal state of the μPD6380. The low-order 8-bit data of the internal data bus (IDB) is transferred to this register. The host CPU can issue a REG RD. command to read the contents of this register directly via the μC-IF block.

(6) Control register (CNT-R)

This register is used to specify the μPD6380 operation mode. The host CPU issues a REG WR. command to set an operation mode value via the μC-IF block.

The control register consists of 16 bits. The host CPU divides the contents of the control register into two halves (8 bits each) to be transferred; however, the control register of the μPD6380 are rewritten after the all contents (16 bits) of the control register have been transferred.

(a) Control register bit layout



(b) Control register functions

Note: The number marked with ◯ is the default after resetting.

Bit position	Name	Function
D15	EMU	①: The D6380 is set in the emulation mode. The signal input from the $\overline{\text{Fs-RST}}$ pin is made effective. The signal generated internally by the signal input from the LRCK1/LRCK2 pin is made ineffective. The host system set the timing of Fs resetting in this register. 0: The D6380 is set in the normal audio signal processing mode. (The emulation mode is reset.) The signal input from the $\overline{\text{Fs-RST}}$ pin is made ineffective. The signal generated internally by the signal input from the LRCK1/LRCK2 pin is made effective. The host system set the timing of Fs resetting in this register. Note: See Chapter 6 "Emulation Mode" for details on the emulation mode.
D14	OVC	1: Overflow compensation is made. ⓪: Overflow compensation is not made.
D13	CK1/$\overline{\text{CK2}}$	①: LRCK1 and BCLK1 are selected as input pins. 0: LRCK2 and BCLK2 are selected as input pins.
D12	32fs/$\overline{\text{48fs}}$	①: The number of bit clocks per channel is set to 16. (Bit clock frequency = 32 fs) 0: The number of bit clocks per channel is set to 24. (Bit clock frequency = 48 fs)
D11	DI1S	①: 32fs/$\overline{\text{48fs}}$ = 0 Of the data input from the D11 pin, 16 bits are effective per channel. 0: 32fs/$\overline{\text{48fs}}$ = 0 Of the data input from the D11 pin, 19 bits are effective per channel. Note: When 32fs/$\overline{\text{48fs}}$ = 1, 16 bits are forcibly made effective per channel.

Bit position	Name	Function
D10	DI2S	①: 32fs/$\overline{48fs}$ = 0 Of the data input from the D12 pin, 16 bits are effective per channel. 0: 32fs/$\overline{48fs}$ = 0 Of the data input from the D12 pin, 19 bits are effective per channel. Note: When 32fs/$\overline{48fs}$ = 1, 16 bits are forcibly made effective per channel.
D9	DO1S	①: 32fs/$\overline{48fs}$ = 0 Of the data input from the 01 pin, 16 bits are effective per channel. 0: 32fs/$\overline{48fs}$ = 0 Of the data input from the DO1 pin, 19 bits are effective per channel. Note: When 32fs/$\overline{48fs}$ = 1, 16 bits are forcibly made effective per channel.
D8	DO2S	①: 32fs/$\overline{48fs}$ = 0 Of the data input from the DO2 pin, 16 bits are effective per channel. 0: 32fs/$\overline{48fs}$ = 0 Of the data input from the DO2 pin, 19 bits are effective per channel. Note: When 32fs/$\overline{48fs}$ = 1, 16 bits are forcibly made effective per channel.
D7	MSTR	1: The D6380 is set in the master mode. Output signals BCLK0, WCLK0, LRCK0, and APTL0, APTR0 are generated by dividing the master clock respectively. ⓪: The D6380 is set in the slave mode. The signal input from the BCLK1/BCLK2 pin is directly output as the BCLK0 signal. The signal input from the LRCK1/LRCK2 pin is directly output as the LRCK0 signal. Since output signals WCLK0, APTL0, and APTR0 are generated by the BCLK0 signal, they are synchronized with BCLK1/BCLK2.

<table>
<tr><th>Bit position</th><th>Name</th><th>Function</th></tr>
<tr><td>D6
D5
D4</td><td>CKRATE</td><td>When MSTR = 1, clock rates of output signals XfsO, BCLKO, WCLKO, LRCKO, APTRO, and APTLO are specified.
<table>
<tr><th rowspan="2">D6</th><th rowspan="2">D5</th><th rowspan="2">D4</th><th colspan="3">Frequency division rate with reference to master clock frequency</th></tr>
<tr><th>XfsO</th><th>LRCKO</th><th>BCLKO</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>(*1)</td><td>512</td><td>16</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4</td><td>512</td><td>16</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td><td>512</td><td>16</td></tr>
<tr><td>⓪</td><td>①</td><td>①</td><td>1</td><td>512</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>(*1)</td><td>768</td><td>16 or 24(*2)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td><td>768</td><td>16 or 24(*2)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>3</td><td>768</td><td>16 or 24(*2)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3 or 2</td><td>768</td><td>16 or 24(*2)</td></tr>
</table>
*1: Clock signals are not output.
*2: When 32fs/$\overline{48fs}$ = 0, the division ratio is 1:16.
When 32fs/$\overline{48fs}$ = 1, the division ratio is 1:24.</td></tr>
<tr><td>D3</td><td>DIMUTE</td><td>①: Signals input to DI1 and DI2 pins are muted. The muting start timing is synchronized with Fs-RST.
0: Signals input to DI1 and DI2 pins are not muted.</td></tr>
<tr><td>D2</td><td>DOMUTE</td><td>①: Signals output from DO1 and DO2 pins are muted. Muting starts at the first edge of the LR clock.
0: Signals output from DO1 and DO2 pins are not muted.</td></tr>
<tr><td>D1</td><td>DOZCM (DO1 only)</td><td>Zero-cross muting is carried out irrespective of DOMUTE.
1: Zero-cross muting is started separately for the left and right outputs at the time of data zero-crossing.
⓪: Zero-cross muting is not carried out. Muting is canceled separately for the left and right outputs at the time of data zero-crossing.</td></tr>
<tr><td>D0</td><td></td><td>(Reserved)</td></tr>
</table>

(7) Data RAM (D-RAM)

This RAM is used to store data. It consists of 128 words x 19 bits. The RAM address is specified by the data pointer (DP). Data may be transferred between this RAM and internal data bus. Moreover, AccL data can be input in the data RAM directly.

(8) Data pointer (DP)

This register is used to specify a RAM address. DPL (low-order four bits) is an UP/DOWN that can be incremented, decremented, or reset. One of these functions can be reset with the corresponding instruction. DPH (high-order 3 bits) sets the 3-bit data in the DPH-M field of the instruction; it may be qualified through exclusive OR.

If an FIR mode is specified with an LDC instruction, DPH (high-order three bits) and DPL (low-order four bits) operate as one UP counter. If the 7-bit counter matches the value of PR2 (preset register 2) given in item (9), the value of PR1 (preset register 1) is set in this counter at the next incrementation.

Thus, loop counting from the PR1 value to the PR2 value is enabled.

(9) Preset register (PR)

This register is used to set DP loop counting start and end addresses in the FIR mode. The FIR mode is selected when an immediate data load instruction (LDC instruction) is issued to this PR and it is canceled when a DPL clear instruction is issued.

(10) Coefficient RAM (C-RAM)

The main purpose of this RAM is to store coefficient data. It consists of 128 words x 16 bits. Data transferred between this RAM and internal data bus. Moreover, data can be transferred to the K-input register of the multiplier directly.

(11) C-RAM pointer (CP)

This register is used to specify the C-RAM address. It consists of a 7-bit up-counter. It is incremented (by 1) by a CPINC instruction.

(12) Multiplier

This is a parallel multiplier, based on the secondary booth algorithm, that multiplies data consisting of 19 bits x 16 bits (representing a 2's complement). Its output consists of a sign bit and 30 data bits. The multiplication result is represented by 34 bits; however, low-order three bits are ignored.

The multiplication result can be referenced by reading the M-register in the instruction cycle that follows the instruction cycle in which data was set in the K- and L-registers.

(13) M-register

This register consists of 31 bits for setting the multiplication result. The contents of this register become the P-input data of the ALU.

(14) ALU

This unit is used for arithmetic logical operation. The following operations are performed between the P-input data and Acc data. Three bits with sign extension are added to the P-input data as an overhead margin.

- o NOP
- o ADD
- o SUB
- o AND
- o OR
- o Addition of 1 to AccH
- o Subtraction of 1 from AccH
- o Shifting 1 bit to the right
- o Shifting 1 bit to the left
- o ABS (absolute value)
- o Acc clear
- o Comparison
- o 2's complement
- o 19-bit rounding
- o 16-bit rounding

(15) Accumulator (Acc)

This register is used to store the ALU operation result. It consists of AccH (high-order 22 bits) and AccL (low-order 12 bits). AccH has three bits with sign extension as an overflow margin.

(16) Shifter (SHIFT)

The following shift operations are performed:

- o The M-register or the data from Acc is shifted 18 or 14 bits to the right or one bit to the left.
- o The data from IDB (data bus) is shifted 1 bit to the right or left.

(17) Flag (FLAG)

This register sets the flag that is qualified by the result of ALU operation.

- o S (Sine flag):
  Indicates the sign of the operation result.
- o Z (Zero flag):
  Indicates that the AccH operation result is zero.
- o OVF (Overflow flag):
  Indicates that the overflow result has overflowed.

(18) Overflow automatic compensation (OVC, OVC')

Overflow is automatically recovered by setting the OVC bit of the control register.

Overflow is compensated in two cases. When the overflow margin (three extended sign bits) of the accumulator is exceeded as the result of ALU operation or the data overflowed as result of accumulator operation is dumped to 19 IDB bits, the positive maximum value (01111...111) or negative maximum value (10000...000) is set automatically.

(19) External RAM control block

The external RAM control block is used to control the 256K DRAM (4-bit parallel I/O) connected externally. The μPD6380 can write 16-bit data into the 256K DRAM with an EXR instruction. It can also read 16-bit data from the external 256K DRAM.

Eight instructions cycles are required to read or write data; however, the hardware automatically sends/receives data after the EXR instruction is issued, that is, another processing may be performed while the external RAM is being accessed.

The delay time can be specified by writing a relative address in the read offset register. Use of this SLI chip realizes stereo delay (44.1 kHz sampling) of up to 10 channels.

(20) Loop counter (LC)

This is an 8-bit register having an incrementer. It is incremented with an instruction.

The MSB is called a general flag (G); it can be set, reset, or toggled (inverted) independently. The value of the G flag provides a condition with the conditional jump instruction.

(21) Temporary register (TR1, TR2)

The TR1/TR2 is a 19-bit general register that is used to latch data temporary. It is connected to the internal data bus.

3. HOST CPU TRANSFER COMMAND

The host CPU issues a host CPU transfer command to transfer data to/from the μPD6380. There are eight types of host CPU transfer commands. For further details on the data transfer method, refer to the User's Manual (IEU-652).

Transfer commands

	Command bit allocation
INST WR.	xxxxx001
Co WR.	xxxxx010
EX RQ.	xxxxx011
REG WR.	xxxxx100
REG RD.	xxxxx101
PC RD.	xxxxx110

3.1 Instruction Write Command (INST WR.)

An INST WR. command consists of at least five bytes.

① Command byte
② Program counter
③ Instruction bits #21 to #16 (high-order two bits are dummy.)
④ Instruction bits #15 to #8
⑤ Instruction bits #7 to #0

The next data can be sent by repeating ③ to ⑤.

This command is used to transfer a 22-bit instruction, one word of the instruction RAM, from the controller to the μPD6380.

3.2 Coefficient Write Command (CO WR.)

A coefficient write command consists of at least four bytes.

① Command byte
② Program counter value
③ High-order eight bits of coefficient data
④ Low-order eight bits of coefficient data

The next data can be sent by repeating ③ and ④. With this command, the host CPU can write data into the coefficient RAM effectively and easily.

The μPD6380 automatically generates an "LDA CRAM coefficient data" instruction according to the 16-bit data sent by ③ and ④ above.

The bits of the data sent by ③ and ④ must be rearranged as shown below.

Actual 16-Bit Data

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

Transferred data

③

D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5

④

D 4	D 3	D 2	D 1	D 0	D 15	D 14	D 13

4

3.3 Execution Request (EX-RQ)

This command consists of one byte (command byte).

If this command is decoded in the μC-IF block, the hardware generates the pattern of the remaining 14 bits for the instruction address latched in the μC-IF block and automatically generates an instruction for jumping to its own address unconditionally.

Then, this unconditional jump instruction is written into the I-RAM (storing the program counter value latched in the μC-IF). When this instruction is executed, the μPD6380 enters the HLT state.

When this conditional jump instruction is written into the instruction RAM, the ERQ flag (EX RQ command issue flag)is set. When the unconditional jump instruction is executed, the ERQ flag is reset.

3.4 Control Register Write Command (REG WR.)

This command consists of three bytes.

① Command byte
② Control data 1
③ Control data 2

This instruction is used to transfer data to the CNT-R (control register) in the μPD6380. The CNT-R is a 16-bit register that determines the μPD6380 operation.

3.5 External Register Read Command (REG RD.)

This command consists of two bytes.

① Command byte
② [Data]

This instruction is used to transfer the value of the EXT-R (external register) to the external controller.

First, command ① is transferred from the CPU to the μPD6380. The μPD6380 decodes this command and transfers the EXT-R data to the shift register in the μC-IF block in the μC-IF block immediately.

Then, the data set in the shift register is output to the SO line in synchronization with eight clock pulses output from the host CPU.

3.6 Program Counter Read Command (PC RD.)

① Command byte

② [Data]

This command is used to read PC data like the REG RD. command.

4. INSTRUCTIONS

One μPD6380 instruction consists of 22 bits. All μPD6380 instructions are 1-word instructions and they are classified into nine types.

OPA instruction:

This instruction performs the following controls in parallel, including control of multiplication and addition which are basic operations of the digital filter:

- o Control of shifter for pseudo double-precision operation
- o ALU control
- o ALU-P input selection
- o Data transfer between registers (including memory)
- o Data RAM (D-RAM) address control
- o Coefficient RAM (C-RAM) address control

RET instruction:

This instruction specifies return from a subroutine and perform the same processing as that of the OPA instruction.

LDA instruction:

This instruction loads 16-bit immediate data or input 16-bit immediate data to ALU (P-input) to perform arithmetic operations between Acc and data. It is mainly used for rewriting the contents of the coefficient RAM. In the emulator mode, this instruction is used as an LDE instruction.

LDB instruction:

This instruction controls conditional loading of 8-bit immediate data. It is mainly used to specify the coefficient or data RAM address.

JMP instruction:

This instruction executes conditional jump instructions including a subroutine call instruction.

OPB:

This instruction carries out a simple conditional operation and transfers data between registers simultaneously.

LDC:

This instruction loads 14-bit immediate data. It is used when the FIR mode is selected or when an external address must be set.

EXR instruction:

This instruction controls the external RAM.

LDE instruction:

This instruction loads 19-bit immediate data. It is used to transfer data in the emulation mode.

4.1 OPA Instruction

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPA	0	1	ALU1				PSEL	CPINC	DP_H.M			DP_L1		DST 1					SRC			

(1) ALU1 field

This field specifies an ALU operation type. There are 15 operation types.

(2) PSEL field

This field is used to select ALU (P-input), that is, it selects an internal data bus or M-register.

(3) CPINC filed

This field specifies incrementation of the CP (C-RAM) pointer value.

(4) DPH·M

The value of high-order three bits of the DP (data pointer) is exclusively ORed with the value of this field to change the pointer value. The new DPH value is effective for the subsequent instructions.

(5) DPL1 field

This field specifies the value of low-order four bits of the data pointer. The specified DPL value is effective for the subsequent instructions.

6) DST1 field

This field specifies the destination register for a transfer instruction. There are 15 types of destination registers.

(7) SRC field

This field specifies the source register for a transfer instruction. There are 14 types of source registers.

4.2 RET Instruction Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RET	0	1	ALU1				PSEL	CPINC	$DP_H.M$			DP_L1		DST 1					SRC			

This function of this instruction is the same as that of the OPA instruction except return from a subroutine. Control is returned from a subroutine when the PC data saved in the stack register with a subroutine call instruction returns to the PC.

4.3 LDA Instruction Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LDA	1	0	ALU2		DST2		IMMMEDIATE DATA 1 (16BIT)															

The LDA instruction is mainly used for loading a filter coefficient. It is also used for loading 16-bit immediate data and performing simple operations.

(1) ALU2 field

This field indicates the type of operation which is performed between 16-bit immediate data 1 transferred through the IDB and Acc. This field is made effective when ALU2 is specified in DST2.

(2) DST2 field

This field indicates the memory or register to which immediate data 1 is to be transferred.

(3) Immediate data 1

This field stores 16-bit immediate data. It is mainly used for loading filter coefficient data.

4.4 LDB Coefficient Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LDB	1	1	1	0	COND						DST 3				IMMEDIATE DATA 2 (8BIT)							

The LDB instruction transfers 8-bit data from the immediate data 2 field to the register indicated by the DST3 field when the condition indicated by the COND field is satisfied. It is mainly used for loading a D-RAM or C-RAM pointer.

(1) COND field

A condition is set for the conditional transfer instruction. (The CALL instruction is not effective.)

(2) DST3 field

This field indicates the register to which 8-bit immediate data 2 is to be transferred.

(3) Immediate data 2

This field stores 8-bit immediate data. It is mainly used for loading a D-RAM or C-RAM pointer.

4.5 JMP Instruction Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
JMP	1	1	1	1	COND					OP				DPL2	NA (8BIT)							

The JMP instruction performs the operation indicated by the OP field when the condition indicated by the COND field is satisfied. It also transfers data from the NA field to the PC (program counter), then jumps to the specified address.

(1) COND field

This field indicates a condition for the conditional jump & operation instruction.

(2) OP field

This field indicates the operation to be performed before jumping to the specified address when the specified condition is satisfied.

(3) DPL2

This field specifies incrementation of the DPL irrespective of the condition indicated by the COND field.

(4) NA

This field indicates the jump destination address when the specified condition is satisfied.

4.6 OPB Instruction Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPB	1	1	0	1	COND					OP				DPL2	DST 4				SRC			

The OPB instruction performs the operation indicated by the OP field when the condition indicated by the COND field is satisfied.

(1) COND

This field indicates a condition for the conditional jump & operation instruction. (The CALL instruction is not effective.)

(2) OP

This field indicates the operation to be performed when the specified condition is satisfied.

(3) DPL2

This field specifies incrementation of the DPL irrespective of the condition indicated by the COND field.

(4) DST4

This field indicates the destination of transfer that is carried out irrespective of the condition indicated by the COND field.

(5) SRC

This field specifies a source register among 14 types of registers.

4.7 LDC Instruction Structure

Instruction	21 20 19 18 17	16 15 14	13 12 11 10 09 08 07 06 05 04 03 02 01 00
LDC	1 1 0 0 0	DST5	IMMEDIATE DATA 3 (14BIT)

This instruction loads 14-bit immediate data. It selects an FIR mode and sets an external delay RAM address.

(1) DST5

This field indicates the register to which 14-bit immediate data 3 is to be transferred.

(2) Immediate data 3

This field sets 14-bit immediate data. It sets the preset register value in the preset register value and external delay RAM address.

4.8 EXR Instruction Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXR	1	1	0	0	1	SC					MODE				DST 1				SRC			

This instruction controls the external delay RAM for digital delay.

(1) SC field

This field indicates one of five registers, write address register and read offset registers 0-3.

(2) MODE field

This register controls data writing into the external RAM, data reading from the external RAM, and data transfer to each register.

(3) DST1 field

This field indicates the register to which data is to be transferred.

(4) SRC field

This field indicates the source of the data to be transferred.

4.9 LED Instruction Structure

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LDE	1	0	DST6	IMMEDIATE DATA 4 3BIT			IMMEDATE DATA 5 16BIT														(DATA4 + DATA5=19BIT)	

This instruction is made effective instead of the LDA instruction in the emulator mode (EMU bit of control register = 1). It is used to transfer 19-bit immediate data; it is not used generally.

(1) DST6 field

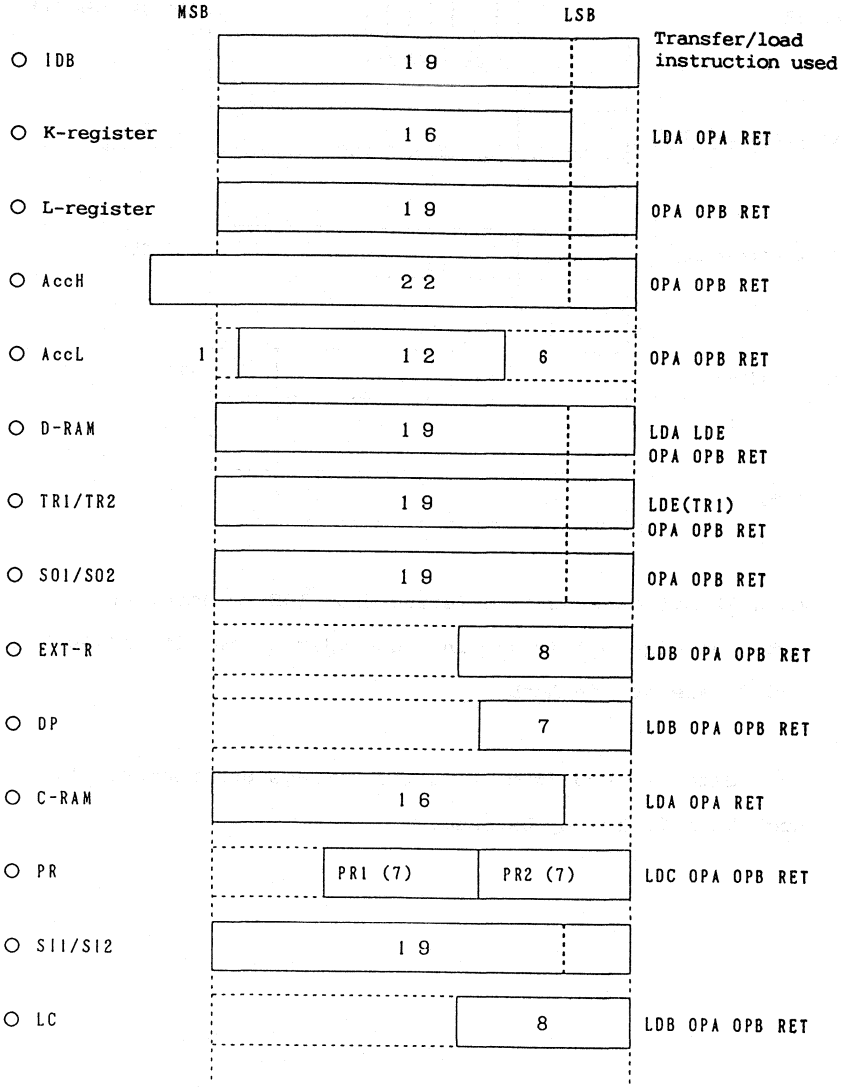
This field indicates the register to which data is to be transferred.

(2) Immediate data fields 4 and 5

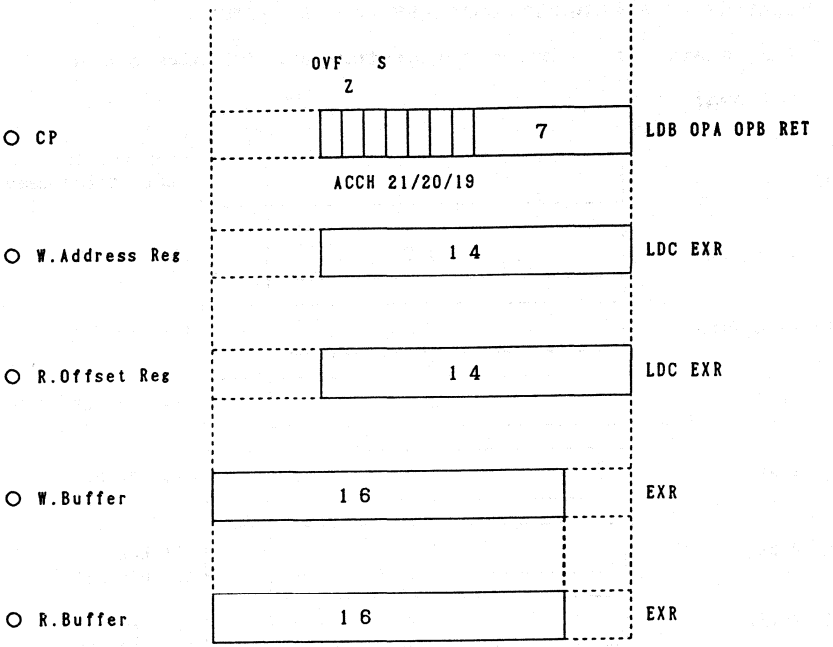
These fields set 19-bit immediate data.

5. RELATIONSHIPS BETWEEN REGISTERS AND IDB BITS

The relationships between registers and IDB bits are as follows:



····· LSB positions of external 16-bit data



When 22-bit data is transferred from IDB to AccH, an extended sign bit is set in high-order three bits of AccH and Os are set in AccL.

When data is read from CP is read, flags and contents of AccH bits 21-19 may be read.

6. INSTRUCTION CODES

Instruction	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPA	0	0	ALU1				PSEL	CPINC	$DP_H.M$			DP_L1		DST 1			SRC					
RET	0	1	ALU1				PSEL	CPINC	$DP_H.M$			DP_L1		DST 1			SRC					
LDA	1	0	ALU2		DST2		IMMMEDIATE DATA 1 (16BIT)															
LDB	1	1	1	0	COND				DST 3					IMMEDIATE DATA 2 (8BIT)								
JMP	1	1	1	1	COND				OP				DPL2	NA (8BIT)								
OPB	1	1	0	1	COND				OP				DPL2	DST 4			SRC					
LDC	1	1	0	0	0	DST5	IMMEDIATE DATA 3 (14BIT)															
EXR	1	1	0	0	1	SC			MODE			DST 1					SRC					
LDE	1	0	DST6	IMMEDIATE DATA 4			IMMEDATE DATA 5 (DATA4 + DATA5) 19BIT															

Note: The LDE instruction is valid only in the emulation mode.

OP Field

Mnemonic	P 12	P 11	P 10	P 09	Operation
NOP	0	0	0	0	No operation
GFTG	0	0	0	1	G-flag toggling
GFST	0	0	1	0	G-flag setting
GFRST	0	0	1	1	G-flag resetting
LCINC	0	1	0	0	LC incrementation
DPLINC	0	1	0	1	DPL incrementation
DPLDEC	0	1	1	0	DPL decrementation
CPINC	0	1	1	1	CP incrementation
UCHDL	1	1	0	1	Start of writing from μC-IF
ERQFRST	1	1	1	0	ERQF flag resetting
BRAKST	1	1	1	1	BRAK flag setting
COMP2	1	0	0	0	(Acc) ← 2's complement
RND16	1	0	0	1	(Acc) ← 16-bit rounding
RND19	1	0	1	0	(Acc) ← 19 bit rounding
ACHINC	1	0	1	1	(Acc) ← (AccH) + 1
ACHDEC	1	1	0	0	(Acc) ← (AccH) - 1

ALU1 Field

Mnemonic	P 19	P 18	P 17	P 16	Operation	Flag operation S	Z	OVF
NOP	0	0	0	0	No operation	●	●	●
OR	0	0	0	1	(Acc) ← (Acc) ∪ (P)	↓	↓	↓
AND	1	1	0	1	(Acc) ← (Acc) ∩ (P)	↓	↓	↓
CLR	0	0	1	1	(Acc) ← ZERO	0	1	0
ADD	1	0	0	1	(Acc) ← (Acc) + (P)	↓	↓	↓
AR18	1	0	0	0	(Acc) ← (Acc) + (P SHR 18)	↓	↓	↓
AR14	1	0	1	0	(Acc) ← (Acc) + (P SHR 14)	↓	↓	↓
AL1	1	0	1	1	(Acc) ← (Acc) + (P SHL 1)	↓	↓	↓
RND19	1	1	0	0	(Acc) ← (Acc) 19-bit rounding	↓	↓	↓
ACHINC	1	1	1	0	(AccH) ← (AccH) + 1	↓	↓	↓
ACHDEC	1	1	1	1	(AccH) ← (AccH) - 1	↓	↓	↓
ABS	0	1	1	1	(Acc) ← Absolute value (Acc)	0	●	↓
SUB	0	1	0	0	(Acc) ← (Acc) - (P)	↓	↓	↓
CMP	0	1	0	1	(Acc) - (P)	↓	↓	↓
SHR1	0	1	1	0	(Acc) ← (Acc) 1-bit shift to the right	●	↓	↓
SHL1	0	0	1	0	(Acc) ← (Acc) 1-bit shift to the left	↓	↓	↓

●: The previous state is maintained.

↓: The operation is affected by the operation result.

0: The flag is cleared to 0s.

ALU2 Field

Mnemonic	P 19	P 18	Operation	Flag operation		
				S	Z	OVF
OR	0	0	(Acc) ← (Acc) + (P)	↓	↓	↓
CMP	0	1	(Acc) - (P)	↓	↓	↓
ADD	1	0	(Acc) ← (Acc) + (P)	↓	↓	↓
AND	1	1	(Acc) ← (Acc) - (P)	↓	↓	↓

↓: The operation is affected by the operation result.

DP_H·M Field

Mnemonic	P 13	P 12	P 11	Operation
M0	0	0	0	(DP6,DP5,DP4) ∀ (0,0,0) → (DP6,DP5,DP4)
M1	0	0	1	(DP6,DP5,DP4) ∀ (0,0,1) → (DP6,DP5,DP4)
M2	0	1	0	(DP6,DP5,DP4) ∀ (0,1,0) → (DP6,DP5,DP4)
M3	0	1	1	(DP6,DP5,DP4) ∀ (0,1,1) → (DP6,DP5,DP4)
M4	1	0	0	(DP6,DP5,DP4) ∀ (1,0,0) → (DP6,DP5,DP4)
M5	1	0	1	(DP6,DP5,DP4) ∀ (1,0,1) → (DP6,DP5,DP4)
M6	1	1	0	(DP6,DP5,DP4) ∀ (1,1,0) → (DP6,DP5,DP4)
M7	1	1	1	(DP6,DP5,DP4) ∀ (1,1,1) → (DP6,DP5,DP4)

DP_L1 Field

Mnemonic	P 10	P 09	Operation
DPNOP	0	0	No operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

DP_L2 Field

Mnemonic	P 08	Operation
DPNOP	0	No operation
DPINC	1	Increment DP_L

DST1 Field

Mnemonic	P 08	P 07	P 06	P 05	P 04	Specified register
MPLY	1	0	0	0	0	IDB → Lreg, C-RAM → Kreg
MPDR	1	0	0	0	1	IDB → Lreg & D-RAM, C-RAM → Kreg
MPT1	1	0	0	1	0	IDB → Lreg & TR1reg, C-RAM → Kreg
MPT2	1	0	0	1	1	IDB → Lreg & TR2reg, C-RAM → Kreg
DRAD	1	1	1	0	1	IDB → D-RAM (DP5=0), AccL → D-RAM (DP5=1)
L	0	1	0	0	0	Lreg
LK	1	1	0	0	0	L & Kreg
K	1	1	0	0	1	Kreg
DRAM	0	0	0	1	1	D-RAM
DRT1	1	1	0	1	0	D-RAM & TR1reg
DRT2	1	1	0	1	1	D-RAM & TR2reg

Mnemonic	P 08	P 07	P 06	P 05	P 04	Specified register
ACCH	0	1	0	1	0	AccHreg
ACCL	0	1	0	1	1	AccLreg
NON	0	0	0	0	0	NON
SO1	0	0	0	1	0	SO1reg
SO2	0	0	1	0	0	SO2reg
DP	0	0	1	0	1	DPreg
CP	0	0	1	1	0	CPreg
CRAM	1	1	1	0	0	C-RAM
LC	0	0	1	1	1	LCreg
EXT	0	1	0	0	1	EXTreg
PR	0	1	1	0	0	PRreg
TR1D1	0	1	1	1	0	TR1reg
TR2D1	0	1	1	1	1	TR2reg

DST2 Field

Mnemonic	P 17	P 16	Specified register
ALUP	1	0	IDB P (The ALU2 field is made effective.)
DRAM	0	1	DP is incremented after data is transferred to D-RAM.
CRAM	0	0	CP is incremented after data is transferred to C-RAM.
K	1	1	Kreg

DST3 Field

Mnemonic	P 11	P 10	Specified register
CP	0	0	CPreg
DP	0	1	DPreg
LC	1	0	LCreg
EXT	1	1	EXTreg

DST4 Field

Mnemonic	P 07	P 06	P 05	P 04	Specified register
L	1	0	0	0	Lreg
DRAM	0	0	1	1	D-RAM
ACCH	1	0	1	1	AccHreg
ACCL	1	0	1	1	AccLreg
NON	0	0	0	0	NON
SO1	0	0	1	0	SO1reg
SO2	0	1	0	0	SO2reg
DP	0	1	0	1	DPreg
CP	0	1	1	0	CPreg
LC	0	1	1	1	LCreg
EXT	1	0	0	1	EXTreg
PR	1	1	0	0	PRreg
TR1	1	1	1	0	TR1reg
TR2	1	1	1	1	TR2reg

DST5 Field

Mnemonic	P 16	P 15	P 14	Specified register
PR	0	0	0	PRreg (Upper 7 Bit → PR1reg, Lower 7 Bit → PR2reg)
NON	0	0	1	NON
WA	0	1	1	Write address register
RO0	1	0	0	Read offset register 0
RO1	1	0	1	Read offset register 1
RO2	1	1	0	Read offset register 2
RO3	1	1	1	Read offset register 3

DST6 Field

Mnemonic	P 19	Specified register
DRAM	0	D-RAM
TR1	1	TR1reg

SRC Field

Mnemonic	P 03	P 02	P 01	P 00	Specified register
NON	1	1	0	1	NON
SO1	0	0	1	0	SO1 register in EMU mode (usually NON)
ACCH	0	0	0	0	AccHreg
ACCL	0	0	0	1	AccLreg
DRAM	0	0	1	1	D-RAM
CRAM	0	1	0	0	C-RAM
TR1	0	1	0	1	TR1reg
TR2	0	1	1	0	TR2reg
SI1	0	1	1	1	SI1reg
SI2	1	0	0	0	SI2reg
L	1	0	0	1	Lreg
DP	1	0	1	0	DPreg
CP	1	0	1	1	CPreg
PR	1	1	0	0	PRreg
LC	1	1	1	0	LCreg
ZERO	1	1	1	1	Zero (K-register in EMU mode)

SC Field

Mnemonic	P 16	P 15	P 14	Specified register
WA	0	0	0	Write address register
RO0	1	0	0	Read offset register 0
RO1	1	0	1	Read offset register 1
RO2	1	1	0	Read offset register 2
RO3	1	1	1	Read offset register 3

P-SEL Field

Mnemonic	P 15	Operation
IDB	0	Data is tansferred from IDB to the ALU (P-input).
M	1	The M-register data (multiplier output) is tarnsferred to the ALU (P-input).

CP-INC Field

Mnemonic	P 14	Operation
CPNOP	0	No operation
CPINC	1	Increment CP

Mode Field

Mnemonic	P 11	P 10	P 09	Operation
REX	0	0	1	Read buffer ← External RAM
RBU	0	1	0	DST ← Read buffer
MRE	0	1	1	(1) DST ← Read buffer (2) Read buffer ← External RAM
WEX	1	0	0	SRC → Write buffer → External RAM
MWR	1	0	1	(1) SRC → Write buffer → External RAM (2) Read buffer ← External RAM
RAR	1	1	0	Address register (selection by SC) → DST
WAR	1	1	1	Address register (selection by SC) ← SRC

Note: (1) and (2) indicates the execution sequence. The IDB access operation is performed first.

Absolute Maximum Rating

Ta = 25°C

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 - 7.0	V
Input voltage	VI	-0.3 - VDD+0.3	V
Output voltage	VO	-0.3 - VDD+0.3	V
Allowable loss	PD	250	mW
On-bias temperature	Topt	-40 - +85	°C
Storage temperature	Tstg	-55 - +125	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VDD		4.5	5.0	5.5	V
High-level input voltage	VIH		0.7 VDD		VDD	V
Low-level input voltage	VIL		0		0.3 VDD	V
Clock input frequency	fCLK		8	24.576	25.0	MHz

AC Characteristics

Ta = -40 to +85°C V_{DD} = 5.0 V ±10%

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/fall time	tr1	Output pins other than the following output pins			15	ns
	tf2				15	
	tr2	RDY, SO, $\overline{OVF}$ 4.7 kΩ pull-up resistor N-channel open drain pin		80		
	tf2				15	
	tr3	I/O 1 - 4			15	
	tf3				15	
Operating frequency	ftcy		8.0		25.0	MHz

Host CPU Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK high level time	tSCH		250			ns
SCK low level time	tSCL		250			
SCK/SO delay time	tSSD	CL = 15 pF		100	150	
$\overline{CS}$/SO delay time	tCSD	RL = 4.7 k		100	150	
$\overline{C}$/D set-up time	tCDS		100			
$\overline{C}$/D hold time	tCDH		100			
$\overline{CS}$ set-up time	tCSS		100			
$\overline{CS}$ hold time	tCSH		100			
$\overline{CS}$ recovery time	tCSR		360			
SI set-up time	tSIS		100			
SI hold time	tSIH		100			

Audio Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
BCLK0 → LRCK0 delay time	tBLD		0		40	ns
DI1/2 set-up time	tDIS		100			
DI1/2 hold time	tDIH		100			
DO1/2 delay time	tDOD		-40		40	
BCLK1/BCLK2 high level time	tBH		100			
BCLK1/BCLK2 low level time	tBL		100			
LRCK1/LRCK2 high level time	tLH		1			μs
LRCK1/LRCK2 low level time	tLL		1			

External Memory Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Read data hold time	tOFF		0			ns
Low address set-up time	tASR		40			
Low address hold time	tRAH		40			
$\overline{RAS}/\overline{CAS}$ delay time	tRCD			3tcy		
$\overline{CAS}$ pulse width	tCAS		80			
$\overline{CAS}$ access time	tCAC				50	
$\overline{CAS}$ high level time	tCP		50			
Column address set-up time	tASC		40			
$\overline{RAS}$ hold time	tRSH		80			
$\overline{RAS}/\overline{WE}$ delay time	tRWD			70		
Write data set-up time	tDS		30			
Write data hold time	tDH		40			
$\overline{RAS}$ pulse width	tRAS			800		
$\overline{RAS}$ precharge time	tRP		100			
CAS hold time	tCSH		200			
Column address hold time	tCAH		80			

Clock-Related Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK pulse width (high level)	tWHE			20		ns
CLK pulse width (low level)	tWLE			20		
CLK cycle	tCLK		40			
Clock rise/fall	tr4, tf4				15	
CLK → Xfs delay time	tCXD				20	
BCLK1/2 → BCLKO delay time	tBD				20	
LRCK1/2 → LRCKO delay time	tLD				20	
BCLKO → WCLKO delay time	tBWD		0		40	
BCLKO → APTLO delay time	tBALD		0		40	
BCLKO → APTRO delay time	tBARD		0		40	
XFsO → LRCKO delay time	tXLD		0		40	

DC Characteristics

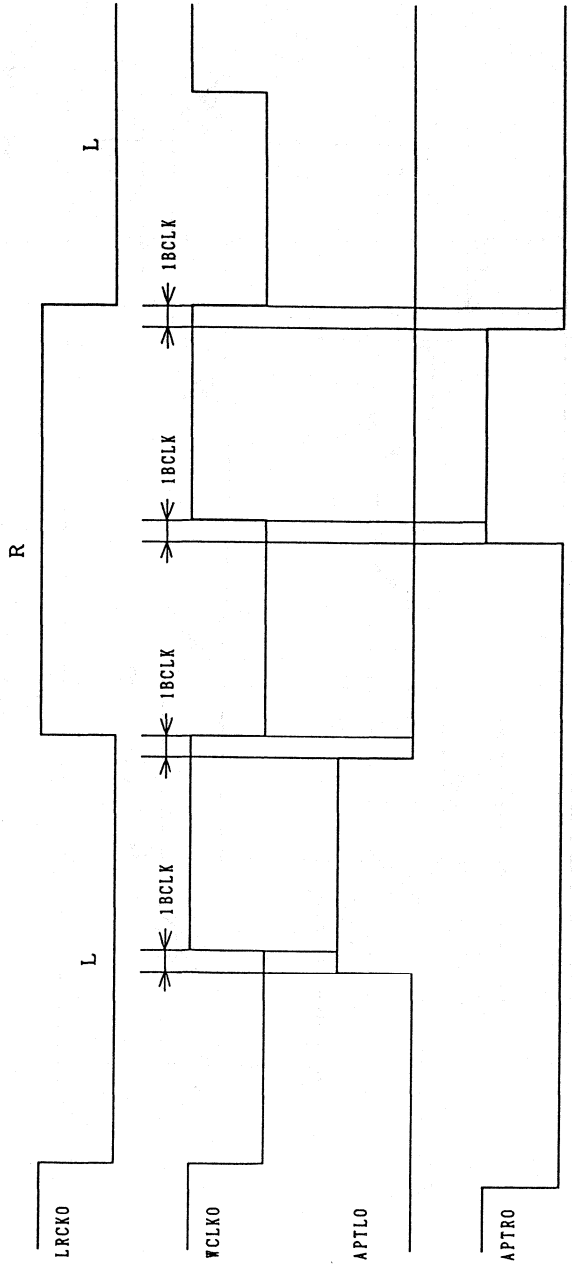
Ta = -40 to +85°C V_{DD} = 5.0 V ±10%

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating supply current		IDD			20		mA
Input voltage	H-level	VP	SI, SCK, C/D, CS, Fs-RST, RST, RST2, D0-RQ, BR-RQ		3.4		V
	L-level	VN			1.5		
Input voltage	H-level	VIH	All pins other than above pins	0.7 VDD		VDD	V
	L-level	VIL		0		0.3 VDD	
Output voltage	H-level	VOH	IOH = -1 mA	VDD -1.0			V
	L-level	VOL	IOH = -1 mA			1.0	
Input leakage	H-level	ILH	VIN = VDD		10		μA
	L-level	ILL	VIN = 0 V		10		

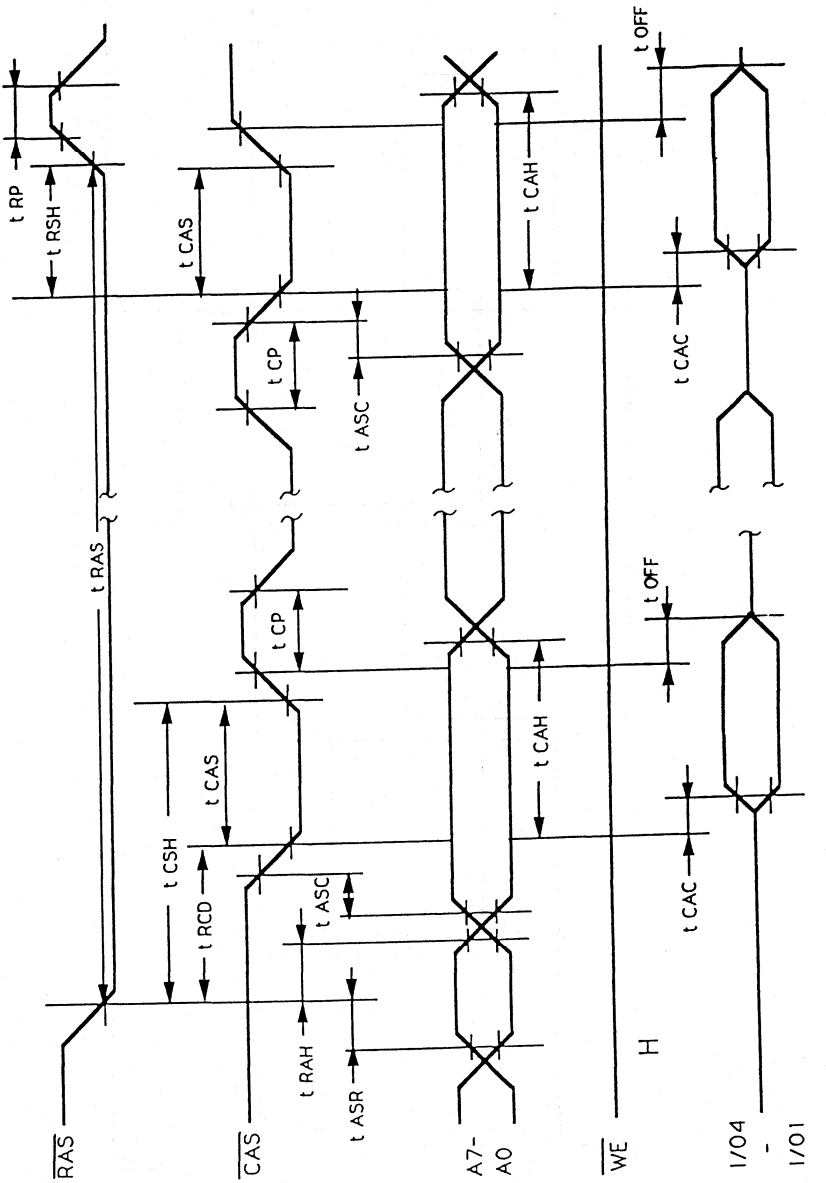
Capacity (Ta = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacity	CIN	fc = 1 MHz			10	pF
Output capacity	COUT	fc = 1 MHz			20	pF

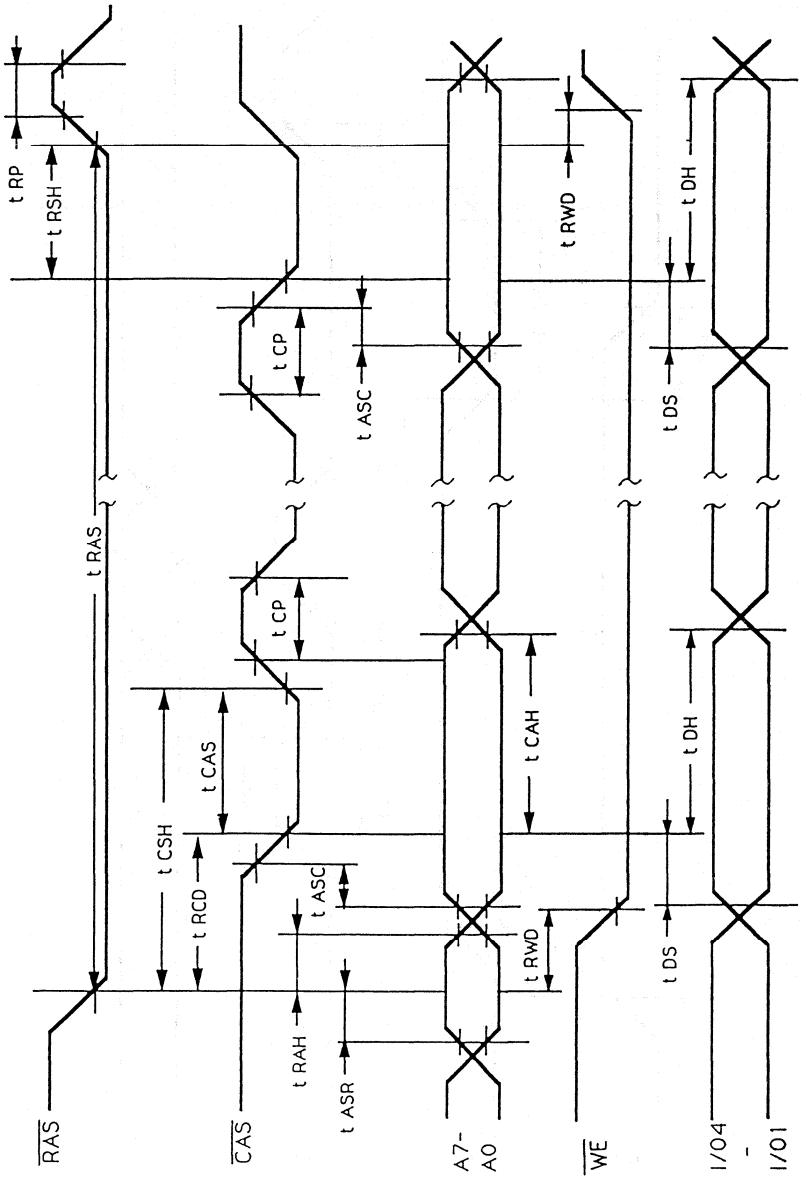
Relationships between LRCKO, WCLKO, APTLO, and APTRO



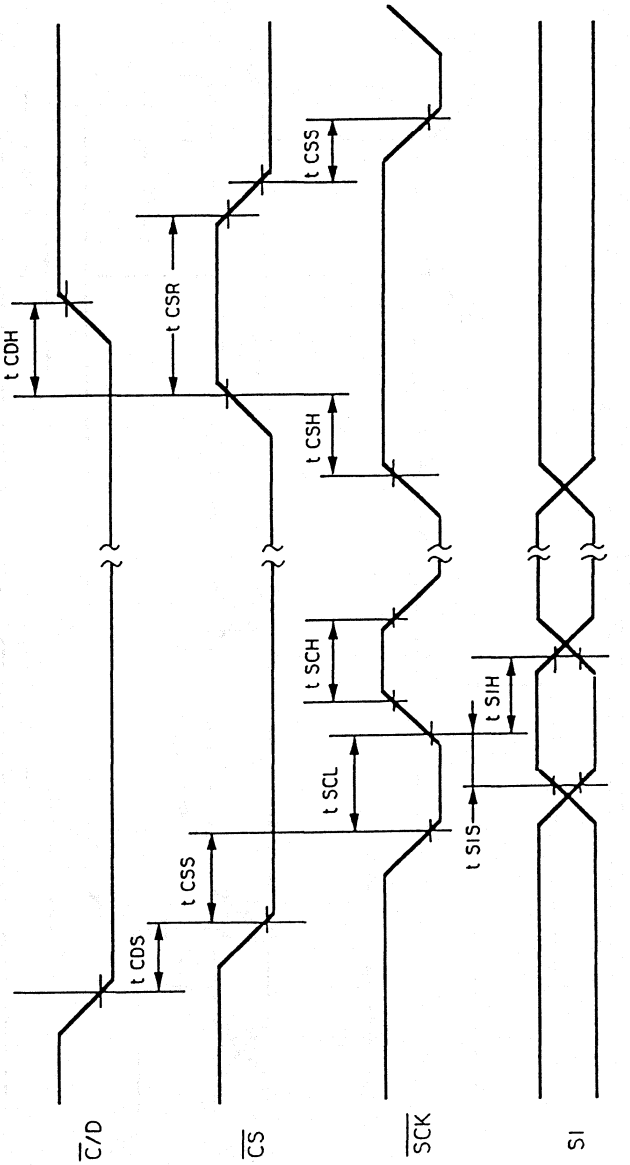
External Memory Timing Chart



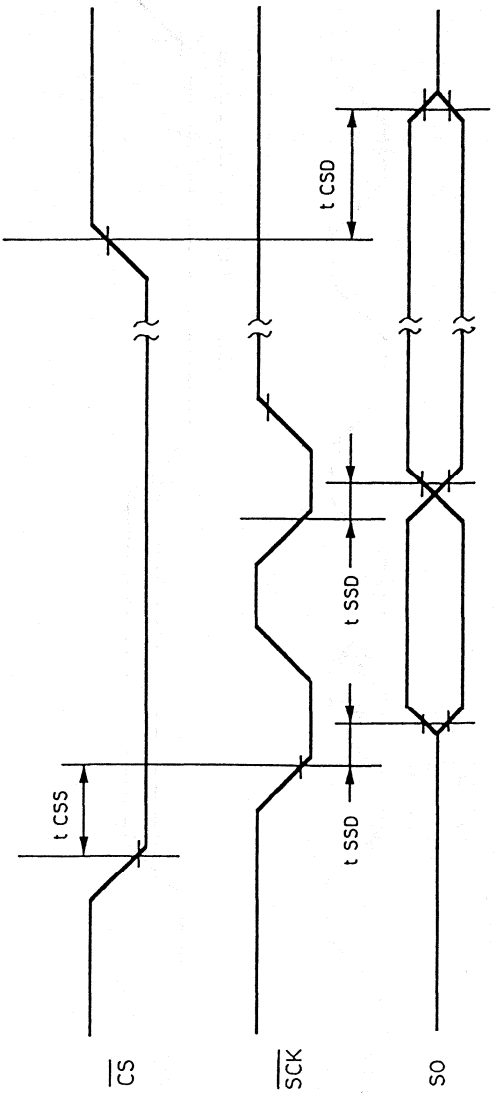
External Memory Write Timing Chart



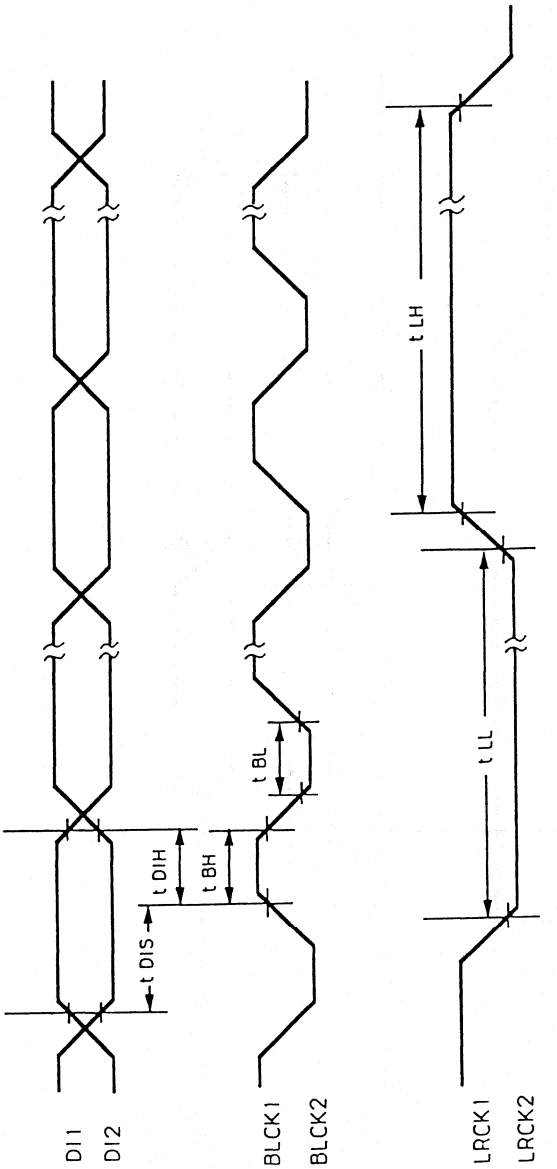
Host CPU Interface Timing Chart (Serial In)



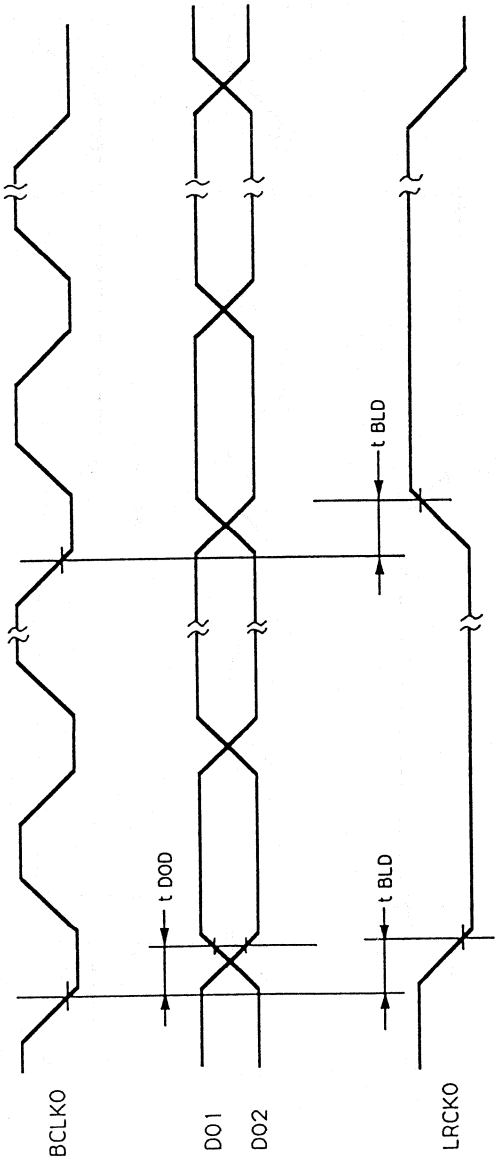
Host CPU Interface Timing Chart (Serial Out)



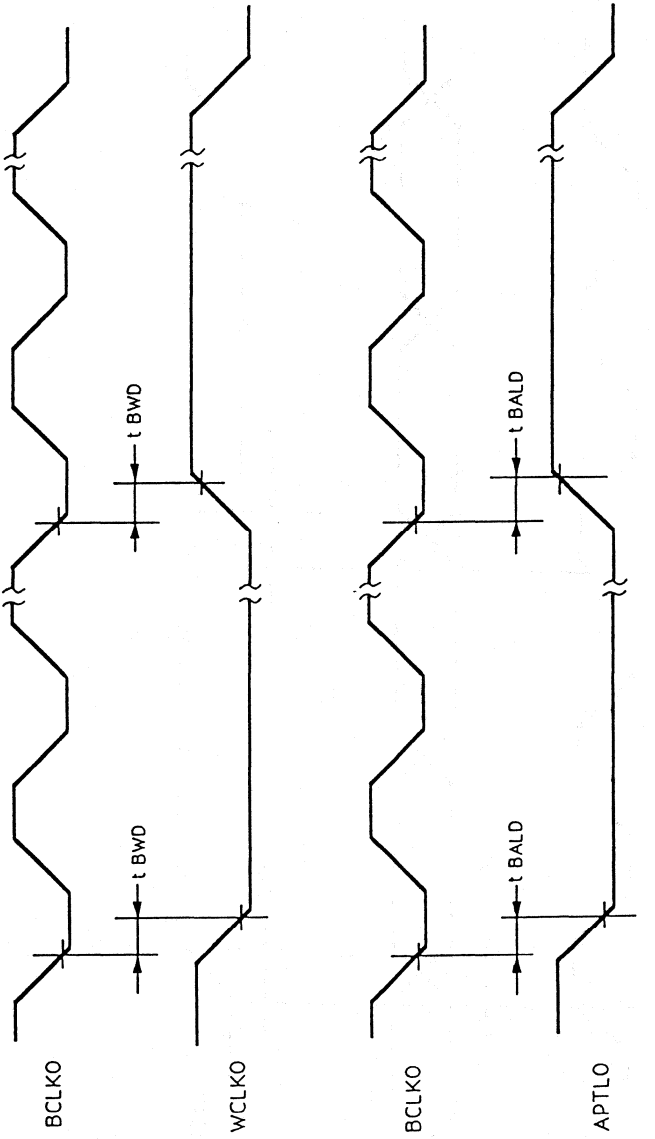
Audio Interface Timing Chart (Serial In)



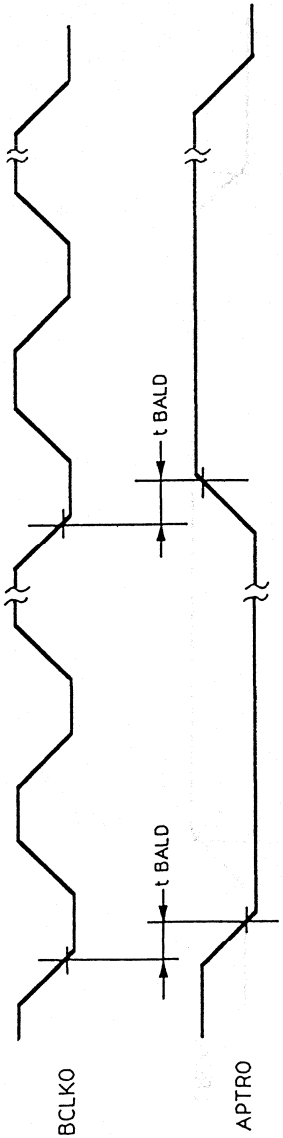
Audio Interface Timing Chart (Serial Out)



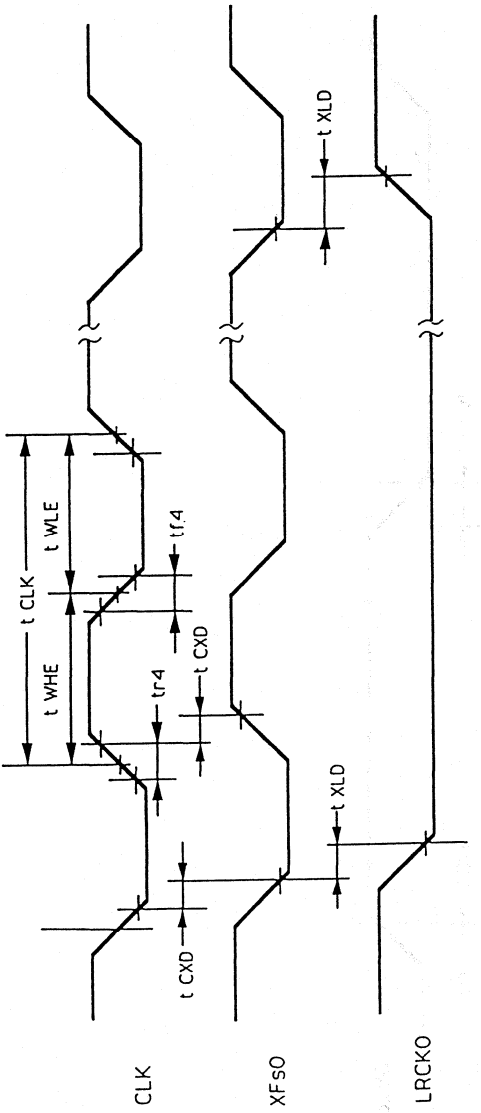
Clock Timing Chart



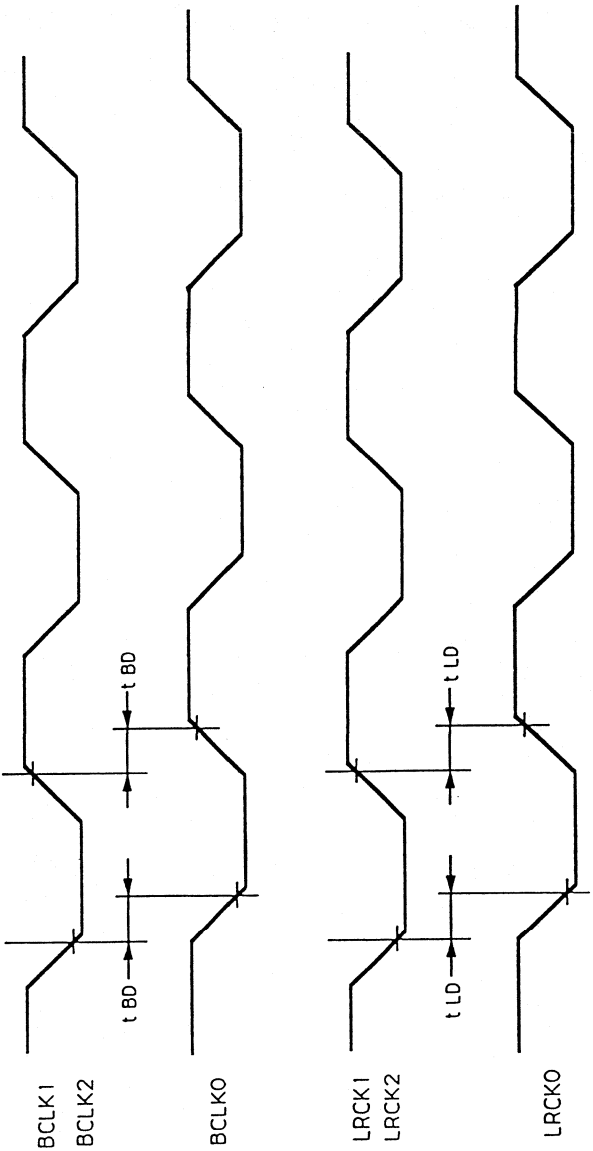
Clock Timing Chart



Clock Timing Chart



Clock Timing Chart



AUDIO DIGITAL SIGNAL PROCESSOR

The μPD6381 is a fixed-point arithmetic type CMOS digital signal processor (DSP) intended for the digital processing of audio signals on a real-time basis.

As its basic architecture, the μPD6381 employs the Harvard architecture which separates the instruction memory section from the data memory section. Therefore, the μPD6381 allows three different operations, that is, ALU operation, data transfer, and pointer manipulation to be executed at the same time only with single step. Because both the instruction memory section and coefficient memory section are of a RAM configuration, two or more processes can be executed by rewriting data from the host CPU. Furthermore, the μPD6381 incorporates an audio serial interface and dedicated hardware for controlling external delay RAMs (256K to 2M) and has easy configuration for double-precision arithmetic. Thus, the μPD6381 is ideal for audio digital signal processing such as sound field control and tone control and graphic equalizer.

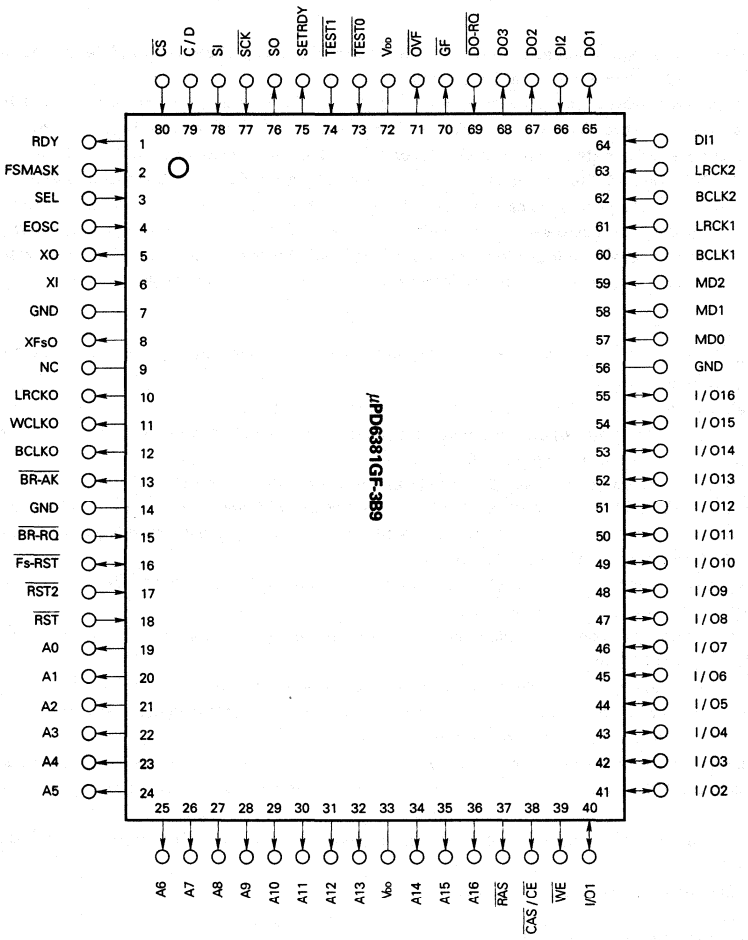
FEATURES

- Instruction RAM (22 bits × 192 words), coefficient RAM (16 bits × 128 words), and data RAM (19 bits × 128 words) are incorporated.
- Dedicated parallel multiplier is incorporated: 19 bits × 16 bits = 31 bits
- High-precision arithmetic operations can be executed thanks to the accumulator and ALU each in a configuration of 31 bits + 3 bits (overflow margin).
- Easy double-precision arithmetic operation is assured through use of a shifter.
- Of the 256K DRAM (64K × 4), 256K SRAM (32K × 8), 1M DRAM (256K × 4), and 1M SRAM (128K × 8), up to two RAM chips can be mounted externally. With one-channel delay, a digital delay of up to 2.7 seconds (1fs × 128K addresses) can be implemented.
- Four input channels and six output channels can be supported with the μPD6381 alone, because the device has two serial input ports and three serial output ports.
- Parallel processing type instructions which allow any ALU operation, data transfer, and memory address update with single step.
- All arithmetic operations including multiplication can be executed in 122 ns (one instruction cycle).
- The contents of the instruction RAM or coefficient RAM can be rewritten dynamically from the host CPU without interrupting the sound processing.
- A function equivalent to 30 secondary Biquad Digital Filters can be implemented (at 44.1 kHz sampling).
- By setting the Master and Slave modes, two or more units of the μPD6381 can be cascade-connected with ease.
- In the above cascade connection, data can be transferred between the μPD6381 units with a data length of 19 bits.
- Host CPU serial interface is incorporated.

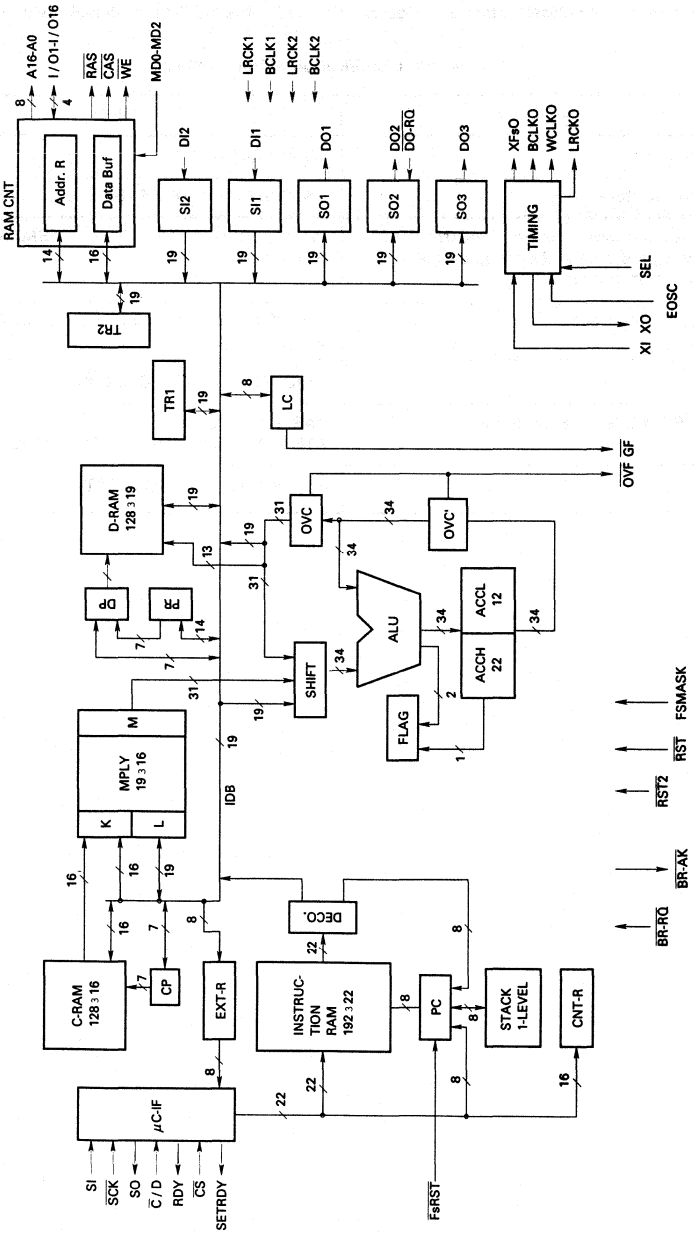
ORDERING INFORMATION

Part Number	Package
μPD6381GF-3B9	80-pin plastic QFP

PIN CONFIGURATIONS (Top View)



INTERNAL BLOCK DIAGRAM



1. PIN FUNCTIONS

Table 1-1 shows the classification of the device pins and **Table 1-2** lists the functions of each pin.

Table 1-1 Classification of Device Pins

Classification	Pins
System clock input	XI, XO, EOSC, SEL
Host CPU interface	$\overline{CS}$, C/$\overline{D}$, RDY, $\overline{OVF}$, $\overline{GF}$, SI, SO, $\overline{SCK}$, $\overline{RST2}$
Pins used in emulation mode (Note that these pins are valid even in ordinary operation modes.)	$\overline{BR}$-$\overline{RQ}$, $\overline{BR}$-$\overline{AK}$, $\overline{DO}$-$\overline{RQ}$, $\overline{Fs}$-$\overline{RST}$, FSMASK, SETRDY
Audio signal interface	DI1, DO1, DI2, DO2, DO3, LRCK1, BCLK1, LRCK2, BCLK2
A/D and D/A support	XFsO, BCLKO, WCLKO, LRCKO
External RAM interface for delay	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ A16 to A0, I/O16 to I/O1, MD0 to MD2
Others	$\overline{RST}$, V_{DD}, GND, $\overline{TEST0}$, $\overline{TEST1}$

Table 1-2 List of Pin Functions

Pin No.	Pin name	Symbol	I/O	Function
33, 72	+ Power Supply	V_{DD}	–	Positive power supply pin to logic circuits.
7, 14, 56	Ground	GND	–	Ground
6	Crystal Input	XI	I	Crystal connection pin (input of inverter)
5	Crystal Output	XO	O	Crystal connection pin (output of inverter)
4	External Clock	EOSC	I	External clock input pin
3	Clock Select Input	SEL	I	Input pin to select either of the external clocks input to the crystal (XI/XO pin) and EOSC pin as the system clock.
80	Chip Select	$\overline{CS}$	I	Input pin for the chip select signal of the μPD6381. While $\overline{CS}$ is active, data can be transferred between the host CPU and the μPD6381 through SI and SO pins. Each signal transferred to SI pin is latched at the high-to-low transition of $\overline{CS}$ signal.
79	Command/Data Input Specification	$\overline{C}$/D	I	Low level of this input pin indicates that the signal on SI pin is a command. High level of this input pin indicates that the signal on SI pin is data.
78	Serial Data Input	SI	I	Input pin for commands and data to the μPD6381. A command or data is input serially.
76	Serial Data Output	SO	O	Pin to serially output the contents of the EXT register or instruction RAM. This pin is of N-channel open drain type.
77	Serial Clock Input	$\overline{SCK}$	I	Each signal input to SI pin or output from SO pin is synchronized with this clock.
1	Ready Output	RDY	O	Output signal to indicate that the μPD6381 is ready to accept commands or data. This pin is of N-channel open drain type.
18	Reset Input	$\overline{RST}$	I	Input pin for the signal to reset the μPD6381.
17	Reset 2 Input	$\overline{RST2}$	I	Input pin for the Reset signal to rewrite the instruction RAM without changing the contents of the internal registers of the μPD6381.
16	Fs Reset Input	$\overline{Fs\text{-}RST}$	I/O	Input pin for the signal to reset the program counter. (This pin is used in emulation mode.) In ordinary modes, pull up this pin with a resistor.

Table 1-2 List of Pin Functions (Cont'd)

Pin No.	Pin name	Symbol	I/O	Function
15	Break Request Input	$\overline{\text{BR-RQ}}$	I	Input pin for a break request signal from the host CPU to the μPD6381. (This pin is used in emulation mode.) In ordinary modes, pull up this pin with a resistor.
13	Break Acknowledge Output	$\overline{\text{BR-AK}}$	O	Output pin to indicate that a break has occurred in the μPD6381 operation. This signal is set by BRAKST instruction. (This pin is used in emulation mode.)
69	Data Out Request Input	$\overline{\text{DO-RQ}}$	I	Input pin for a signal requesting data output from DO1 pin when the μPD6381 is in emulation mode. In ordinary modes, pull up this pin with resistor.
71	Overflow Output	$\overline{\text{OVF}}$	O	Output pin to indicate that overflow compensation has been completed in the μPD6381. This pin is of N-channel open drain type.
70	General Flag Output	$\overline{\text{GF}}$	O	Pin to output the MSB value of the loop counter in the μPD6381. The loop counter is set or reset with an instruction.
64	Data Input 1	DI1	I	Serial input pins for audio signals
66	Data Input 2	DI2	I	
65	Data Output 1	DO1	O	Serial output pins for audio signals
67	Data Output 2	DO2	O	
68	Data Output 3	DO3	O	
60	Bit Clock Input 1	BCLK1	I	Input pin for the bit clock signal of signals to be input or output through DI1 and DI2 pins or DO1, DO2, and DO3 pins. Either BCLK1 or BCLK2 is selected by the CNT register.
62	Bit Clock Input 2	BCLK2	I	
61	LR Clock Input 1	LRCK1	I	Input pin for the signal specifying L channel or R channel of signals to be input or output through DI1 and DI2 pins or DO1, DO2, and DO3 pins. Either LRCK1 or LRCK2 is selected by the CNT register.
63	LR Clock Input 2	LRCK2	I	
36	Ext. RAM Address Output 16	A16	O	Address output pins of the external RAM for digital delay (A16 to A0). A16 is the MSB, whereas A0 is the LSB. When DRAM is selected, both row and column addresses are output.
35	Ext. RAM Address Output 15	A15		

Table 1-2 List of Pin Functions (Cont'd)

Pin No.	Pin name	Symbol	I/O	Function
34	Ext. RAM Address Output 14	A14	O	Address output pins of the external RAM for digital delay (A16 to A0). A16 is the MSB, whereas A0 is the LSB. When DRAM is selected, both row and column addresses are output.
32	Ext. RAM Address Output 13	A13		
31	Ext. RAM Address Output 12	A12		
30	Ext. RAM Address Output 11	A11		
29	Ext. RAM Address Output 10	A10		
28	Ext. RAM Address Output 9	A9		
27	Ext. RAM Address Output 8	A8		
26	Ext. RAM Address Output 7	A7		
25	Ext. RAM Address Output 6	A6		
24	Ext. RAM Address Output 5	A5		
23	Ext. RAM Address Output 4	A4		
22	Ext. RAM Address Output 3	A3		
21	Ext. RAM Address Output 2	A2		
20	Ext. RAM Address Output 1	A1		
19	Ext. RAM Address Output 0	A0		
55	Ext. RAM Data I/O16	I/O16	I/O	Data input/output pins of the external RAM for digital delay (I/O16 to I/O1). I/O16 is the MSB, whereas I/O1 is the LSB.
54	Ext. RAM Data I/O15	I/O15		
53	Ext. RAM Data I/O14	I/O14		
52	Ext. RAM Data I/O13	I/O13		
51	Ext. RAM Data I/O12	I/O12		
50	Ext. RAM Data I/O11	I/O11		

Table 1-2 List of Pin Functions (Cont'd)

Pin No.	Pin name	Symbol	I/O	Function
49	Ext. RAM Data I/O10	I/O10	I/O	Data input/output pins of the external RAM for digital delay (I/O16 to I/O1). I/O16 is the MSB, whereas I/O1 is the LSB.
48	Ext. RAM Data I/O9	I/O9		
47	Ext. RAM Data I/O8	I/O8		
46	Ext. RAM Data I/O7	I/O7		
45	Ext. RAM Data I/O6	I/O6		
44	Ext. RAM Data I/O5	I/O5		
43	Ext. RAM Data I/O4	I/O4		
42	Ext. RAM Data I/O3	I/O3		
41	Ext. RAM Data I/O2	I/O2		
40	Ext. RAM Data I/O1	I/O1		
39	Ext. RAM Write Enable Output	$\overline{WE}$	O	Output pin for the write enable signal of the external RAM for digital delay.
38	Ext. RAM Column Address Strobe/Chip Select Output	$\overline{CAS}/\overline{CS}$	O	Output pin for the column address strobe signal or chip select signal of the external RAM for digital delay.
37	Ext. RAM Row Address Strobe Output	$\overline{RAS}$	O	Output pin for the row address strobe signal of the external RAM for digital delay.
59	Ext. RAM Type Select Input 2	MD2	I	Input pins to select the type and connection condition of the external RAM for digital delay with MD2 to MD0 signals.
58	Ext. RAM Type Select Input 1	MD1		
57	Ext. RAM Type Select Input 0	MD0		
8	X times fs Output	XFsO	O	Output pin for the clock signal to control the A/D or D/A converter. This clock signal is output by dividing the system clock of the μPD6381, according to the frequency dividing ratio specified by the CNT register.
12	Bit Clock Output	BCLKO	O	Output pin for the bit clock signal to control the A/D or D/A converter. In master mode, this pin is used by being connected to BCLK1 or BCLK2 pin.
10	LR Clock Output	LRCKO	O	Output pin for the LR clock signal to control the A/D or D/A converter. In master mode, this pin is used by being connected to LRCK1 or LRCK2 pin.

Table 1-2 List of Pin Functions (Cont'd)

Pin No.	Pin name	Symbol	I/O	Function
11	Word Clock Output	WCLKO	O	Output pin for the bit clock signal to control the A/D or D/A converter. LRCKO signal is obtained by dividing the frequency of this signal by two.
9	—	NC	—	Leave this pin open.
2	Fs Mask Input	FSMASK	I	Input pin for the Fs reset inhibit signal. (This pin is used in emulation mode.) In ordinary modes, connect this pin to GND.
73	Test Input	$\overline{\text{TEST0}}$	I	Input pin for testing. Pull up this pin with a resistor.
74	Test Input	$\overline{\text{TEST1}}$	I	Input pin for testing. Pull up this pin with a resistor.
75	Data Set Ready Output	SETRDY	O	Output pin to indicate that the μPD6381 is ready to accept command set (or data set). (This pin is used in emulation mode.) In ordinary modes, leave this pin open.

2. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (at T_a = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to +7.0	V
Input voltage	V_I	−0.3 to V_{DD} +0.3	V
Output voltage	V_O	−0.3 to V_{DD} +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opt}	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input high voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input low voltage	V_{IL}		0		0.3 V_{DD}	V
Clock input frequency	f_{CLK}		8.0	24.576	25.0	MHz

DC CHARACTERISTICS (at T_a = −40 to +85 °C, V_{DD} = 5.0 V ± 10 %)

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating supply current		I_{DD}			20		mA
Input voltage	High	V_P	SI, $\overline{SCK}$, C/$\overline{D}$, $\overline{CS}$, $\overline{Fs\text{-}RST}$, $\overline{RST}$, RST2, DO-RQ, BR-RQ		3.4		V
	Low	V_N			1.5		
Input voltage	High	V_P	I/O1 to I/O16	2.4			V
	Low	V_N				0.4	
Input voltage	High	V_{IH}	All pins except those indicated above	0.7 V_{DD}		V_{DD}	V
	Low	V_{IL}		0		0.3 V_{DD}	
Output voltage	High	V_{OH}	I_{OH} = −1 mA	V_{DD} −1.0			V
	Low	V_{OL}	I_{OL} = 1 mA			1.0	
Input leakage current	High	I_{LH}	V_{IN} = V_{DD}		10		μA
	Low	I_{LL}	V_{IN} = 0 V		10		

CAPACITANCE (at T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f_C = 1 MHz			10	pF
Output capacitance	C_{OUT}	f_C = 1 MHz			20	pF

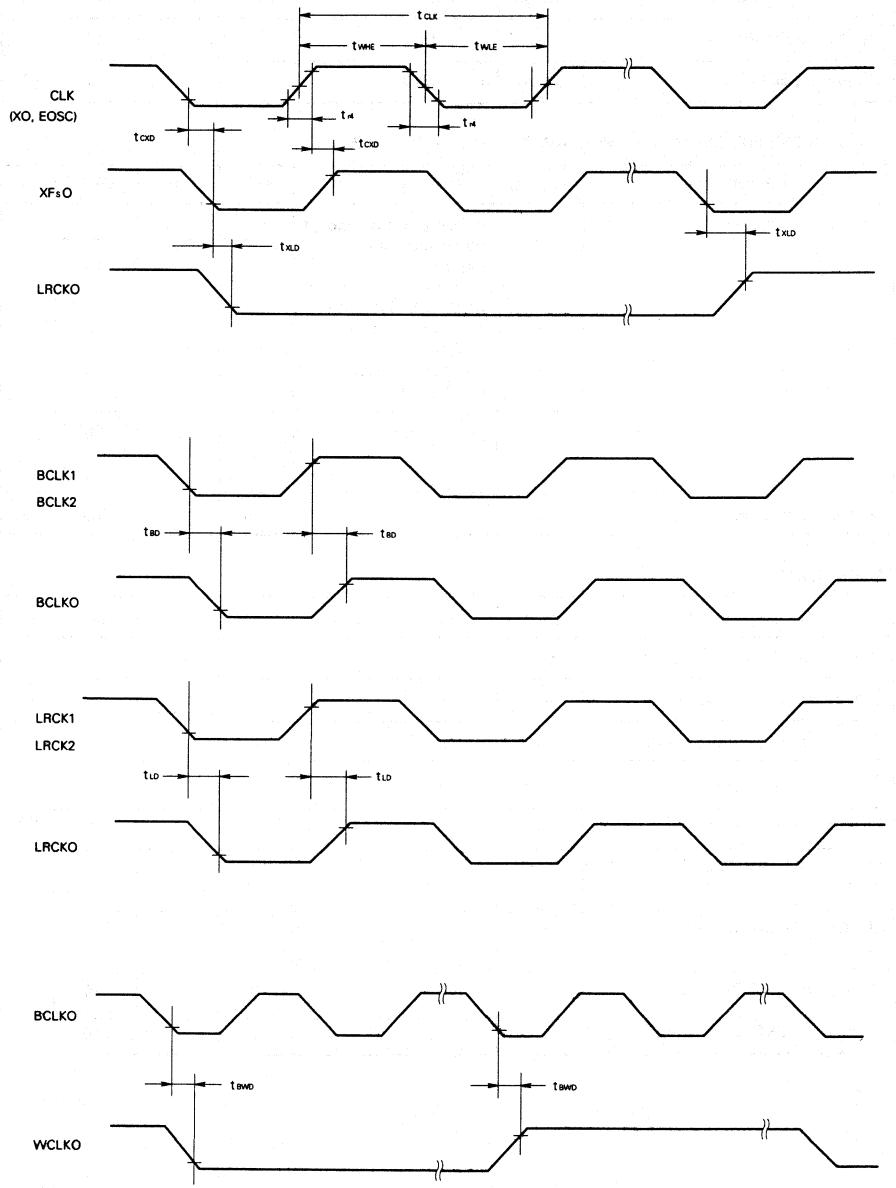
AC CHARACTERISTICS (at T_a = −40 to +85 °C, V_{DD} = 5.0 V ± 10 %)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Rise and fall times	t_{r1}	All output pins except those indicated below			15	ns
	t_{f1}				15	
	t_{r2}	RDY, SO, $\overline{OVF}$ with 4.7 kΩ pull-up resistor (N-channel open drain pins)		80		
	t_{f2}				15	
	t_{r3}	I/O1 to I/O4			15	
	t_{f3}				15	
Operating frequency	f_{tcy}		8.0		25.0	MHz

CLOCK RELATED

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
CLK pulse width (High level)	t_{WHE}			20		ns
CLK pulse width (Low level)	t_{WLE}			20		
CLK pulse repetition period	t_{CLK}		40			
Clock rise time/fall time	t_{r4}, t_{f4}				15	
CLK to XFsO delay time	t_{CXD}				20	
BCLK1/BCLK2 to BCLKO delay time	t_{BD}				20	
LRCK1/LRCK2 to LRCKO delay time	t_{LD}				20	
BCLKO to WCLKO delay time	t_{BWD}		0		40	
XFsO to LRCKO delay time	t_{XLD}		0		40	

TIMING CHARTS OF CLOCK RELATED SIGNALS

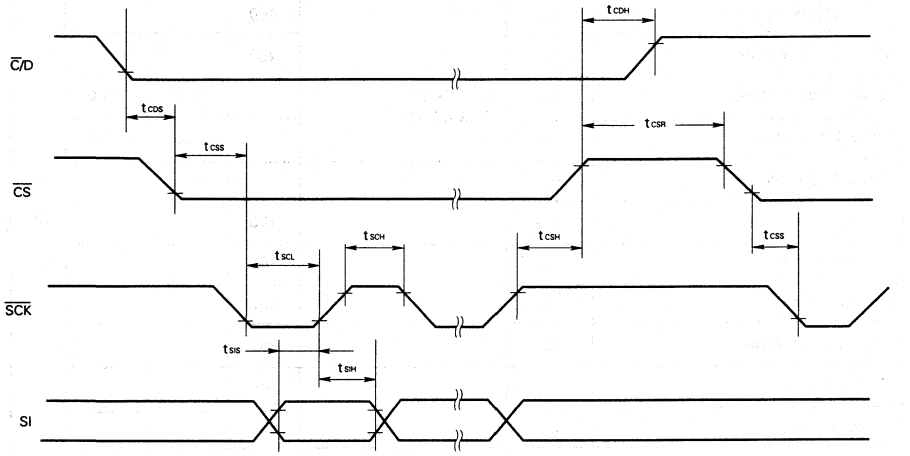


HOST CPU INTERFACE

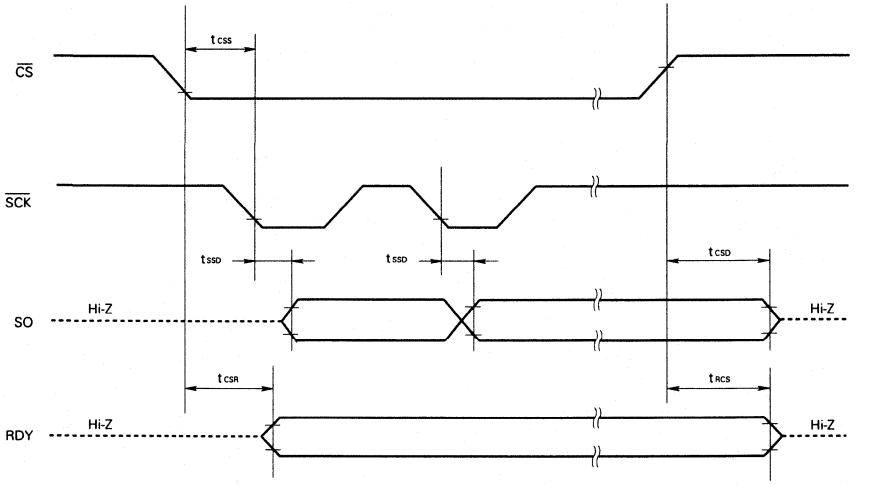
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ high-level time	t_{SCH}		250			ns
$\overline{SCK}$ low-level time	t_{SCL}		250			
$\overline{SCK}$/SO delay time	t_{SSD}	C_L = 15 pF R_L = 4.7 kΩ		100	150	
$\overline{CS}$/SO delay time	t_{CSD}			100	150	
$\overline{C}$/D setup time	t_{CDS}		100			
$\overline{C}$/D hold time	t_{CDH}		100			
$\overline{CS}$ setup time	t_{CSS}		100			
$\overline{CS}$ hold time	t_{CSH}		100			
$\overline{CS}$ recovery time	t_{CSR}		360			
SI setup time	t_{SIS}		100			
SI hold time	t_{SIH}		100			
$\overline{CS}$/RDY delay time	t_{RCS}				500	

4

TIMING CHARTS OF HOST CPU INTERFACE RELATED SIGNALS (SERIAL INPUT)



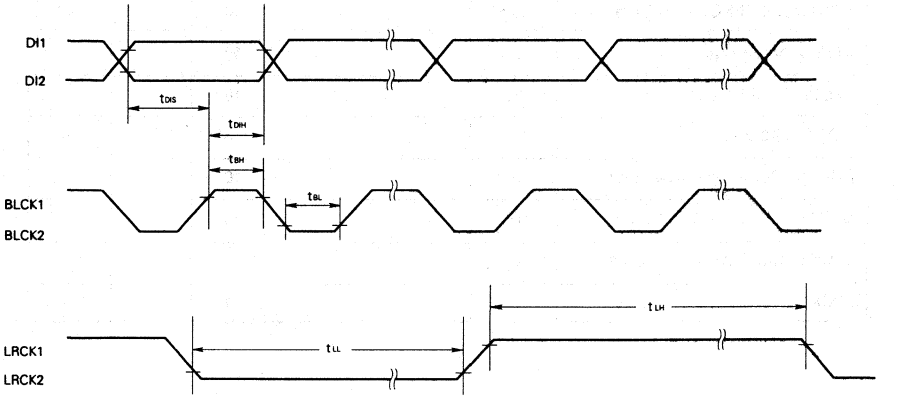
TIMING CHARTS OF HOST CPU INTERFACE RELATED SIGNALS (SERIAL OUTPUT)



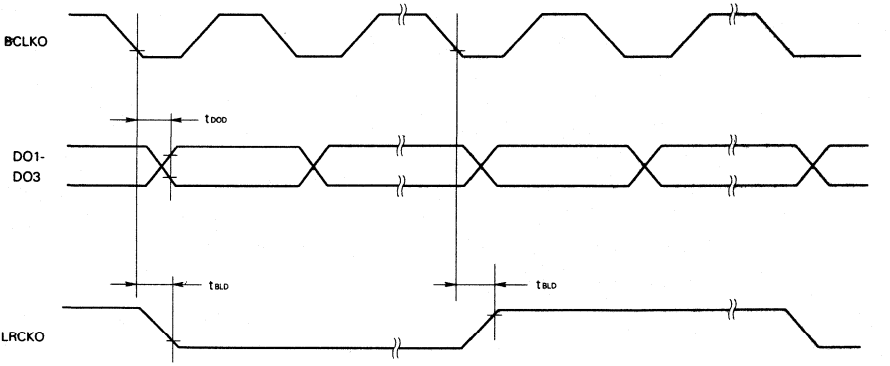
AUDIO INTERFACE

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
BCLKO to LRCKO delay time	t_{BLD}		0		40	ns
DI1/DI2 setup time	t_{DIS}		100			
DI1/DI2 hold time	t_{DIH}		100			
DO1 – DO3 delay time	t_{DOD}		−40		40	
BCLK1/BCLK2 high-level time	t_{BH}		100			
BCLK1/BCLK2 low-level time	t_{BL}		100			
LRCK1/LRCK2 high-level time	t_{LH}		1			μs
LRCK1/LRCK2 low-level time	t_{LL}		1			

TIMING CHARTS OF AUDIO INTERFACE RELATED SIGNALS (SERIAL INPUT)



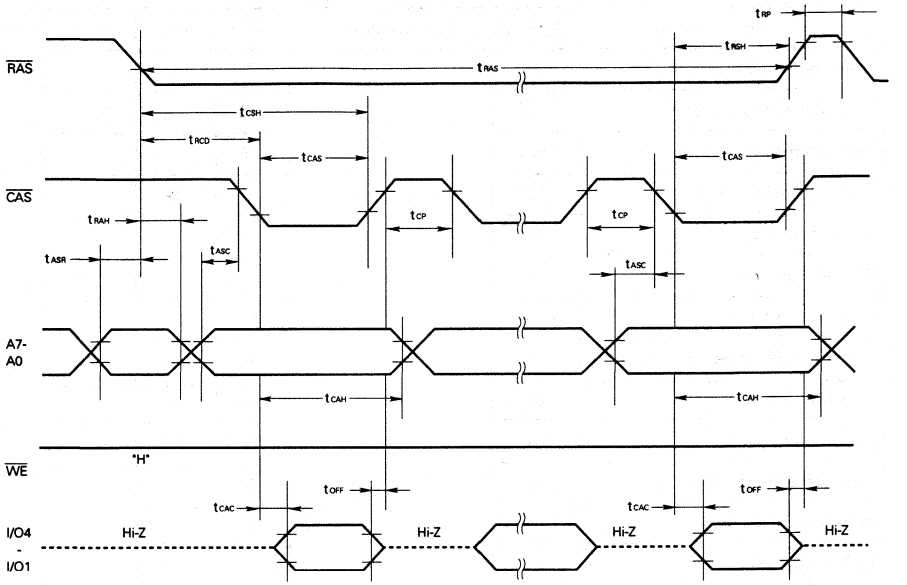
TIMING CHARTS OF AUDIO INTERFACE RELATED SIGNALS (SERIAL OUTPUT)



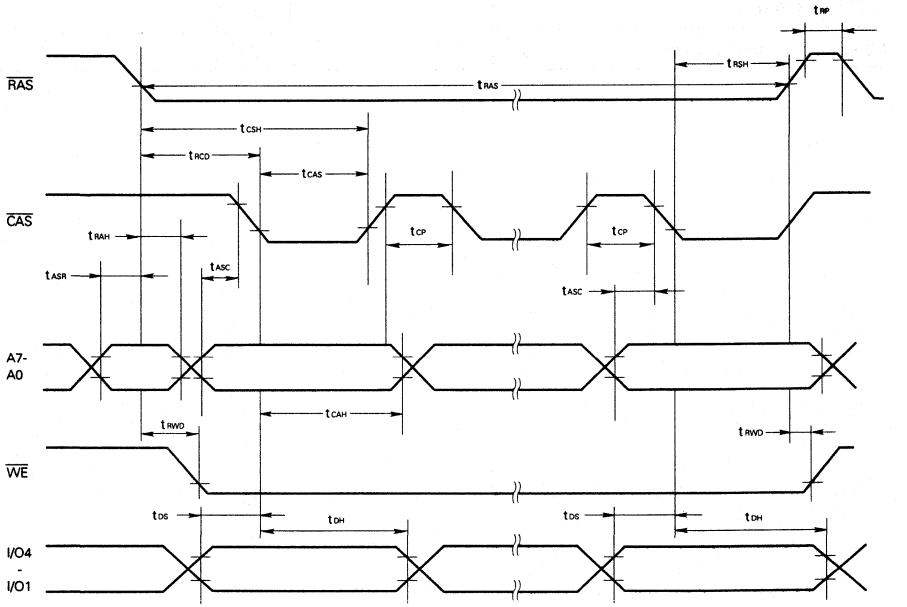
EXTERNAL MEMORY INTERFACE (WHEN DRAM IS SELECTED)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Read data hold time	t_{DRF}		0			ns
Row address setup time	t_{ASR}		40			
Row address hold time	t_{RAH}		40			
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}			$3t_{CY}$		
$\overline{CAS}$ pulse width	t_{CAS}		80			
$\overline{CAS}$ access time	t_{CAC}				50	
$\overline{CAS}$ high-level time	t_{CP}		50			
Column address setup time	t_{ASC}		40			
$\overline{RAS}$ hold time	t_{RSH}		80			
$\overline{RAS}$/$\overline{WE}$ delay time	t_{RWD}			70		
Write data setup time	t_{DS}		30			
Write data hold time	t_{DH}		40			
$\overline{RAS}$ pulse width	t_{RAS}			800		
$\overline{RAS}$ precharge time	t_{RP}		100			
$\overline{CAS}$ hold time	t_{CSH}		200			
Column address hold time	t_{CAH}		80			

TIMING CHARTS OF EXTERNAL MEMORY READ OPERATION (WITH DRAM)



TIMING CHARTS OF EXTERNAL MEMORY WRITE OPERATION (WITH DRAM)



EXTERNAL MEMORY INTERFACE (WHEN SRAM IS SELECTED)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Read/write cycle time	t_C		210			ns
$\overline{CE}$ access time	t_{CEA}				120	
$\overline{CE}$ pulse width	t_{CE}		120			
Address setup time	t_{ASC}		0			
Address hold time	t_{AHC}		30			
$\overline{CE}$ precharge time	t_P		80			
Output data Off time	t_{CHZ}				40	
Write command hold time	t_{WCH}		60			
Write command read time	t_{CWL}		60			
$\overline{WE}$ pulse width	t_{WP}		60			
Write data setup time	t_{DSC}		50			
Write data hold time	t_{DHC}		0			
Write data setup time	t_{DSW}		50			
Write data hold time	t_{DHW}		0			

TV Analog ICs

5

VERTICAL DEFLECTION OUTPUT IC FOR COLOR TELEVISION

The μPC1488H is a vertical deflection output IC for color television. This IC requires no voltage-boosted pulses and can therefore be connected to chrominance-video deflection IC μPC1401CA, deflection IC μPC1377C, or the like.

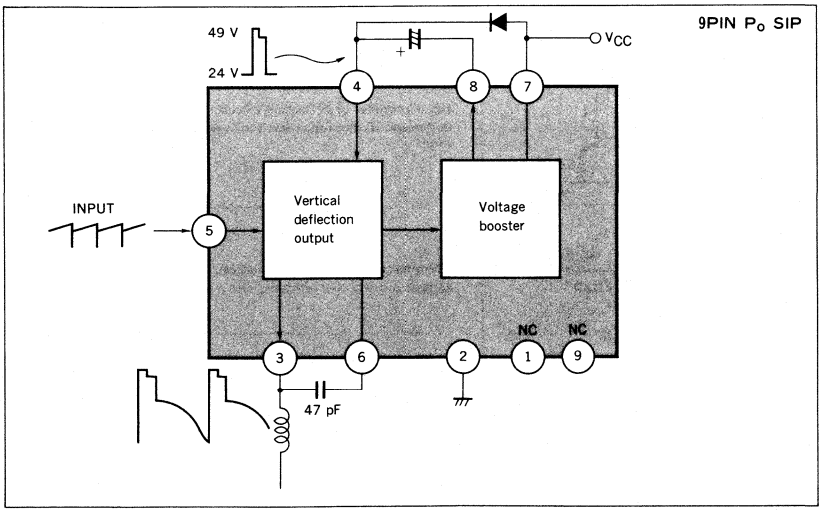
The package is designed for one-point fixing, reducing installation man-hours.

It is optimum for 9-inch to 21-inch color televisions.

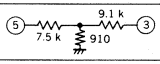
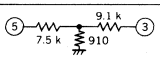
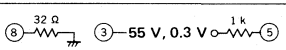
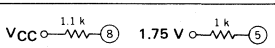
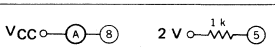
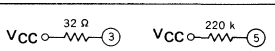
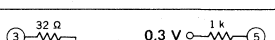
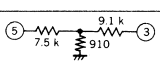
FEATURES

- The IC requires high power voltage only during fly-back time, greatly reducing power consumption.
- Deflection control in the preceding stage can be used both by discrete components and ICs.
- The package is designed for one-point fixing, reducing installation man-hours.
- The IC can be connected directly to deflection IC μPC1377C or chrominance-video deflection IC μPC1401CA.

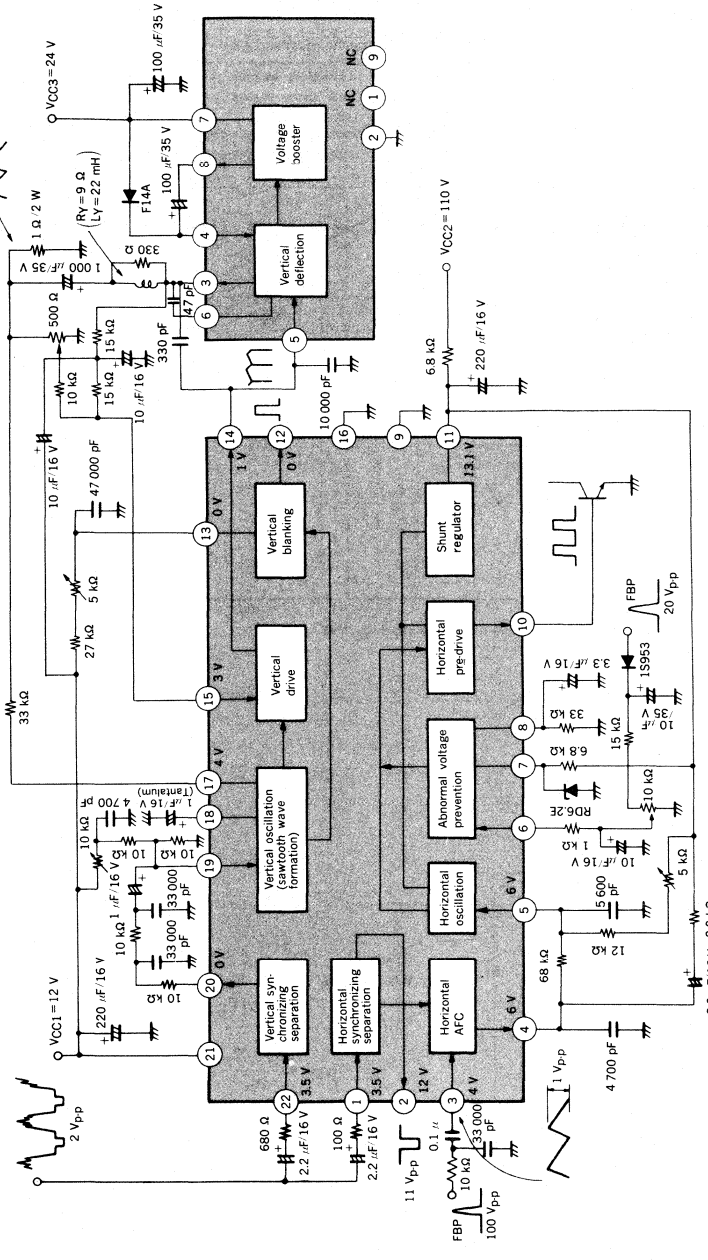
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_a = 25 °C, R_L = 9 Ω, 22 mH)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power supply current	I_{CC}	170	190	210	mA	Standard circuit (I_{DEF} = 1.3 A TYP.)
Deflection voltage	I_{DEF}	1.2	1.3	1.4	A_{p-p}	Standard circuit
Neutral point potential	V_{ODC}	10.0	12.0	14.0	V	
Fly-back pulse voltage	RPV	46	49	54	V	Standard circuit
Blanking pulse width	RPW	850	1000	1200	μs	Standard circuit
Idling current	I_Q	8	15	24	mA	
Voltage booster discharge saturation voltage	V_{S7-8}		1.4	2.0	V	
Voltage booster charge saturation voltage	V_{S8-2}		1.0	1.5	V	
Voltage booster charge current	I_8	55	85	120	mA	
Deflection circuit output saturation voltage	V_{S3-2}		0.8	1.6	V	
Deflection circuit output saturation voltage	V_{S4-3}		2.0	3.0	V	
Deflection circuit input saturation voltage	V_5	0.85	1.0	1.15	V	
Voltage gain	A_{VO}		55		dB	Standard circuit (R_L = ∞)
Input resistance	R_{in}		22		kΩ	Standard circuit
Thermal resistance	$R_{th(j-c)}$			5.0	°C/W	

APPLICATION CIRCUIT EXAMPLE



The application circuit and circuit constants described in this material shall not apply to a design for mass production where parts deviations and temperature characteristics are considered. Those factors should be studied before applying this IC to mass production.

5

VERTICAL DEFLECTION OUTPUT IC FOR COLOR TELEVISION

The μPC1498H is a vertical deflection output IC for color television. This IC requires no voltage-boosted pulses and can therefore be connected to chrominance-video deflection IC μPC1401CA, deflection IC μPC1377C, or the like.

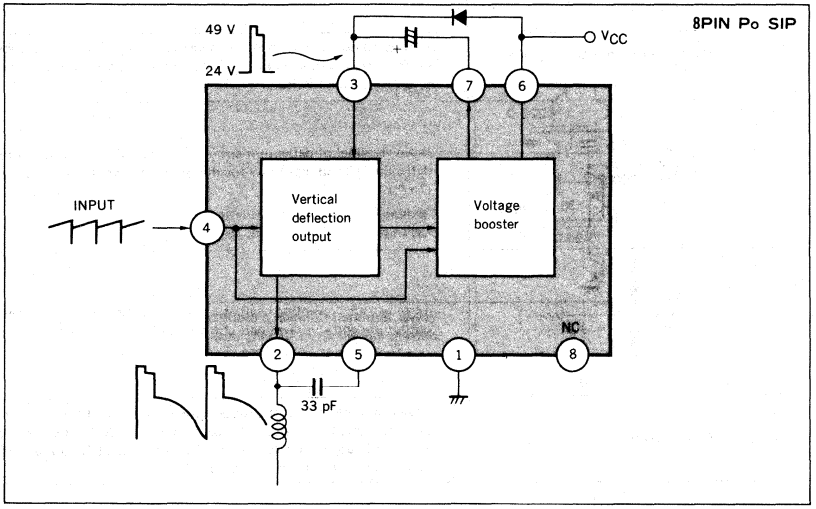
The package is designed for one-point fixing, reducing installation man-hours.

It is optimum for 22-inch or larger color televisions.

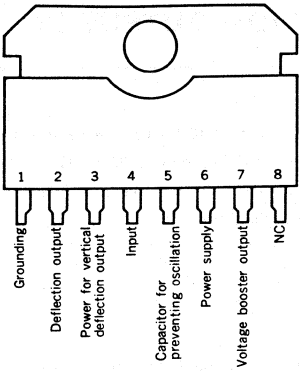
FEATURES

- The IC requires high power voltage only during fly-back time, greatly reducing power consumption.
- Deflection control in the preceding stage can be used both by discrete components and ICs.
- The package is designed for one-point fixing, reducing installation man-hours.
- The IC can be connected directly to deflection IC μPC1377C or chrominance-video deflection IC μPC1401CA.

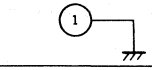
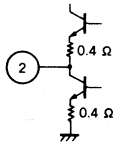
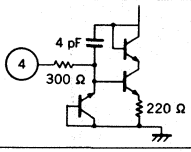
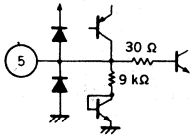
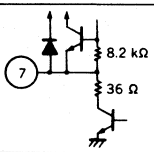
BLOCK DIAGRAM



TERMINAL CONNECTIONS



EQUIVALENT CIRCUIT DIAGRAMS

Pin No.	Equivalent Circuit	Function Explanation
1		Grounding terminal.
2		Deflection output terminal. Connect a deflection coil to this terminal. The coil should have an impedance of R = 6 to 12 Ω and L = 9 to 20 mH. Design should be optimum considering the screen size of TV, saturation voltage of IC, and other factors.
3	Deflection output circuit power supply	Deflection output circuit power supply. The pin 6 voltage is imposed during scanning time and the pin 3 and pin 7 capacitor is charged to $+V_{CC}$ during fly-back.
4		Input terminal of deflection circuit. Connect it to the output of a deflection IC and input saw-tooth waves. The input impedance is 22 kΩ (TYP.).
5		Terminal for preventing oscillation. Connect a capacitor between the output pin and this terminal. Use a 33 to 56 pF capacitor.
6	Power terminal	Power terminal. Connect a diode between pin 3 and this terminal to prevent current from flowing into the terminal during fly-back. Use a diode of approximately 300 mA DC with dielectric strength of 56 V. (This depends on the deflection coil.)
7		Output terminal of voltage booster. It charges an external capacitor during scanning time. The charging voltage is approximately V_{CC}.
8	(8) NC	Unused pin, not connected internally.

ABSOLUTE MAXIMUM RATING (T_a = 25 °C) A positive current flows into the IC, and a negative current flows out of it.

Power supply voltage	$V_{CC(V_6)}$	30	V
Circuit current	I_{CC}	350	mA
Deflection circuit voltage	V_3	65	V
Deflection input signal voltage	V_4	2.5	V
Deflection output current	$I_{DEF(I_2)}$	−1.5 to +1.5	A_{peak}
Voltage booster output current	I_7	−1.5 to +1.5	A_{peak}
Voltage booster output voltage	V_7	V_6	V
Allowable loss	P_D	8.0	W
Operating temperature range	T_{opt}	−20 to +75	°C
Storage temperature range	T_{stg}	−40 to +150	°C
Junction temperature	T_j	+150	°C

RECOMMENDED OPERATING RANGE (T_a = 25 °C)

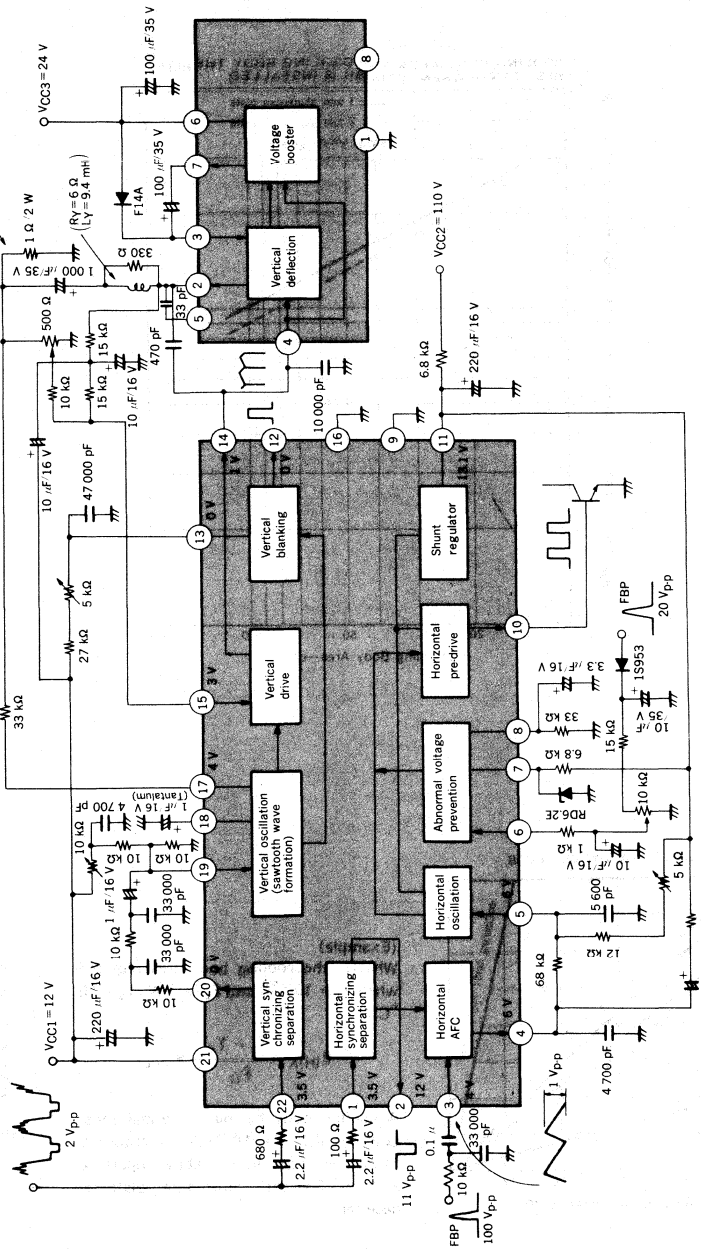
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply voltage	$V_{CC(V6)}$	20	24	27	V
Deflection output current	$I_{DEF(I_2)}$	1.0	–	2.1	A_{p-p}

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_a = 25 °C, R_L = 6 Ω, 9.4 mH)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power supply current	I_{CC}	240	270	300	mA	Standard circuit (I_{DEF} = 2.0 A TYP.)
Deflection voltage	I_{DEF}	1.9	2.0	2.1	A_{p-p}	Standard circuit
Neutral point potential	V_{ODC}	10.0	12.0	14.0	V	④ — 7.5 k — 910 — 9.1 k — ②
Fly-back pulse voltage	RPV	46	49	54	V	Standard circuit
Blanking pulse width	RPW	550	650	750	μs	Standard circuit
Idling current	I_Q	8	15	24	mA	④ — 7.5 k — 910 — 9.1 k — ②
Voltage booster discharge saturation voltage	V_{S6-7}		1.8	2.4	V	⑦ — 22 Ω — , ② — 55 V, 0.3 V — 1 k — ④
Voltage booster charge saturation voltage	V_{S7-1}		1.0	1.5	V	V_{CC} — 1.1 k — ⑦ , 1.75 V — 1 k — ④
Voltage booster charge current	I_7	55	85	120	mA	V_{CC} — Ⓐ — ⑦ , 1.75 V — 1 k — ④
Deflection circuit output saturation voltage	V_{S2-1}		1.0	1.6	V	V_{CC} ③ — 22 Ω — ②
Deflection circuit output saturation voltage	V_{S3-2}		2.4	3.0	V	② — 22 Ω — , 0.3 V — 1 k — ④
Deflection circuit input saturation voltage	V_4	0.85	1.0	1.15	V	④ — 7.5 k — 910 — 9.1 k — ②
Voltage gain	A_{VO}		55		dB	Standard circuit (R_L = ∞)
Input resistance	R_{in}		22		kΩ	Standard circuit
Thermal resistance	$R_{th(j-c)}$			4.0	°C/W	

APPLICATION CIRCUIT EXAMPLE

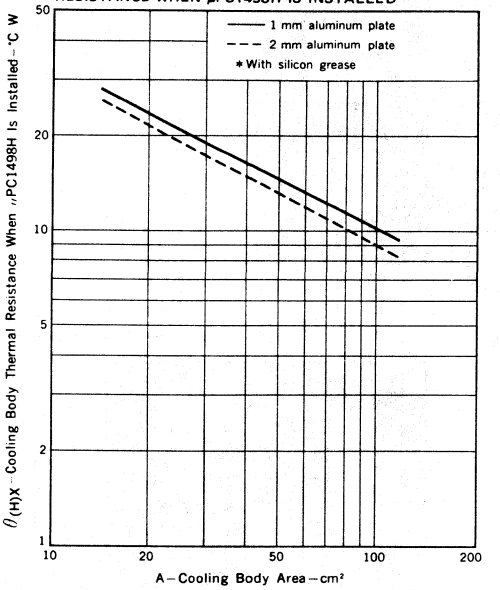


The application circuit and circuit constants described here do not apply to a design for mass production where parts deviations and temperature characteristics are considered. Those factors should be studied before applying this IC to mass production.

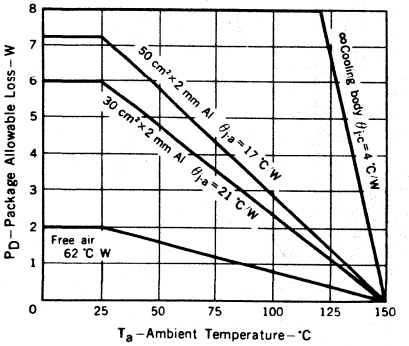
5

DESIGN OF COOLING BODY

COOLING BODY AREA AND COOLING BODY THERMAL RESISTANCE WHEN μPC1498H IS INSTALLED



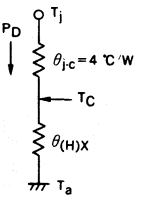
PACKAGE ALLOWABLE LOSS



(Example)
What is the cooling body area required when T_j = 100 °C and P_D = 3 W (T_a = 40 °C)?

$$\theta_{(H)X} = \frac{T_j - T_a}{P_D} - \theta_{(j-c)}$$

A cooling body having a thermal resistance of $\theta_{(H)X}$ = 16 °C/W is required. From the graph in the above figure, a 2 mm, 33 cm² aluminum plate is necessary.



PRECAUTIONS FOR HANDLING

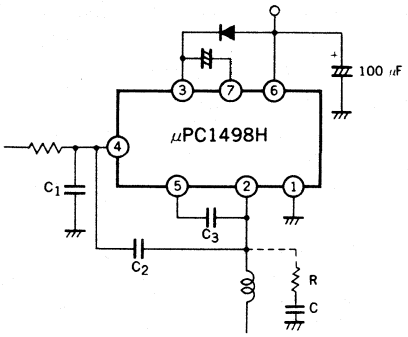
1. Oscillation

(1) C_1, C_2, and C_3 have to be changed depending on the deflection IC or coil in the preceding stage or the wiring of the printed circuit board.

If a difference between those capacitors is very large, a fly-back rise time is delays. If oscillation can not be stopped with these capacitors, connect R (approximately 10 Ω) and C (0.01 μF) in series between the pin 2 and GND.

(2) Ground the GND terminal of the pin 6 electrolytic capacitor near pin 1.

(3) Ground the GND terminal of the pin 4 capacitor near pin 1.



2. Installation

(1) Use a radiator of flatness 0.1 mm or less.

(2) Apply silicon grease between the cooling bodies of the IC.

(3) Use a 3 mm small screw with a large head diameter.

(4) Apply screw tightening torques and speeds shown in the table below.

Tightening torque (km·cm)			Speed (rpm)	
MIN.	TYP.	MAX.	TYP.	MAX.
5	7	10	400	1000

3. Design Precautions

A set must be designed so that the lower part is not saturated even at the free-run frequency. (If saturated, bounce occurs.)

SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT VOLTAGE STABILIZER FOR ELECTRONIC TUNER

The μPC574J is a monolithic integrated voltage stabilizer especially designed as voltage supplier for varactor diodes in television tuners.

FEATURES

- Low temperature coefficient
- Low dynamic resistance
- Typical reference voltage of 33 V

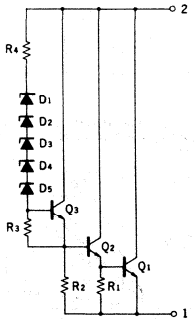
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Zener Current	I_Z	10	mA
Power Dissipation	P_D	200 (Note)	mW
Operating Ambient Temperature Range	T_{opt}	- 20 to 75	°C
Storage Temperature Range	T_{stg}	- 40 to 125	°C

Note: At ambient temperature of 75°C

Pin Connection
1. Anode
2. Cathode

EQUIVALENT CIRCUIT

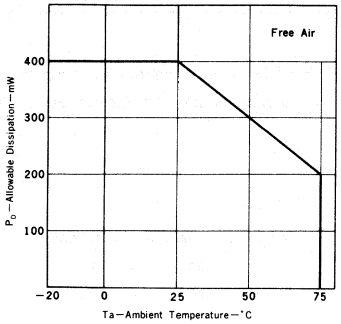


ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Stabilized Voltage	V_Z	31		35	V	I_Z = 5mA
Stabilized Voltage Temperature Drift	$\Delta V_Z/\Delta T$	-1.0	0	1.0	mV/°C	I_Z = 5mA Ta = - 20 to 75°C
Dynamic Resistance	r_z		10	25	Ω	I_Z = 5mA f = 1 kHz I_{AC} = 0.5mA

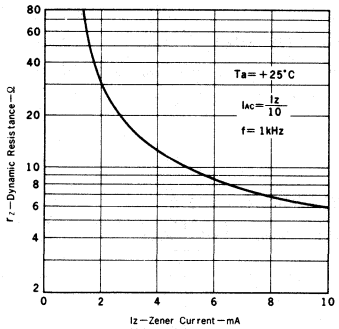
POWER-TEMPERATURE DERATING CURVE

ALLOWABLE DISSIPATION vs.
AMBIENT TEMPERATURE

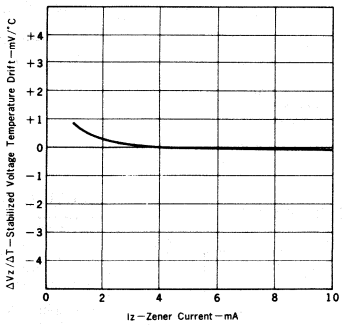


TYPICAL CHARACTERISTIC CURVES (Ta = 25°C)

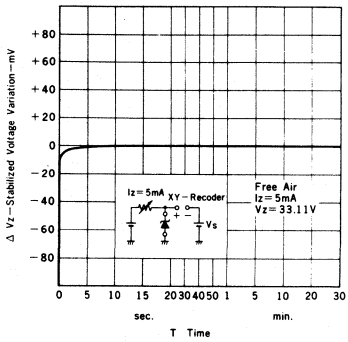
DYNAMIC RESISTANCE vs.
ZENER CURRENT



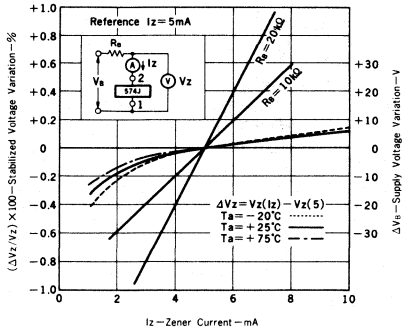
STABILIZED VOLTAGE TEMPERATURE
DRIFT vs. ZENER CURRENT



STABILIZED VOLTAGE VARIATION
vs. TIME

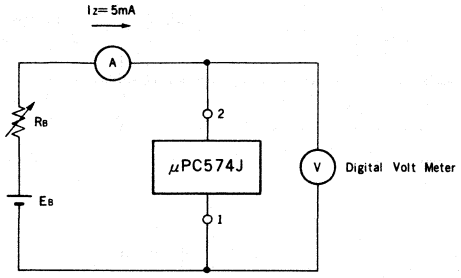


STABILIZED VOLTAGE VARIATION &
SUPPLY VOLTAGE VARIATION vs.
ZENER CURRENT

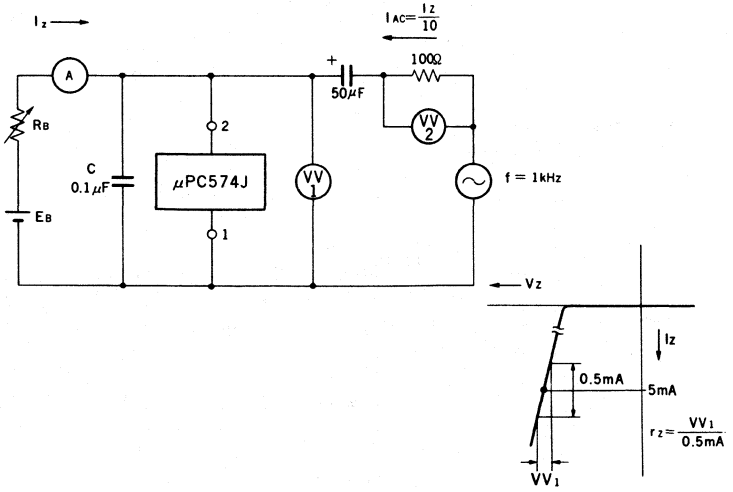


MEASURING CIRCUITS

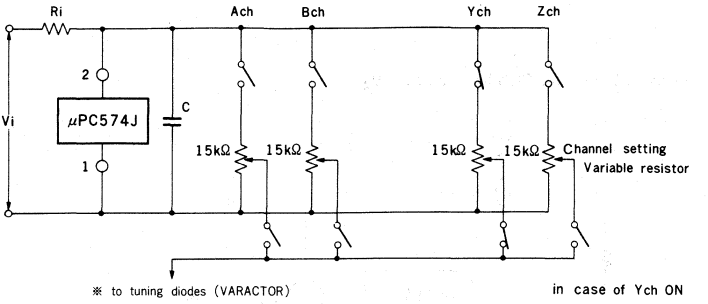
Measuring Circuit for Stabilized Voltage V_Z



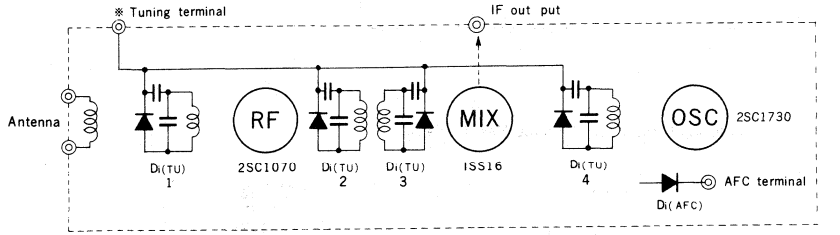
Measuring Circuit for Dynamic Resistance r_Z



TYPICAL APPLICATION

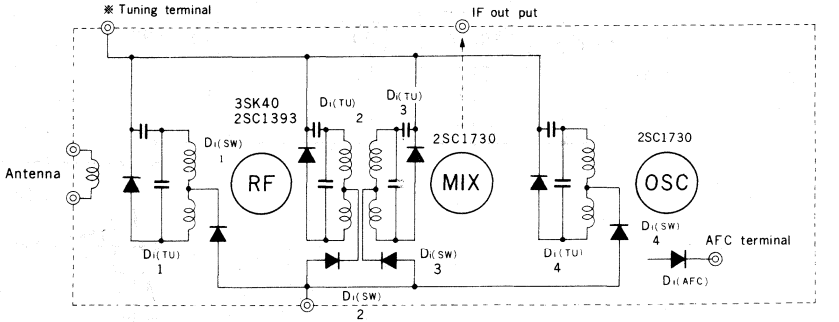


(1) UHF Tuner



$D_{i(TU)1}$~$D_{i(TU)4}$: IS2208 $D_{i(AFC)}$: IS2207

(2) VHF Tuner



$D_{i(TU)1}$~$D_{i(TU)4}$: IS2209 $D_{i(AFC)}$: IS2207 $D_{i(SW)1\sim4}$: IS2222

COLOR TV/VTR PLL IF SIGNAL PROCESSING IC

The μPC1820 is a semiconductor integrated circuit for processing the color TV/VTR PIF/SIF signals. This IC is housed in a 30-pin shrink dual-in-line package (DIP). Its main features are supported by the built-in keyed-pulse generator circuit needed for the L-SECAM, the VTR-oriented EQ amplifier, the SECAM-L/PAL B/G switch, the PLL VCO circuit, and the split sound carrier output device.

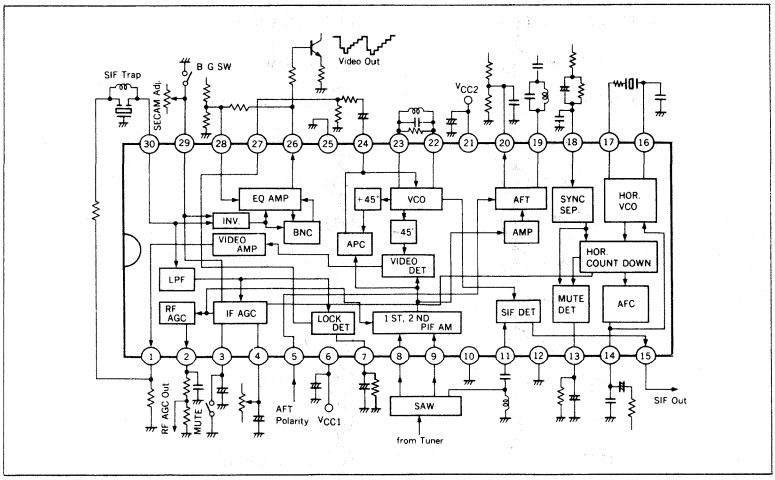
FEATURES

- SECAM-L system (keyed AGC) and PAL B/G system (peak AGC) application.
- For SECAM L system, the built-in keying pulse generator circuit realizes the VTR application which has no FBP.
- Good DG, DP characteristics is realized by the PLL system video detection circuit.
- Video equalizer circuit for VTR application.
- Split-carrier system realizes high audio-sensitivity and good S/buzz characteristics.
- Built-in Mute detection circuit
- AFT polarity switching circuit is provided.
- Supply voltage 9 V
- Power consumption 477 mW

ORDERING INFORMATION

Part number	Package
μPC1820CA	30 pin plastic shrink DIP (400 mil)

BLOCK DIAGRAM



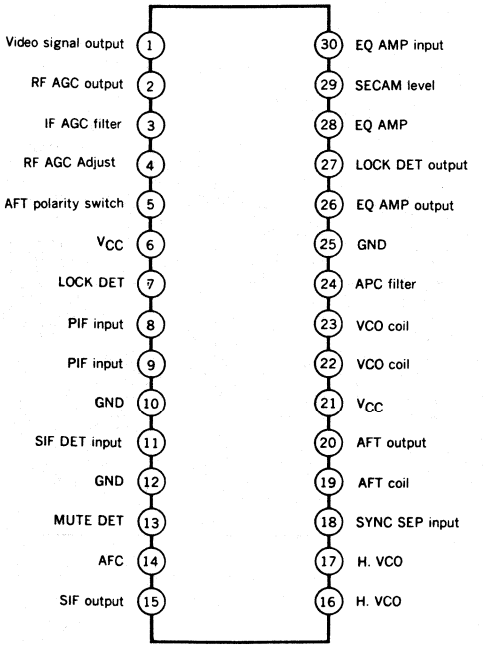
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC}	11	V
Control Voltage	V_{29}	7	V
AFT Control Voltage	V_5	V_{CC}	V
Power Dissipation	P_D	590 (T_a = 75 °C)	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING RANGE (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	RECOMMENDED VALUE	UNIT
Supply Voltage	V_{CC}	8.0 to 9.0 to 10.0	V
Control Voltage (B/G)	V_{29L}	0 to 1.0	V
Control Voltage (L)	V_{29H}	3.0 to 5.0	V
AFT Control Voltage (1)	V_{5L}	0 to 1.7	V
AFT Control Voltage (2)	V_{5H}	3.7 to 8	V

PIN CONNECTION (Top View)

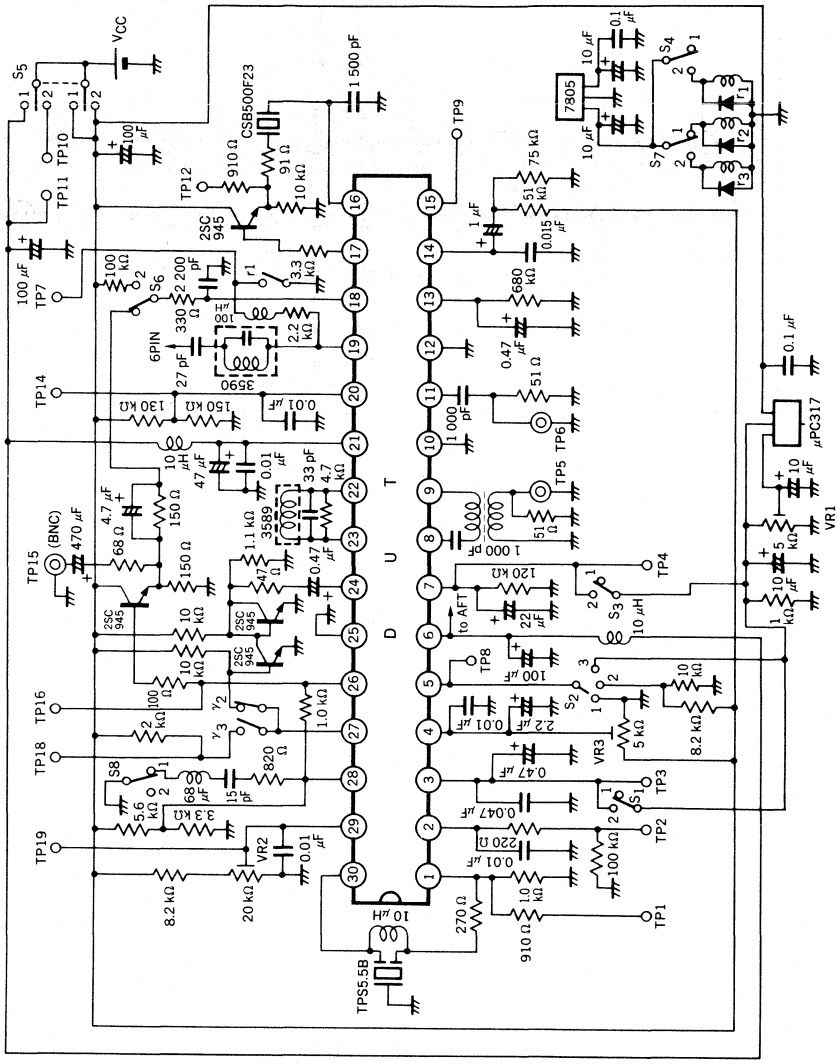


ELECTRICAL RATINGS (T_a = 25 ±3 °C, RH ≦ 70 %, unless otherwise specified)

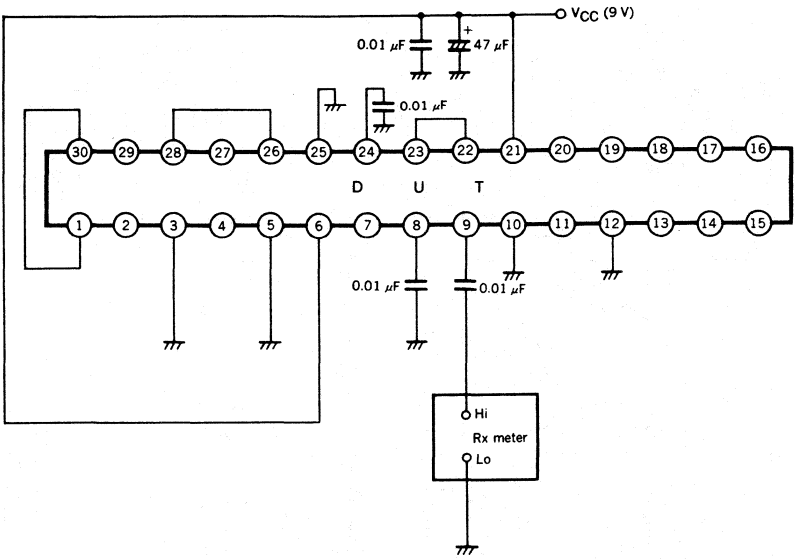
Characteristic	Symbol	MIN.	TYP.	MAX.	UNIT	Test conditions
Circuit current	I_{CC}	42	53	68	mA	No signal (L mode)
Video detection output voltage 1	V_O(B)	1.6	1.9	2.4	V_{p-p}	V_{ip} = 90 dBμ, f_o = 32.7 MHz, and video modulation is 87.5 %. (B/G mode)
Video detection output voltage 2	V_O(L)		2.0		V_{p-p}	V_{ip} = 90 dBμ, f_o = 32.7 MHz, and video modulation is 94 %. (L mode)
Video detection output DC voltage 1	V_1(B)	4.8	5.0	5.3	V	No signal (B/G mode)
Video detection output DC voltage 2	V_1(L)	4.8	5.0	5.2	V	No signal (L mode)
Video detection output DC voltage 3	V_{26}(B)	5.1	5.5	6.0	V	No signal (B/G mode)
Video detection output DC voltage 4	V_{26}(L)	2.4	2.8	3.2	V	No signal (L mode)
Video S/N	P/N	47	52		dB	V_i = 90 dBμ (L mode)
Video frequency characteristics	BW(B)	6.0	8.0		MHz	Modulated frequency when V_o(P) has decreased by 3 dB due to a change of the input IF modulated signal.
Input sensitivity	V_{ip}SENSE		49	53	dBμ	Input voltage when V_o(P) has decreased by 3 dB as the input IF voltage was gradually reduced. (L mode)
Premissible maximum input	V_{ip}MAX.	105			dBμ	Input voltage when V_o(P) was increased by 1 dB as the input IF voltage was gradually reduced. (L mode)
AFT detector sensitivity 1	μ-1	60	90		mV/kHz	Black video signal at V_{ip} = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = L.
Maximum AFT voltage 1	V_{20H-1}	8.0	8.7		V	Black video signal at V_{ip} = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = L.
Minimum AFT voltage 1	V_{20L-1}		0.24	0.8	V	Black video signal at V_{ip} = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = L.
AFT defeat voltage	V_{20TH}	4.3	4.7	5.3	V	Black video signal: V_{ip} = 90 dBμ (B/G mode)
AFT defeat current	I_{19DEF}	290	340	390	μA	Current that flows from pin 19 at AFT defeat
AFT polarity threshold voltage	V_{5TH}	2.2	2.7	3.2	V	Voltage of pin 5 when the output of pin 20 is reversed
AFT detector sensitivity 2	μ-2	91	108	119	%	Black video signal: V_{ip} = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = H. The ratio of μ-1/μ-2
Maximum AFT voltage 2	V_{20H-2}	8.0	8.7		V	Black video signal: V_{ip} = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = H.
Minimum AFT voltage 2	V_{20L-2}		0.24	0.8	V	Black video signal: V_{ip} = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = H.
IF AGC minimum voltage	V_{3H}	8.2	8.6		V	No input (L mode)
IF AGC minimum voltage	V_{3L}	3.0	3.2	3.4	V	Voltage of pin 3 at maximum input (L mode)
Maximum RF AGC voltage	V_{2H}	7.0	8.0		V	V_{ip} = 90 dBμ, f_o = 32.7 MHz (B/G mode) video modulation is 87.5 %, and APL = 50 %.
Minimum RF AGC voltage	V_{2L}		0	0.5	V	V_{ip} = 90 dBμ, f_o = 32.7 MHz (B/G mode) video modulation is 87.5 %, and APL = 50 %.
Cap challenge (Upper 1)	f_{CLU-1}	0.5	1.49		MHz	V_{ip} = 90 dBμ, f_o = 32.7 MHz, video modulation is 87.5 %, APL = 50 %, and Lock SW = OFF (B/G mode)
Cap challenge (Lower 1)	f_{CLL-1}	1.25	1.64		MHz	V_{ip} = 90 dBμ, f_o = 32.7 MHz, video modulation is 87.5 %, APL = 50 %, and Lock SW = OFF (B/G mode)

Characteristic	Symbol	MIN.	TYP.	MAX.	UNIT	Test conditions
Cap challenge (Upper 2)	f_{COU-2}	0.5	1.49		MHz	V_{ip} = 90 dBμ, f_o = 32.7 MHz video modulation is 87.5 %, APL = 50 %, and Lock SW = ON (B/G mode)
Cap challenge (Lower 2)	f_{CLL-2}	1.20	1.49		MHz	V_{ip} = 90 dBμ, f_o = 32.7 MHz, video modulation is 87.5 %, APL = 50 %, and Lock SW = ON (B/G mode)
Lock detection threshold voltage	V_{7th}	3.9	4.2	4.5	V	Pin 29 is grounded. (B/G mode)
EQ frequency characteristics 1	FC1		2.6		dB	32.7 MHz +0.5 MHz mixed waves (B/G mode)
EQ frequency characteristics 2	FC2		4.7		dB	32.7 MHz +3.43 MHz mixed waves (B/G mode)
EQ frequency characteristics 3	FC3		7.5		dB	32.7 MHz +4.43 MHz mixed waves (B/G mode)
Intermodulation	IM	30	35		dB	CW compound frequency of 32.7 MHz, 37.13 MHz, and 38.2 MHz is input as the PIF input. (B/G mode)
Differential gain	DG		2	5	%	V_{ip} = 90 dBμ, f_o = 32.7 MHz, in the standard 10 step frequency modulation. (B/G mode)
Differential phase	DP		2	5	deg.	V_{ip} = 90 dBμ, f_o = 32.7 MHz, in the standard 10 step frequency modulation. (B/G mode)
SYNC chip level 1	$V_{sync(B)}$	3.0	3.4	3.8	V	V_{ip} = 90 dBμ, f_o = 32.7 MHz (B/G mode), 87.5 % video modulation, and APL = 50 %.
SYNC chip level 2	$V_{sync(L)}$	2.5	2.9	3.2	V	V_{ip} = 90 dBμ, f_o = 32.7 MHz (L-SECAM) 94 % video modulation, and APL = 50 %.
PAL sync ratio	$SR_{(B)}$	26	29	32	%	(Black level − sync level)/V_o(P) x 100 (B/G mode)
SECAM sync ratio	$SR_{(L)}$	28	30	32	%	(Black level − sync level)/2 x 100 (L mode)
Input resistance	$R_{in(V)}$		1		kΩ	
Input capacitance	$C_{in(V)}$		4		pF	
Horizontal oscillation starting voltage	V_{ccmin}		4	5.0	V	
Horizontal free run frequency	f_H	15.25	15.625	16.0	kHz	
Horizontal pulling range	f_{PL}	310	445		Hz	V_{ip} = 90 dBμ (L mode)
Horizontal pulling range	f_{PH}	374	423		Hz	V_{ip} = 90 dBμ (L mode)
G/L switch threshold level	V_{TH}	1.5	2.0	2.5	V	Voltage of pin 29 when the video output is reversed.
SECAM AFT detector sensitivity	μ-S	60	90		mV/kHz	V_{ip} = 90 dBμ, f_o = 32.7 MHz (L mode), 94 % video modulation, and white = 100 %.
Maximum AFT voltage S	V_{20H-S}	8.0	8.7		V	V_{ip} = 90 dBμ, f_o = 32.7 MHz (L mode), 94 % video modulation, and white = 100 %.
Minimum AFT voltage S	V_{20L-S}		0.24	0.80	V	V_{ip} = 90 dBμ, f_o = 32.7 MHz (L mode), 94 % video modulation, and white = 100 %.
RF AGC temperature characteristics	RFAGC ΔTa		3	6	dB	V_{ip} = 90 dBμ, f_o = 32.7 MHz, 87.5 % video modulation, and APL = 50 %.
SIF DET input sensitivity	V_{is}SENSE		69	73	dBμ	V_{ip} = 90 dBμ SIF input voltage when V_o(S) has decreased by 3 dB as the input SIF voltage was gradually reduced.
SIF DET maximum output voltage	V_o(S)	158 104	282 109	502 114	mV dBμ	V_{ip} = 90 dBμ SIF output voltage when V_o(S) has limited by the SIF input voltage was gradually increased.
Horizontal oscillation output voltage	V_o(H)	0.60	0.70	0.80	V_{p-p}	Pin 17 output voltage when horizontal free-running frequency.

MEASURING CIRCUIT 1



MEASURING CIRCUIT 2



MEASURING CIRCUIT SWITCHES

No.	Symbol	Measuring circuit	Measuring conditions																												Remarks
			S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	TP 1	TP 2	TP 3	TP 4	TP 5	TP 6	TP 7	TP 8	TP 9	TP 10	TP 11	TP 12	TP 13	TP 14	TP 15	TP 16	TP 17	TP 18	TP 19		
1	I_{CC}	1	1	1	1	1	2	1	1	1										M(+)	M(−)										Note 1
2	$v_{0(B)}$	1	1	1	1	1	1	1	1	1					SG_1											M					Note 2
3	$v_{0(L)}$	1	1	1	1	1	1	1	1	1					SG_9											M					Note 3
4	$V_{1(B)}$	1	1	1	1	1	1	1	1	1	M																				TP19 = 0 V
5	$V_{1(L)}$	1	1	1	1	1	1	1	1	1	M																				TP19 = 4 V
6	$V_{26(B)}$	1	1	1	1	1	1	1	1	1																M					TP19 = 0 V
7	$V_{26(L)}$	1	1	1	1	1	1	1	1	1																M					TP19 = 4 V
8	P/N	1	1	1	1	1	1	1	1	2					SG_2										M						Note 4
9	$BW_{(B)}$	1	1	1	1	1	1	1	1	1	(M)				SG_3																Note 5
10	v_{ip} SENSE	1	1	1	1	1	1	1	1	1					SG_9											M					Note 6
11	v_{ip} MAX.	1	1	1	1	1	1	1	1	1					SG_9											M					Note 7
12	μ-1	1	1	1	1	1	1	1	1	1					SG_4								M								Note 8
13	V_{20H-1}	1	1	1	1	1	1	1	1	1					SG_4								M								Note 9
14	V_{20L-1}	1	1	1	1	1	1	1	1	1					SG_4								M								Note 10
15	V_{20TH}	1	1	1	1	2	1	1	1	1					SG_4								M								
16	I_{19DEF}	1	1	1	1	1	1	1	1	1							M														Note 11
17	V_{5TH}	1	1	3	1	1	1	1	1	1					SG_4			M					P								Note 12
18	μ-2	1	1	2	1	1	1	1	1	1					SG_4								M								Note 13
19	V_{20H-2}	1	1	2	1	1	1	1	1	1					SG_4								M								Note 14
20	V_{20L-2}	1	1	2	1	1	1	1	1	1					SG_4								M								Note 15
21	V_{3H}	1	1	1	1	1	1	1	1	1			M																		
22	V_{3L}	1	1	1	1	1	1	1	1	1			M		SG_9																Note 16
23	V_{2H}	1	1	1	1	1	1	1	1	1		M			SG_1																Note 17
24	V_{2L}	1	1	1	1	1	1	1	1	1		M			SG_1																Note 18
25	f_{CLU-1}	1	1	1	2	1	1	1	1	1				4.5 V	SG_1											P					Note 19
26	f_{CLL-1}	1	1	1	2	1	1	1	1	1				4.5 V	SG_1											P					Note 20
27	f_{CLU-2}	1	1	1	2	1	1	1	1	1				4.0 V	SG_1											P					Note 21
28	f_{CLL-2}	1	1	1	2	1	1	1	1	1				4.0 V	SG_1											P					Note 22

No.	Symbol	Measuring circuit	Measuring conditions																												Remarks
			S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	TP 1	TP 2	TP 3	TP 4	TP 5	TP 6	TP 7	TP 8	TP 9	TP 10	TP 11	TP 12	TP 13	TP 14	TP 15	TP 16	TP 17	TP 18	TP 19	
29	V_{6TH}	1	1	1	2	1	1	1	2	1				M													P		Note 23
30	FC1	1	1	1	1	1	1	1	1	1	(M)				SG_3										M				Note 24
31	FC2	1	1	1	1	1	1	1	1	1	(M)				SG_3										M				Note 24
32	FC3	1	1	1	1	1	1	1	1	1	(M)				SG_3										M				Note 24
33	IM	1	2	1	1	1	1	1	1	1	(M)				SG_5														Note 25
34	DG	1	1	1	1	1	1	1	1	1					SG_1									M					Note 26
35	DP	1	1	1	1	1	1	1	1	1					SG_1									M					Note 27
36	$V_{sync(B)}$	1	1	1	1	1	1	1	1	1					SG_1										M				Note 28
37	$V_{sync(L)}$	1	1	1	1	1	1	1	1	1					SG_9										M				Note 29
38	$SR_{(B)}$	1	1	1	1	1	1	1	1	1					SG_1										M				Note 30
39	$SR_{(L)}$	1	1	1	1	1	1	1	1	1					SG_9										M				Note 31
40	$R_{in(V)}$	2																											
41	$C_{in(V)}$	2																											
42	$V_{ccmin.}$	1	1	1	1	1	1	2	1	1											M								Note 32
43	f_H	1	1	1	1	1	1	2	1	1											M								Note 33
44	f_{PL}	1	1	1	1	1	1	1	1	1					SG_6						M				P				Note 34
45	f_{PH}	1	1	1	1	1	1	1	1	1					SG_6						M				P				Note 35
46	V_{TH}	1	1	1	1	1	1	1	1	1					SG_1										P			M	Note 36
47	μ-s	1	1	1	1	1	1	1	1	1					SG_7								M						Note 37
48	V_{20H-S}	1	1	1	1	1	1	1	1	1					SG_7								M						Note 38
49	V_{20L-S}	1	1	1	1	1	1	1	1	1					SG_7								M						Note 39
50	RF AGC ΔT_a	1	1	1	1	1	1	1	1	1		M			SG_1														Note 40
51	v_{is} SENSE	1	1	1	1	1	1	1	1	1					SG_1	SG_8			M										Note 41
52	$v_{O(S)}$	1	1	1	1	1	1	1	1	1					SG_1	SG_8			M										Note 42
53	$v_{O(H)}$	1	1	1	1	1	1	2	1	1											M								Note 43

Signal Sources

SG1 B/G system, modulation ratio 87.5 %, Stair 10 steps (no chrominance signal)
V_{ip} = 90 dBμ, f_O = 32.7 MHz, APL = 50 %

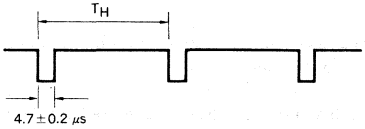
SG2 L system, modulation ratio 94 %, white 100 % signal
V_{ip} = 90 dBμ, f_O = 32.7 MHz

SG3 CW mixed waves
f_1 = 32.7 MHz, V_{ip} = 90 dBμ
f_2 = 32.7 MHz + Δf V_{ip} = 60 dBμ
Δf is 0.5 to 10 MHz.

SG4 B/G system, modulation ratio 87.5 % or equivalent, black video signal
V_{ip} = 90 dBμ, f_O = 32.7 MHz

SG5 CW mixed waves:
f_1 = 32.7 MHz, V_{ip} = 90 dBμ
f_2 = 32.106 MHz, V_{ip} = 80 dBμ
f_3 = 39.2 MHz, V_{ip} = 80 dBμ

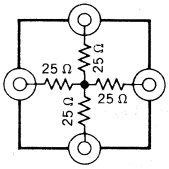
SG6 32.7 MHz modulated waves added by the following pulse to L system modulation signal



– T_H is variable around 64 μs at lock range measurement.
– The horizontal frequency is 1/TH.

SG7 L system, modulation ratio 94 %, white 100 % video signal
V_{ip} = 90 dBμ, f_O = 32.7 MHz

SG8 CW wave 38.2 MHz
About mixed waves



Use the mixer shown on the left for SG3, SG5, and SG6.
Terminate the one remaining pin in SG3 and SG5 with 50 ohms.
◎ is a BNC connector.

SG9 L system, modulation ratio 94 %, Stair 10 steps
V_{ip} = 90 dBμ, f_O = 32.7 MHz

NOTES

Note 1: Connect the plus (+) side of the ammeter to TP10 and the minus (−) side to TP11.

Note 2: Adjust VR2 to set TP19 to 0 V, connect SG1 to TP5 (BNC), then measure the amplitude from white 100 % to the leading tip of the sync signal at TP16 with an oscilloscope.

Note 3: Connect SG9 to TP9 (BNC) and measure the amplitude from white 100 % to the leading tip of the sync signal at TP16 with an oscilloscope.

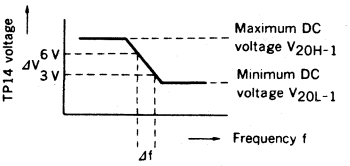
Note 4: Input SG2 to TP5 (BNC) and inputs the TP15 (BNC) output to the PAL noise meter.

Note 5: a. Set SG3 as shown below.
Mixed waves:
f_1 = 32.7 MHz, V_{ip} = 90 dBμ
f_2 = 33.2 MHz, V_{ip} = 60 dBμ
b. Measure the 0.5 MHz component at pin 1 of the DUT.
c. Increase frequency f_2 unitl ($f_1 - f_2$) at pin 1 of the DUT decreases 3 dB to V_i, then read the frequency.
d. $BW_{(B)} = f_2 - 32.7$ (MHz)

Note 6: Connect an oscilloscope to TP16. Set the SG9 output to 90 dBμ then adjust the TP16 output to 2 V_{p-p}. Increase the SG9 output from 90 dBμ until the TP16 output decreases 3 dB (approx. 1.4 V_{p-p}). The output level at this time is $V_{ip\ SENSE}$.

Note 7: Similar to Note 6, adjust the TP16 output level, then increase the SG9 output until the TP16 output decreases 1 dB (approx. 1.78 V_{p-p}). The output level at this time is $V_{ip\ MAX}$.

Note 8: Adjust VR2 to set the TP19 voltage to 0 V, input the SG4 signal to TP5 (BNC), and connect an ammeter to TP14. While reading the ammeter, change the SG4 frequency from 27.7 MHz to 37.7 MHz. The AFT sensitivity is defined as shown below on the curve obtained at this time.



AFT detection sensitivity μ-1 = $\frac{\Delta V}{\Delta f}$ (mV/kHz)

Note 9: The maximum DC voltage shown in Note 8 is stated as V_{20H-1}.

Note 10: The minimum DC voltage shown in Note 8 is stated as V_{20L-1}.

Note 11: Connect the plus (+) side of the ammeter to TP7 and the minus (−) side to GND.

Note 12: Connect an ammeter to TP8 and TP14 and adjust VR1 to increase the TP8 voltage from the minimum value. V_{5TH} is the TP8 voltage when the TP14 polarity changes.

Note 13: AFT sensitivity measurement procedures are the same as in Note 8. Define μ-2 as follows:

$$\mu\text{-}2 = \frac{\mu\text{-}1}{\text{Measured value}} \times 100\ (\%)$$

Note 14: Curve when the polarity in Note 8 is reversed. Same as AFT maximum voltage 1.

Note 15: Curve when the polarity in Note 8 is reversed. Same as AFT minimum voltage 1.

Note 16: Input SG9 to TR5 (BNC) and an ammeter to TP3. The TP3 voltage when the SG9 output becomes the maximum capacitance is the IF AGC minimum voltage.

Note 17: Connect SG1 to TR5 (BNC) and an ammeter to pin 4 of the DUT and adjust VR3 to 3.09 V. Connect TP2 to the ammeter and measure the TP2 voltage when the SG1 output becomes 70 dBμV. This voltage is the RF AGC maximum voltage.

Note 18: The TP2 voltage when the SG1 output becomes 90 dBμ in Note 17 is the RF AGC minimum voltage.

Note 19: Connect an oscilloscope to TP16. Adjust VR1 and set the TP4 voltage to 4.5 V, then increase the SG1 frequency while reading the TP16 waveforms until the VCO is unlocked. Decrease the SG1 frequency until the VCO is locked. This frequency is $f_{CLU\text{-}1}$.

Note 20: Decrease the SG1 frequency until VCO is unlocked in Note 19. Then, increase the frequency until the VCO is locked. This frequency is $f_{CLL\text{-}1}$.

Note 21: Set the TP4 voltage to 4.0 V and perform the same steps as in Note 19. The measured value is $f_{CLU\text{-}2}$.

Note 22: Set the TP4 voltage to 4.0 V and perform the same steps as in Note 20. The measured value is $f_{CLL\text{-}2}$.

Note 23: Connect an ammeter to TP4 and an oscilloscope to TP18 and adjust VR1 to decrease the TP4 voltage from the maximum value. The TP4 voltage when the TP18 voltage changes from high to low is the lock detection threshold voltage.

Note 24: Connect SG3 to TP5 (BNC) and observe the Δf signal level of pin 1 of the DUT with a spectrum analyzer. Then, observe the Δf signal level of TP16. The EQ frequency characteristic is the TP16 level minus the level of pin 1 of the DUT.

Note 25: Input SG5 to TP5 (BNC), observe TP16, and adjust VR1 so that the TP16 wave becomes the minimum. The level at pin 1 of the DUT (4.406 MHz level to 2.094 MHz level) is the inter-modulation.

Note 26: Add a chrominance signal in SG1 and input to TP5 (BNC). Connect TP15 (BNC) to a vector scope to measure in DG mode.

Note 27: Observe in DP mode in the same way as in Note 26.

Note 28: Connect S1 to TP5 (BNC) and an oscilloscope to TP16. Adjust VR2 so that the TP19 voltage becomes 0 V. The sync level observed at TP16 at this time is the sync chip level 1.

Note 29: Connect SG9 to TP5 (BNC) and an oscilloscope to TP16. Adjust the TP19 voltage with VR2 so that the TP16 output reaches 2 $V_{p\text{-}p}$. The sync level observed at this time is the sync chip level 2.

Note 30: The PAL sync ratio is found by the following expression in Note 28:
(Black level – sync level)/output voltage of pin 16 x 100 (%)

Note 31: The SECAM sync ratio is found by the following expression in Note 29:
(Black level – sync level)/2 x 100 (%)

Note 32: Connect an oscilloscope to TP12 and increase V_{CC} from 0 V. The V_{CC} voltage when the waveform of the TP12 output becomes 2 μs cycles is V_{CC} min.

Note 33: Connect a spectrum analyzer to TP12, read the value, and divide it by 32. This value is the horizontal free-run frequency.

Note 34: Input SG6 to TP5 (BNC), and connect a spectrum analyzer to TP12 and an oscilloscope to TP16. Increase the SG6 cycle T_H until the VCO is unlocked, then decrease until the VCO is locked. Read the spectrum analyzer at this time and divide the read value by 32. The horizontal pull-in range (f_{PL}) is the difference between the obtained value and 15.625 kHz.

Note 35: Connect in the same way as in Note 34. Increase the SG6 cycle T_H until the VCO is unlocked, then decrease until the VCO is locked. Read the spectrum analyzer at this time and divide the read value by 32. The horizontal pull-in range (f_{PH}) is the difference between the obtained value and 15.625 kHz.

Note 36: Connect the oscilloscope to TP16 and an ammeter to TP19. Adjust VR2 to increase the TP19 voltage from 0 V until the TP waveforms are reversed. This TP19 voltage is the G/L switch threshold voltage.

Note 37: Input SG7 to TP5 (BNC) and connect an ammeter to TP14. Measure in the same way as in Note 8.

Note 38: Maximum AFT output voltage when the SG7 frequency is variable in Note 37. Measurement procedures are the same as in Note 9.

Note 39: Minimum AFT output voltage when the SG7 frequency is variable in Note 37. Measurement procedures are the same as in Note 10.

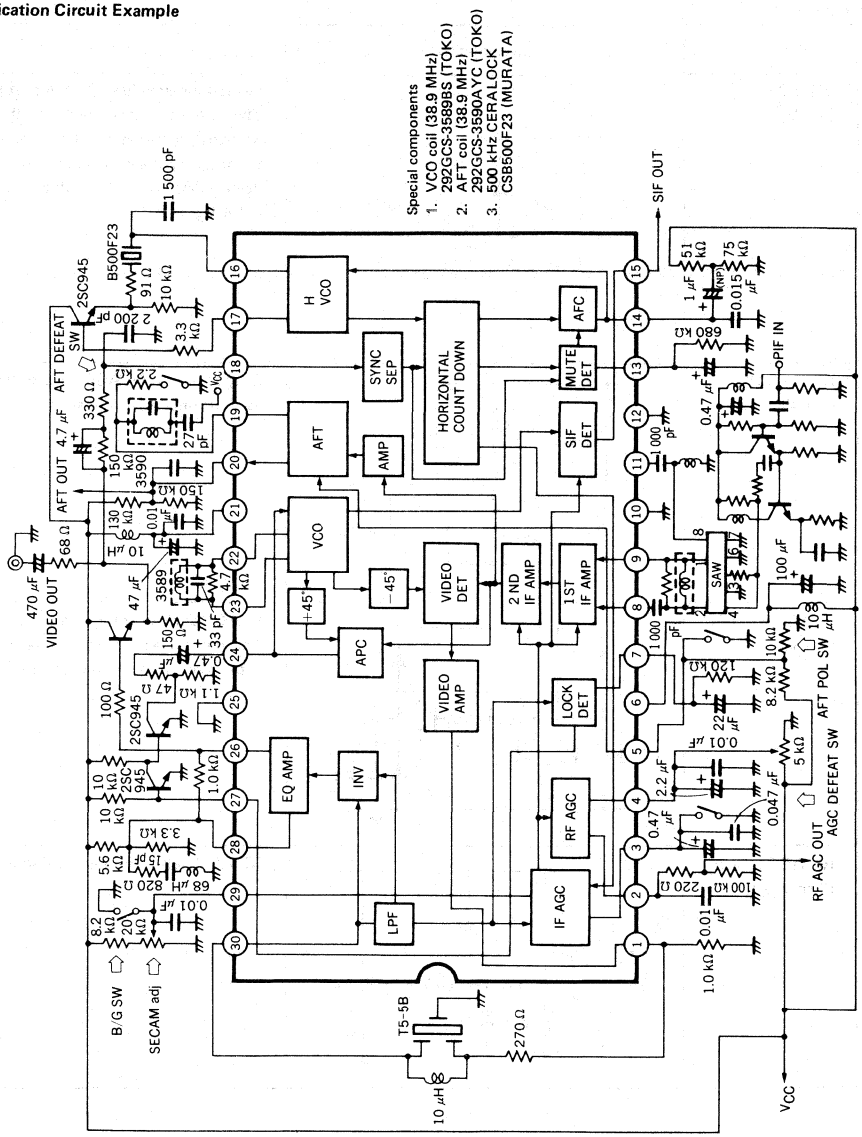
Note 40: Input SG1 to TP5 (BNC) and connect an ammeter to TP2. Change the ambient temperature T_a from −25 °C to 75 °C. The input level displacement required to change the TP2 output level is the RF AGC temperature characteristics.

Note 41: Input SG1 to TP5 (BNC), and connect SG8 to TP6 (BNC) and a spectrum analyzer to TP9. Increase the SG8 signal level until the TP9 output voltage reaches the SIF DET maximum output voltage. Next, decrease the SG8 signal level until the TP9 output voltage decreases 3 dB. The signal level at this time is the SIF DET input sensitivity.

Note 42: Input SG1 to TP5 (BNC), and connect SG8 to TP6 (BNC) and a spectrum analyzer to TP9. Increase the SG8 signal level until the TP9 output voltage is saturated. The voltage at this time is the SIF DET maximum output voltage.

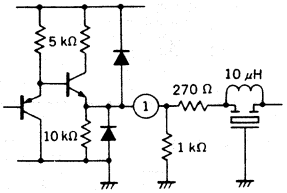
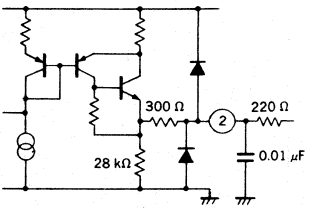
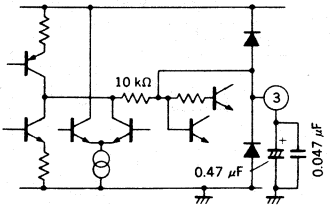
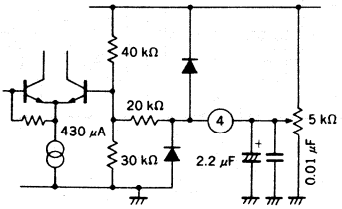
Note 43: Connect an oscilloscope to TP12.

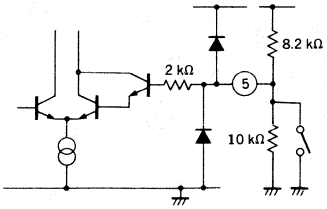
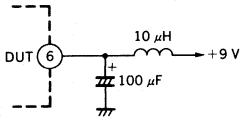
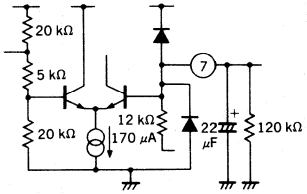
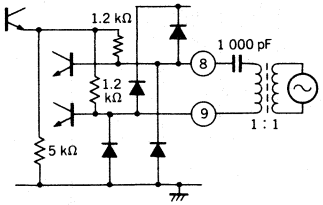
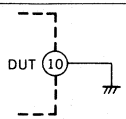
Application Circuit Example

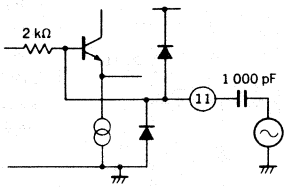
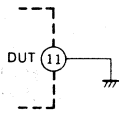
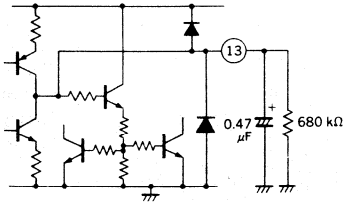
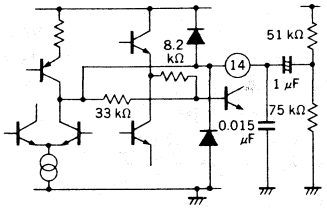
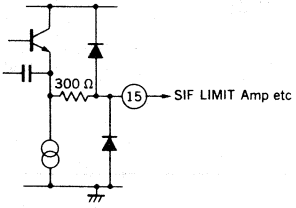


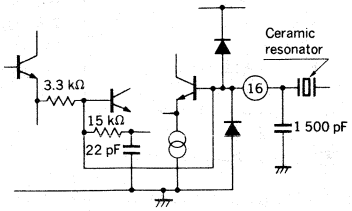
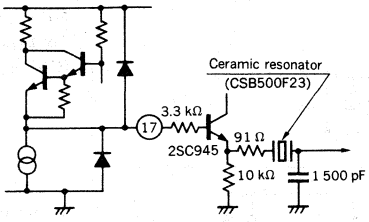
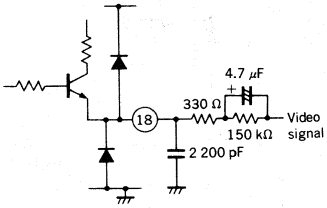
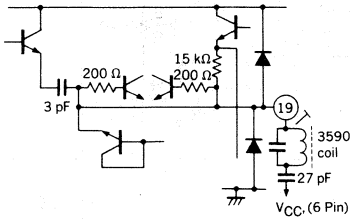
The application circuit and circuit constants are examples and do not apply to mass production.

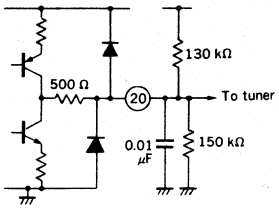
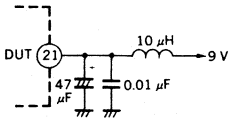
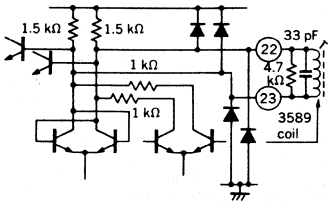
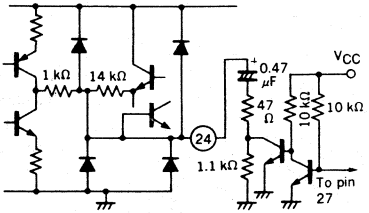
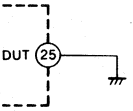
Pin Description

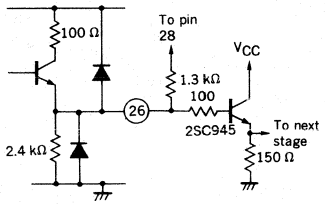
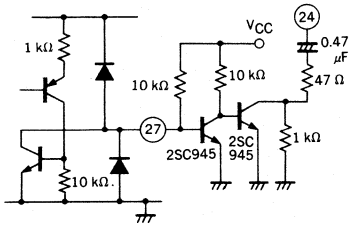
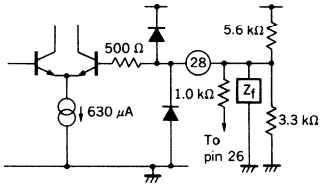
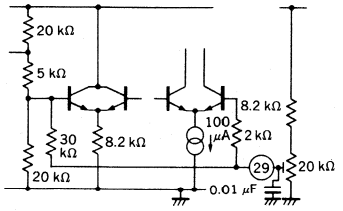
Pin No.	Pin name	Equivalent circuit	Function
1	VIDEO OUT (4.9 V)		Demodulated video signal output pin. The voltage is approximately 4.9 V at no signal; the level of the leading edge tip of the sync signal is 3.3 V at demodulation; and the video amplitude is 1.4 $V_{p\text{-}p}$.
2	RF AGC OUT (8.1 V)		Output pin of RF AGC control signal used as tuner AGC signal
3	IF AGC FILTER (8.5 V)		IF AGC control voltage smooth pin. This pin is used to set the time constant depending on external capacity.
4	RF AGC DELAY (0 to V_{CC})		RF AGC delay point control input pin

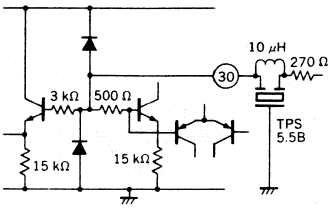
Pin No.	Pin name	Equivalent circuit	Function
5	AFT POLARITY (0 to 5 V)		AFT output polarity switch input pin to PIF input frequency. The threshold voltage is 2.7 V and the PIF input frequency to AFT output voltage is positive at high level and negative at low level.
6	V_{CC}		Power supply pin for AFT, H VCO, and IF/RF AGC. Use at 8 to 10 V (9 V, typ.).
7	LOCK DET FILTER (4.9 V)		Lock detector smooth pin. This pin is used to set the LOCK SW time constant. The input impedance is approximately 12 k-ohms.
8 9	PIF IN (2.2 V)		PIF signal input pin. The input impedance is approximately 1 k-ohms.
10	GND		GND pin for PIF amplifier SIF DET.

Pin No.	Pin name	Equivalent circuit	Function
11	SIF DET IN (4.0 V)		SIF DET input pin. The input impedance is approximately 2 k-ohms.
12	GND		GND pin for AFT, H/VCO, and RF/IF AGC
13	CONCIDENCE FILTER (0 V)		Filter pin used to detect the horizontal VCO (H/VCO) sync mode. The signal goes low when the horizontal PLL is unlocked.
14	AFC FILTER (5.3 V)		AFC filter pin. Use a 1 μF external electrolytic capacitor with no polarity.
15	SIF DET OUT (7.65 V)		SIF split carrier output pin. The maximum output voltage is approximately 300 $mV_{p\text{-}p}$.

Pin No.	Pin name	Equivalent circuit	Function
16	H/OSC IN (3.9 V)		Horizontal VCO oscillation input pin. The input impedance is approximately 2.9 k-ohms.
17	H/OSC OUT (7.2 V)		Horizontal VCO oscillator output pin. The output voltage is 270 mV_{p-p} (typ.).
18	SYNC SEPA IN (6.7 V)		Sync separator input pin. The bias voltage is approximately 6.7 V.
19	AFT COIL (5.4 V)		AFT phase control pin. The opposite side of the capacitor connected with the AFT coil is connected to pin 6 (V_{CC}).

Pin No.	Pin name	Equivalent circuit	Function
20	AFT OUT (4.7 V)		AFT output pin. The output voltage is 0.8 to 8 V. The sensitivity is adjustable depending on the external resistor.
21	V_{CC}		Power supply pin for PIF/PLL VCO APC. For bypass capacitor GND, use the same GND as pin 25.
22 23	VCO COIL (7.8 V)		PLL VCO oscillator coil pin. Set the dumping resistor to 4.7 k-ohms or more.
24	APC FILTER (4.5 V)		PLL VCO control voltage filter pin
25	GND		GND pin for PLL VCO, APC, and SIF DET

Pin No.	Pin name	Equivalent circuit	Function
26	EQ VIDEO OUT B/G (5.7 V) L (2.5 V)		Equalizer amplifier output pin. Use the video signal at 3.2 V at the sync edge and the amplitude under 2 $V_{p\text{-}p}$.
27	LOCK SW (OFF)		Pin used to switch the time constant of PLL VCO control voltage filter. The signal goes low impedance when PLL VCO is locked to IF carrier.
28	FEED BACK EQ B/G (4.9 V) L (2.9 V)		Equalizer amplifier blaking input pin. The frequency characteristics are adjustable by Z_f.
29	SECAM LEVEL (0 to 7 V)		Demodulation level control input pin at L system (positive modulation signal) modulation. Apply approximately 4.42 V. Set to 0 V at G/G system modulation. Use this control input pin between 0 to 7 V.

Pin No.	Pin name	Equivalent circuit	Function
30	EQ IN (4.9 V)		Equalizer amplifier input pin. The voltage is 4.9 V at no signal and 3.3 V at the sync edge of the video signal. The amplitude of the video signal is 1.4 $V_{p\text{-}p}$.

SYNCHRONOUS DEFLECTION LSI FOR MULTI-SYNC. DISPLAY TV RECEIVER

The μPC1880 is a silicon monolithic circuit designed for synchronous deflection processing of multi-sync. display TV receiver capable of coping with several kinds of personal computers. It incorporates all function circuits, – synchronous signal processing and horizontal/vertical oscillation, into a single chip.

This IC application can change the conventional multi-sync. TV receiver consisted of 7 or 8 ICs to a single-chip system. Therefore it enables you to reduce external components and miniaturize print board, providing a big fall cost down on the application.

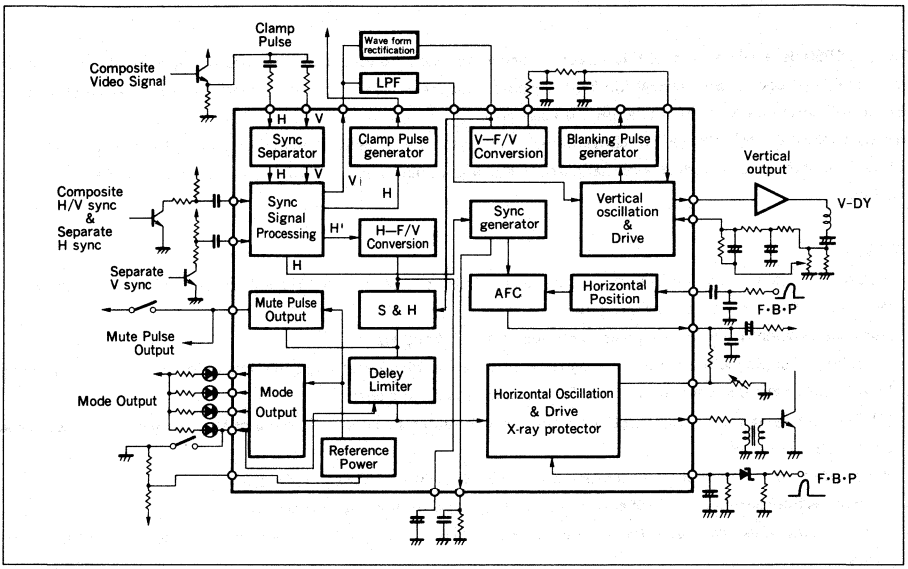
FEATURES

- Automatic switch to horizontal frequency between 15 kHz and 50 kHz/20 kHz and 60 kHz/30 kHz and 90 kHz (Horizontal frequency width is three times.)
- Automatic switch to vertical frequency between 40 Hz and 100 Hz
- Capability of coping with synchronous signal bi-polarity (positive/negative) at the time of input from personal computers
- Built-in automatic discrimination circuit for the following input signals;
  (1) Separate synchronous signal, (2) Composite synchronous signal and (3) composite video signal – These signals are discriminated in order.
- Built-in delay detector of chattering protection for mode switch of horizontal frequency
- Keeping vertical output amplitude constant even if input vertical frequency changes
- Built-in clamp pulse generator for automatic timing change at the time of input from TV receivers and personal computers
- Power supply voltage: 12 V

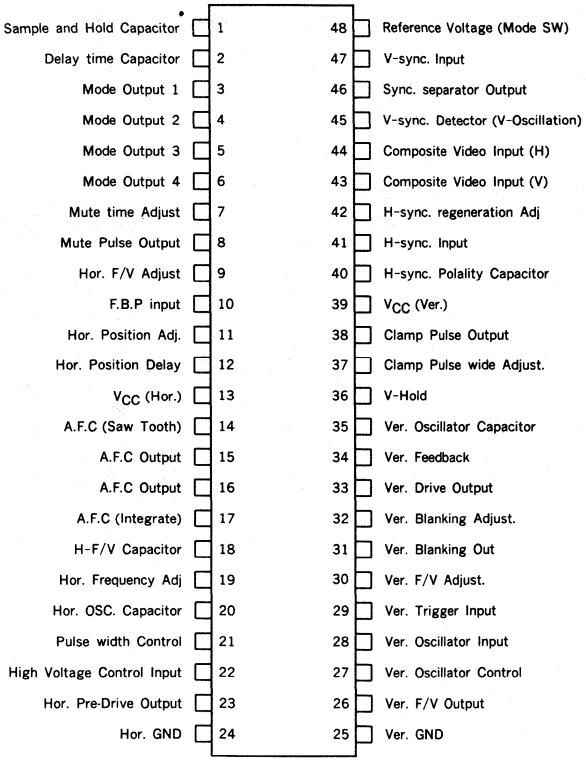
ORDERING INFORMATION

Part Number	Package
μPC1880CA	48 pin plastic shrink DIP (600 mil)

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



5

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power Supply Voltage	V_{CC} ($V_{13, 39}$)	13.5	V
Horizontal Pulse Output Current	I_{23}	10	mA
Vertical Drive Output Current	I_{33}	10	mA
Mode Output Current	$I_{3, 4, 5, 6}$	30	mA
Separate Sync. Input Voltage (H)	V_{41}	6	V_{p-p}
Separate Sync. Input Voltage (V)	V_{47}	6	V_{p-p}
Vertical Blanking Output Current	I_{31}	3	mA
Clamp Pulse Output Current	I_{38}	3	mA
Power Dissipation	P_D: T_a = 75 °C	1.25	W
Operating Temperature	T_{opt}	−10 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Horizontal Power Supply Voltage	V_{13}	11	12	13	V
Vertical Power Supply Voltage	V_{39}	11	12	13	V
Composite Video Input Voltage	$V_{43, 44}$		2		V_{p-p}
Separation Sync. Input Voltage (H)	V_{41}	2	4	5	V_{p-p}
Separation Sync. Input Voltage (V)	V_{47}	2	4	5	V_{p-p}
Mode Output Current	$I_{3, 4, 5, 6}$		10	30	mA
Horizontal Operating Frequency Range	f_H	15 20 30		50 60 90	kHz
Vertical Operating Frequency Range	f_V	40		120	Hz

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, RH = 70 %)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITION
[Synchronous Part]							
Discrimination of Horizontal Synchronization (1)	HSP_1	1.0	–	22	μs	1	f_H = 15.75 kHz Capable Sync. Pulse Width (Negative sync.)
Discrimination of Horizontal Synchronization (2)	HSP_2	1.0	–	22	μs	1	f_H = 15.75 kHz Capable Sync. Pulse Width (Positive sync.)
Discrimination of Horizontal Synchronization (3)	HSP_3	1.0	–	22	μs	2	f_H = 30 kHz Capable Sync. Pulse Width (Negative sync.)
Discrimination of Horizontal Synchronization (4)	HSP_4	1.0	–	22	μs	2	f_H = 30 kHz Capable Sync. Pulse Width (Positive sync.)
Discrimination of Vertical Synchronization (1)	VSP_1	1	–	55	H	1	f_V = 60 Hz Capable Sync. Pulse Width (Negative sync.)
Discrimination of Vertical Synchronization (2)	VSP_2	1	–	55	H	1	f_V = 60 Hz Capable Sync. Pulse Width (Negative sync.)
Clamp Pulse Timing (1)	CLt_1	0.14	0.24	0.34	μs	1	Between clamp pulse start and H. Sync. rise-time
Clamp Pulse Timing (2)	CLt_2	0.14	0.24	0.34	μs	1	Between clamp pulse end and H. Sync. rise-time
Clamp Pulse Width	CLW	2.3	2.5	2.7	μs	1	
H. Sync. Output Pulse Voltage (1)	$HSPV_1$	9	10	11	μs	1	Only H. Sync = –15 dB, f_H = 15.75 kHz
H. Sync. Output Pulse Width (1)	$HSPW_1$	–	4.5	5.5	μs	1	Only H. Sync = –15 dB, f_H = 15.75 kHz
H. Sync. Output Pulse Voltage (2)	$HSPV_2$	9	10	11	μs	2	Only H. Sync = –15 dB, f_H = 30 kHz
H. Sync. Output Pulse Width (2)	$HSPW_2$	–	4.5	5.5	μs	2	Only H. Sync = –15 dB, f_H = 30 kHz
V. Sync. Output Pulse Voltage	VSPV	9	10	11	V	1	Only V. Sync = –5 dB, f_V = 60 Hz
V. Sync. Output Pulse Width	VSPW	–	185	220	μs	1	Only V. Sync = –5 dB, f_V = 60 Hz
Synchronous Signal Output Pulse Voltage (1)	SPV_1	9	10	11	V	1	Composite Sync. = –11 dB, f_H = 15.75 kHz
Synchronous Signal Output Pulse Width (1)	SPW_2	–	4.7	5.2	μs	1	Composite Sync. = –11 dB, f_H = 15.75 kHz
Synchronous Signal Output Pulse Voltage (2)	SPV_2	9	10	11	V	2	Composite Sync. = –11 dB, f_H = 30 kHz
Synchronous Signal Output Pulse Width (2)	SPW_2	–	4.7	5.2	μs	2	Composite Sync. = –11 dB, f_H = 30 kHz
[Horizontal Part]							
Power Supply Current	I_{13}	25	35	47	mA	1	No signal
F/V Converter Linearity ERROR (1)	$H.F/V_1$	–	±0.5	±1.0	%	1	f_H = 30 kHz Input, f_H = 10 kHz Standard
F/V Converter Linearity ERROR (2)	$H.F/V_2$	–	±1.0	±2.0	%	1	f_H = 50 kHz Input, f_H = 10 kHz Standard
F/V Converter Linearity ERROR (3)	$H.F/V_3$	–	±1.0	±2.0	%	1	f_H = 30 kHz Input, T_a = –10 to +60 °C
F/V Converter Linearity ERROR (4)	$H.F/V_4$	–	±0.5	±1.0	%	2	f_H = 60 kHz Input, f_H = 30 kHz Standard
F/V Converter Linearity ERROR (5)	$H.F/V_5$	–	±1.0	±2.5	%	2	f_H = 90 kHz Input, f_H = 30 kHz Standard
F/V Converter Linearity (1)	$H.\Delta F/V_1$	0.155	0.170	0.185	V/kHz	1	$\Delta V/\Delta F$, Slope between 20 kHz and 40 kHz (= f_H) f_H = 15.75 kHz
F/V Converter Linearity (2)	$H.\Delta F/V_2$	0.088	0.097	0.106	V/kHz	2	$\Delta V/\Delta F$, Slope between 30 kHz and 90 kHz
Sample and HOLD (1)	$S\cdot H_1$	–0.4	–0.1	0	%	1	f_H = 15.75 kHz
Sample and HOLD (2)	$S\cdot H_2$	–0.8	–0.2	0	%	2	f_H = 30 kHz
Delay Characteristics (1)	DL_1	1.0	1.5	2.0	s	1	Input f_H: 15.75 kHz → 50 kHz
Delay Characteristics (2)	DL_2	2.0	3.0	4.0	s	1	Input f_H: 50 kHz → 15.75 kHz

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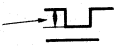
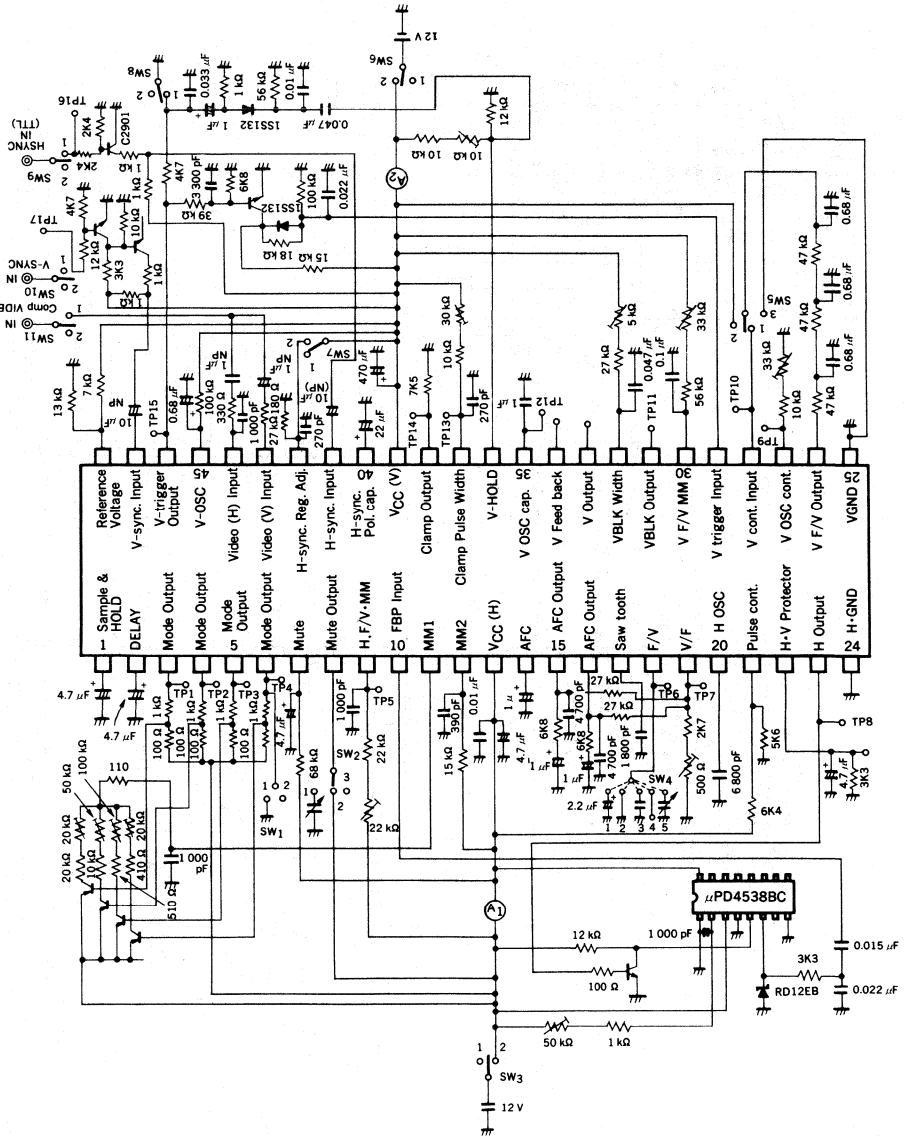
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITION
Delay Characteristics (3)	DL_3	1.0	1.5	2.0	s	2	Input f_H: 30 kHz → 90 kHz
Delay Characteristics (4)	DL_4	2.0	3.0	4.0	s	2	Input f_H: 90 kHz → 30 kHz
f_H Mode Switch Threshold (1)	MOC_1	3.3	3.4	3.5	V	1	At the time of switching f_H to 1.5 f_H
f_H Mode Switch Threshold (2)	MOC_2	4.55	4.70	4.85	V	1	At the time of switching 1.5 f_H
f_H Mode Switch Threshold (3)	MOC_3	5.9	6.1	6.3	V	1	At the time of switching 2.0 f_H
f_H Mode Detection Hysteresis (1)	MOH_1	0.13	0.16	0.19	V	1	At the time of switching f_H to 1.5 f_H (Pin 18)
f_H Mode Detection Hysteresis (2)	MOH_2	0.13	0.16	0.19	V	1	At the time of switching 1.5 f_H to 2.0 f_H (Pin 18)
f_H Mode Detection Hysteresis (3)	MOH_3	0.13	0.16	0.19	V	1	At the time of switching 2.0 f_H to 2.5 f_H (Pin 18)
f_H Mode Terminal Output Saturation Voltage (1)	MOV(1)	–	0.4	1.0	V	1	$I_{(3,4,5)out}$ = 10 mA Pin 3, 4 and 5 each same
f_H Mode Terminal Output Saturation Voltage (2)	MOV(2)	–	2.5	3.2	V	1	$I_{(6)out}$ = 10 mA, Pin 6
AFC Cut Operating Voltage	AF OFF	11.0	11.4	V_{CC}	V	1	Starting voltage when charging voltage to Pin 8 changes from 0 V to V_{OC} AFC operations turns off.
Mute Pulse Width (1)	MPW_1	210	230	250	ms	1	Pin 7; C = 4.7 μ, R = 68 kΩ Input f_H → 1.5 f_H
Mute Pulse Width (2)	MPW_2	210	230	250	ms	1	Pin 7; C = 4.7 μ, R = 68 kΩ Input 1.5 f_H → 2.0 f_H
Mute Pulse Width (3)	MPW_3	210	230	250	ms	1	Pin 7; C = 4.7 μ, R = 68 kΩ Input 2.0 f_H → 2.5 f_H
Mute Pulse Voltage	MPV	5.8	6.3	6.8	V_{p-p}	1	8 Pin Pulse Height 
Mute Pulse Output Voltage	MPOV	–	120	300	mV	1	8 Pin Pulse Voltage (Low) 
AFC Capture Range (1)	f_{PH1}	±700	±900	±1100	Hz	1	H. duty = 7 %, f_H = 15.75 kHz
AFC Capture Range (2)	f_{PH2}	±700	±900	±1100	Hz	1	H. duty = 7 %, f_H = 23.625 kHz
AFC Capture Range (3)	f_{PH3}	±700	±900	±1100	Hz	1	H. duty = 7 %, f_H = 31.5 kHz
AFC Capture Range (4)	f_{PH4}	±700	±900	±1100	Hz	1	H. duty = 7 %, f_H = 39.375 kHz
AFC Capture Range (5)	f_{PH5}	±1000	±1300	±1600	Hz	1	H. sync. Width 4.4 μs, f_H = 23.625 kHz
AFC Capture Range (6)	f_{PH6}	±1300	±1600	±2000	Hz	1	H. sync. Width 4.4 μs, f_H = 31.5 kHz
AFC Capture Range (7)	f_{PH7}	±1500	±1900	±2300	Hz	1	H. sync. Width 4.4 μs, f_H = 39.375 kHz
AFC Capture Range (8)	f_{PH8}	±1.0	±2.0	±3.5	kHz	2	H. duty = 7 %, f_H = 30 kHz
AFC Capture Range (9)	f_{PH9}	±1.0	±2.0	±3.5	kHz	2	H. duty = 7 %, f_H = 46 kHz
AFC Capture Range (10)	f_{PH10}	±1.0	±2.0	±3.5	kHz	2	H. duty = 7 %, f_H = 60 kHz
AFC Capture Range (11)	f_{PH11}	±1.0	±2.0	±3.5	kHz	2	H. duty = 7 %, f_H = 75 kHz
AFC Capture Range (12)	f_{PH12}	±0.8	±1.3	±2.5	kHz	2	H. sync. Width 2.2 μs, f_H = 45 kHz
AFC Capture Range (13)	f_{PH13}	±0.8	±1.5	±2.5	kHz	2	H. sync. Width 2.2 μs, f_H = 60 kHz
AFC Capture Range (14)	f_{PH14}	±1.0	±1.7	±2.7	kHz	2	H. sync. Width 2.2 μs, f_H = 75 kHz
Free-run Frequency (1)	f_{HO1}	−400	0	+300	Hz	1	Frequency Error for f_H = 23.625 kHz
Free-run Frequency (2)	f_{HO2}	−400	0	+400	Hz	1	Frequency Error for f_H = 31.5 kHz
Free-run Frequency (3)	f_{HO3}	−600	0	+400	Hz	1	Frequency Error for f_H = 39.375 kHz
Free-run Frequency (4)	f_{HO4}	−400	0	+400	Hz	2	Frequency Error for f_H = 45 kHz

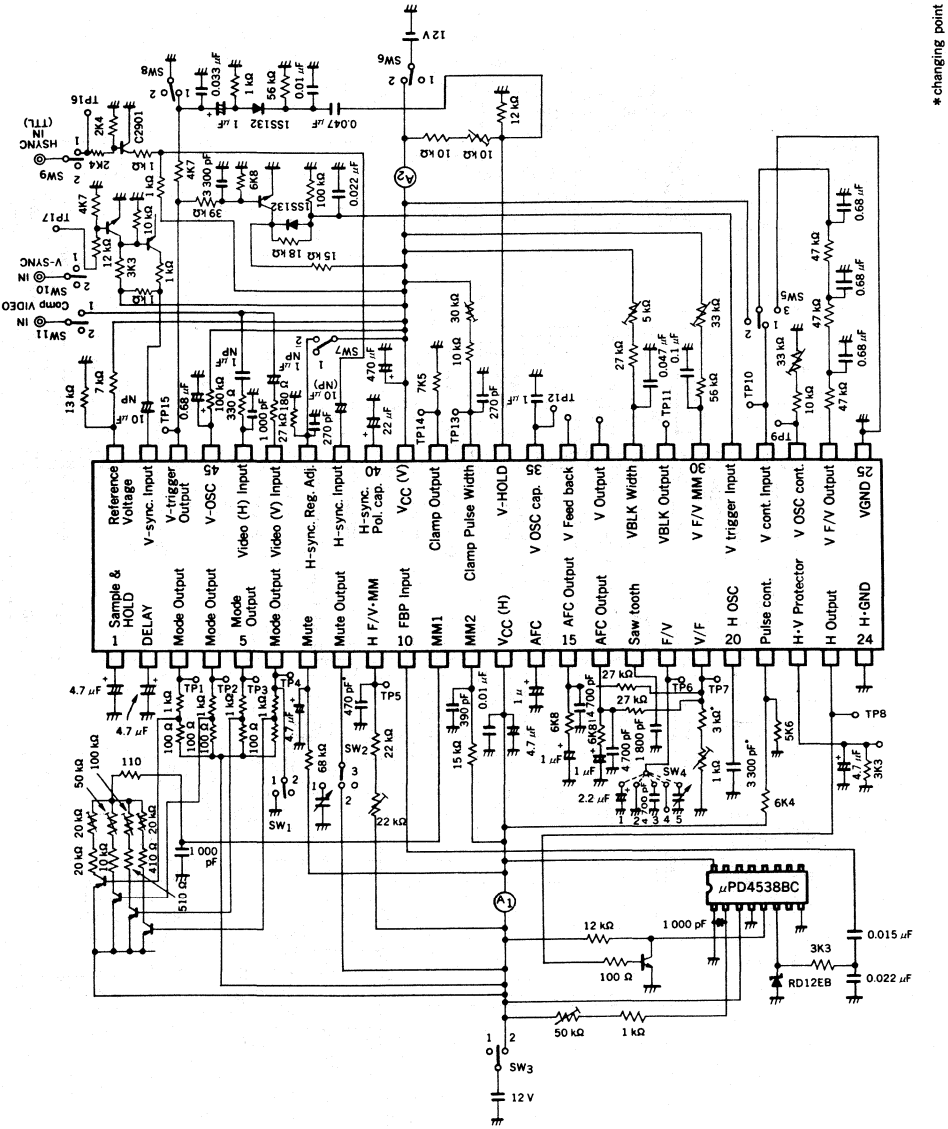
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITION
Free-run Frequency (5)	f_{HO5}	−600	0	+600	Hz	2	Frequency Error for f_H = 60 kHz
Free-run Frequency (6)	f_{HO6}	−800	0	+800	Hz	2	Frequency Error for f_H = 75 kHz
Free-run Frequency Power Supply Fluctuation (1)	$\Delta f_{H(V_{CC})}1$	–	150	300	Hz	1	$\Delta f_{H(V_{CC})}$ = | $f_{H(11\ V)} - f_{H(13\ V)}$ | f_H = 15.75 kHz
Free-run Frequency Power Supply Fluctuation (2)	$\Delta f_{H(V_{CC})}2$	–	280	450	Hz	1	Same as $\Delta f_{H(V_{CC})}1$, but f_H = 23.625 kHz
Free-run Frequency Power Supply Fluctuation (3)	$\Delta f_{H(V_{CC})}3$	–	380	550	Hz	1	Same as $\Delta f_{H(V_{CC})}1$, but f_H = 31.5 kHz
Free-run Frequency Power Supply Fluctuation (4)	$\Delta f_{H(V_{CC})}4$	–	500	700	Hz	1	Same as $\Delta f_{H(V_{CC})}1$, but f_H = 39.375 kHz
Free-run Frequency Power Supply Fluctuation (5)	$\Delta f_{H(V_{CC})}5$	–	300	500	Hz	2	$\Delta f_{H(V_{CC})}$ = | $f_{H(11\ V)} - f_{H\ (13\ V)}$ | f_H = 30 kHz
Free-run Frequency Power Supply Fluctuation (6)	$\Delta f_{H(V_{CC})}6$	–	450	700	Hz	2	Same as $\Delta f_{H(V_{CC})}1$, but f_H = 45 kHz
Free-run Frequency Power Supply Fluctuation (7)	$\Delta f_{H(V_{CC})}7$	–	600	900	Hz	2	Same as $\Delta f_{H(V_{CC})}1$, but f_H = 60 kHz
Free-run Frequency Power Supply Fluctuation (8)	$\Delta f_{H(V_{CC})}8$	–	750	1000	Hz	2	Same as $\Delta f_{H(V_{CC})}1$, but f_H = 75 kHz
Free-run Frequency Temperature Fluctuation (1)	$\Delta f_{H(T_a)}1$	–	200	300	Hz	1	$\Delta f_{H(T_a)}$ = | $f_{H(-10\ °C)} - f_{H(+60\ °C)}$ | f_H = 15.75 kHz
Free-run Frequency Temperature Fluctuation (2)	$\Delta f_{H(T_a)}2$	–	200	400	Hz	1	Same as $\Delta f_{H(T_a)}1$, but f_H = 23.625 kHz
Free-run Frequency Temperature Fluctuation (3)	$\Delta f_{H(T_a)}3$	–	300	450	Hz	1	Same as $\Delta f_{H(T_a)}1$, but f_H = 31.5 kHz
Free-run Frequency Temperature Fluctuation (4)	$\Delta f_{H(T_a)}4$	–	550	700	Hz	1	Same as $\Delta f_{H(T_a)}1$, but f_H = 39.375 kHz
Free-run Frequency Temperature Fluctuation (5)	$\Delta f_{H(T_a)}5$	–	400	600	Hz	2	$\Delta f_{H(T_a)}$ = | $f_{H(-10\ °C)} - f_{H(+60\ °C)}$ | f_H = 30 kHz
Free-run Frequency Temperature Fluctuation (6)	$\Delta f_{H(T_a)}6$	–	200	400	Hz	2	Same as $\Delta f_{H(T_a)}1$, but f_H = 45 kHz
Free-run Frequency Temperature Fluctuation (7)	$\Delta f_{H(T_a)}7$	–	300	450	Hz	2	Same as $\Delta f_{H(T_a)}1$, but f_H = 60 kHz
Free-run Frequency Temperature Fluctuation (8)	$\Delta f_{H(T_a)}8$	–	550	700	Hz	2	Same as $\Delta f_{H(T_a)}1$, but f_H = 75 kHz
Horizontal Oscillation	V_{23}	–	5.9	6.5	V	1	f_H = 15.75 kHz±1 kHz, (At the time of free-run)
Starting Hor. OSC Voltage	V_{23}	–	5.9	6.5	V	2	f_H = 30 kHz±1 kHz, (At the time of free-run)
H.V. Protection Threshold Voltage	V_{22}	0.53	0.63	0.73	V	1	Pin 22's voltage at Pin 23 output stop
Limiter Characteristics Voltage (low.)	HLL	2.55	2.65	2.75	V	1	SW4 → 2, SW1 → 2
Limiter Characteristics Voltage (high.) (1)	HLH_1	9.0	9.15	9.3	V	1	SW4 → 5, SW1 → 2
Limiter Characteristics Voltage (high.)	HLH_2	6.45	6.60	6.75	V	1	SW4 → 5, SW1 → 1
[Vertical Part]							
Power Supply Current	I_{39}	18	30	37	mA	1	No Signal
Free-run Frequency (1)	f_{VO1}	32	35	38	Hz	1	f_V = 40 Hz (Free-run = 35 Hz)
Free-run Frequency (2)	f_{VO2}	44	47	50	Hz	1	f_V = 55 Hz
Free-run Frequency (3)	f_{VO3}	48	51	54	Hz	1	f_V = 60 Hz
Free-run Frequency (4)	f_{VO4}	64	67	70	Hz	1	f_V = 80 Hz

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITION
Free-run Frequency (5)	f_{VO5}	80	84	88	Hz	1	f_V = 100 Hz
V.F/V Converter Non-Linearity	V.F/V	−2.5	−1.6	0	%	1	100 Hz (40 Hz, standard, Input Pin 47)
Capture Frequency (1)	f_{PV1}	−26	−28	−30	Hz	1	f_V(in) = 40 Hz
Capture Frequency (2)	f_{PV2}	−33	−36	−39	Hz	1	f_V(in) = 55 Hz
Capture Frequency (3)	f_{PV3}	−37	−40	−43	Hz	1	f_V(in) = 60 Hz
Capture Frequency (4)	f_{PV4}	−51	−55	−59	Hz	1	f_V(in) = 80 Hz
Capture Frequency (5)	f_{PV5}	−64	−68	−72	Hz	1	f_V(in) = 100 Hz
Free-run Frequency Power Supply Fluctuation (1)	$\Delta f_{VO(VCC)1}$	–	0.1	0.4	Hz	1	$\Delta f_{VO(VCC)}$ = | f_{VO}(11 V)−f_{VO}(13 V)| f_V = 40 Hz
Free-run Frequency Power Supply Fluctuation (2)	$\Delta f_{VO(VCC)2}$	–	0.2	0.5	Hz	1	Same as $f_{VO(VCC)1}$, but f_V = 55 Hz
Free-run Frequency Power Supply Fluctuation (3)	$\Delta f_{VO(VCC)3}$	–	0.2	0.6	Hz	1	Same as $f_{VO(VCC)1}$, but f_V = 65 Hz
Free-run Frequency Power Supply Fluctuation (4)	$\Delta f_{VO(VCC)4}$	–	0.3	0.8	Hz	1	Same as $f_{VO(VCC)1}$, but f_V = 80 Hz
Free-run Frequency Power Supply Fluctuation (5)	$\Delta f_{VO(VCC)5}$	–	0.4	1.0	Hz	1	Same as $f_{VO(VCC)1}$, but f_V = 100 Hz
Free-run Frequency Temperature Fluctuation (1)	$\Delta f_{VO(Ta)1}$	–	0.4	0.8	Hz	1	$\Delta f_{VO(T2)}$ = | f_{VO}(−10 °C) −f_{VO}(+60 °C) |, f_V = 40 Hz
Free-run Frequency Temperature Fluctuation (2)	$\Delta f_{VO(Ta)2}$	–	0.8	1.5	Hz	1	Same as $f_{VO(Ta)1}$, but f_V = 55 Hz
Free-run Frequency Temperature Fluctuation (3)	$\Delta f_{VO(Ta)3}$	–	1.0	2.0	Hz	1	Same as $f_{VO(Ta)1}$, but f_V = 65 Hz
Free-run Frequency Temperature Fluctuation (4)	$\Delta f_{VO(Ta)4}$	–	1.2	2.5	Hz	1	Same as $f_{VO(Ta)1}$, but f_V = 80 Hz
Free-run Frequency Temperature Fluctuation (5)	$\Delta f_{VO(Ta)5}$	–	1.4	3.0	Hz	1	Same as $f_{VO(Ta)1}$, but f_V = 100 Hz
Vertical Oscillation	V_{35}	–	3.7	5.0	V	1	At the time of Saw-tooth form at Pin 35
Blanking Pulse Width	RPW	0.95	1.0	1.05	ms	1	–
Blanking Pulse Voltage	RPV	10	11	12	V	1	–
Limiter Voltage (high.)	VLH	8.3	8.6	8.9	V	1	–
Limiter Voltage (low.)	VLL	2.4	2.5	2.6	V	1	–

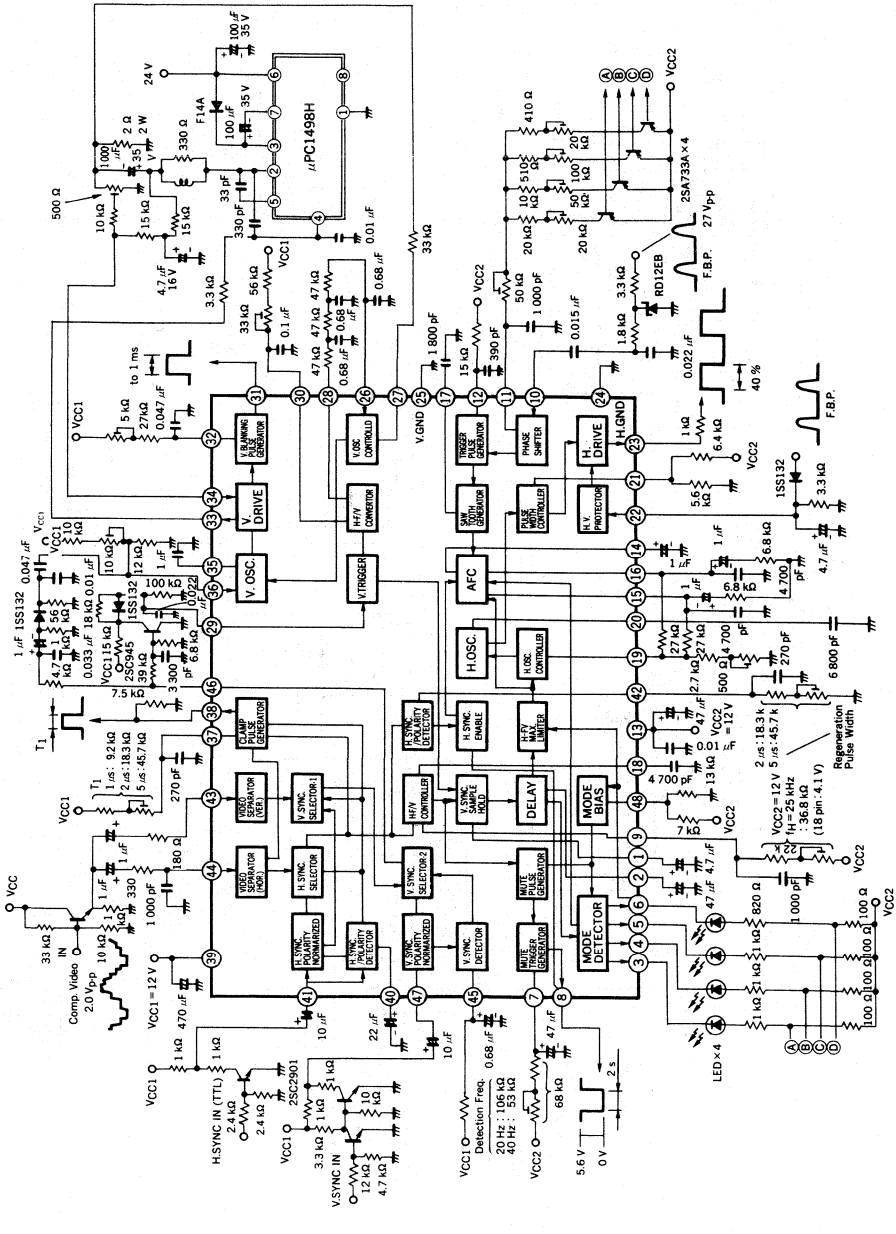
TEST CIRCUIT 1 (f_H = 15 kHz to 50 kHz)



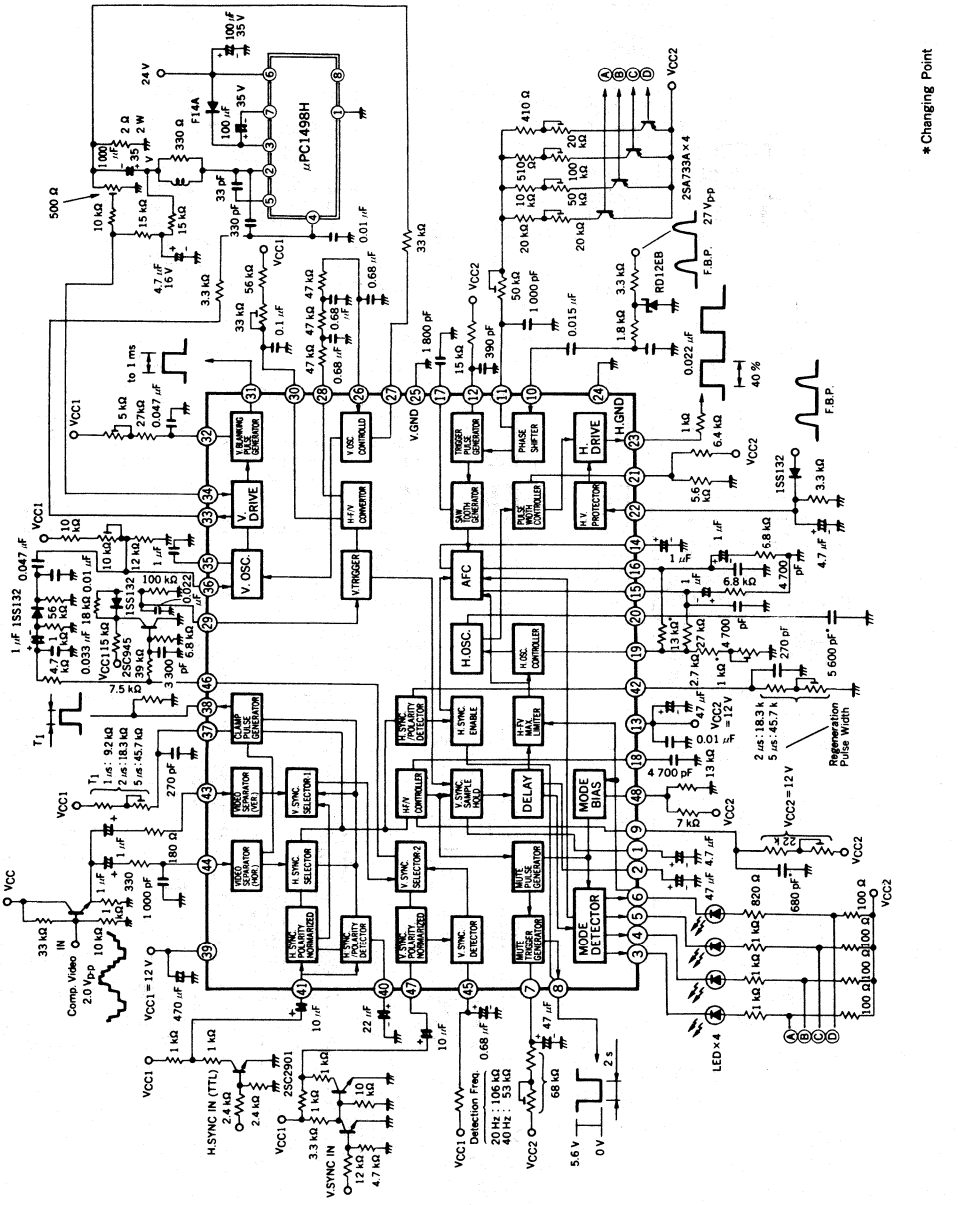
TEST CIRCUIT 2 (f_H = 30 kHz to 90 kHz)



APPLICATION CIRCUIT 1 (f_H = 15 kHz to 50 kHz)

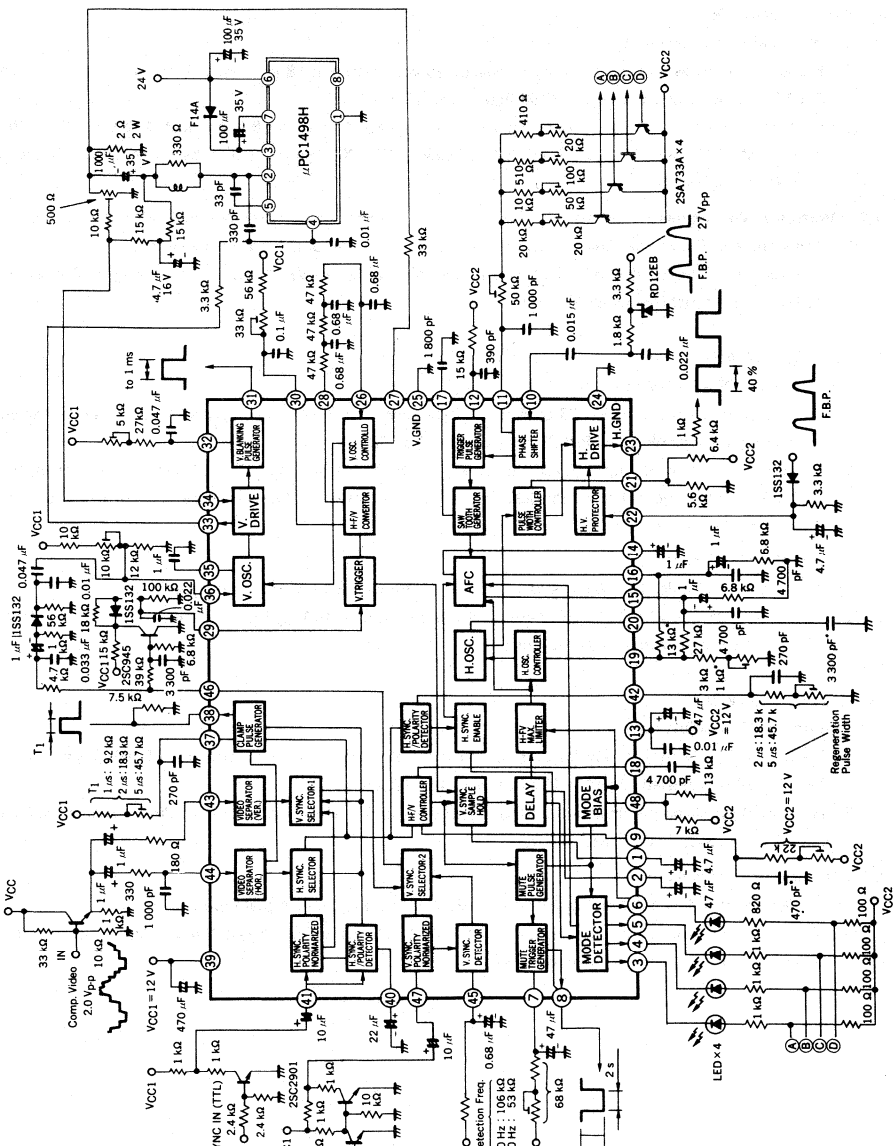


APPLICATION CIRCUIT 2 (f_H = 20 kHz to 60 kHz)



*Changing Point

APPLICATION CIRCUIT 3 (f_H = 30 kHz to 90 kHz)



* Changing Point

5

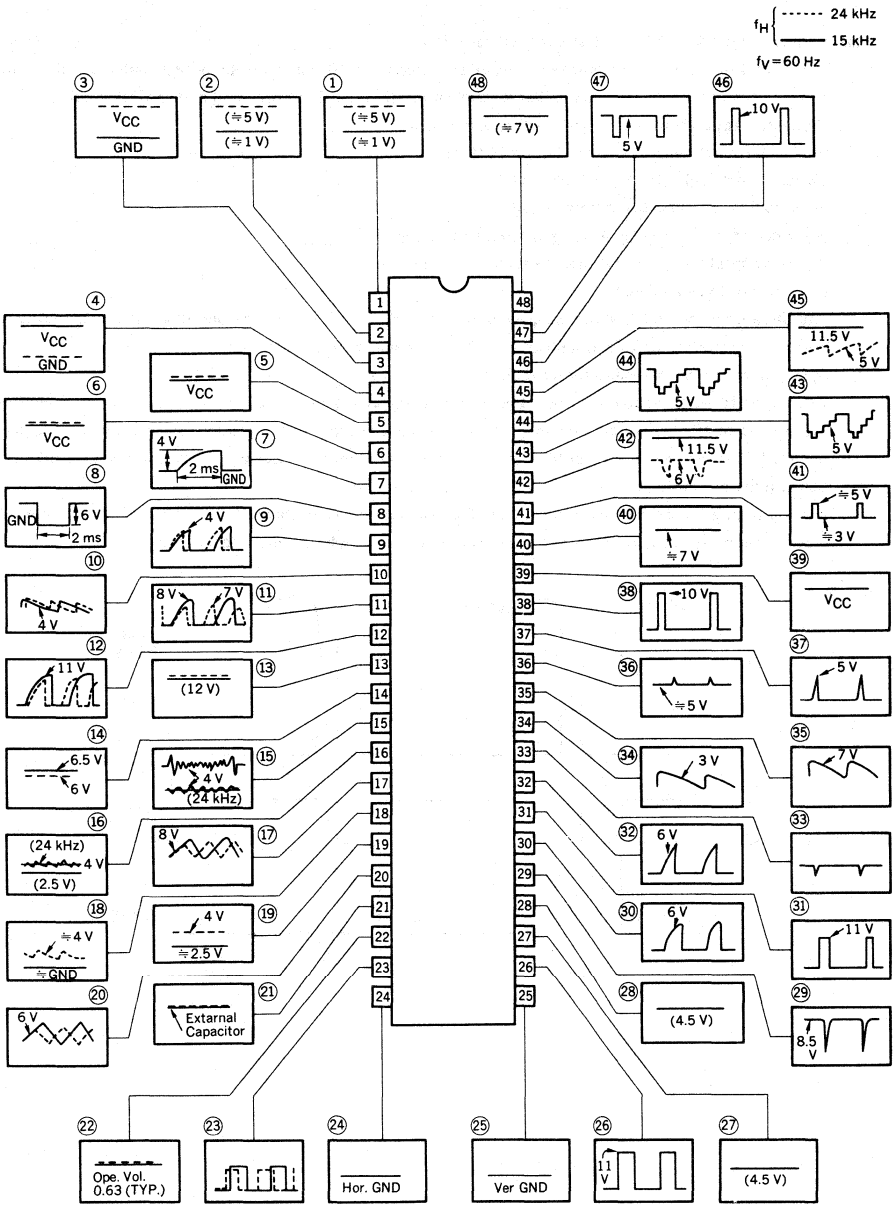
ADJUSTMENT NOTES

1. f_H = 15 kHz to 50 kHz
   1.1 Horizontal F/V adjustment
      (1) Frequency is measured at Pin 23 by frequency counter after Pin 18 is connected to GND. Then, the volume of Pin 19 shall be adjusted to set Pin 23's frequency to 15.734 kHz.
      (2) Horizontal synchronous signal (23.625 kHz) is input to Pin 41 and Pin 8 is connected to V_{CC}. Then, the volume of Pin 9 shall be adjusted to set Pin 23's frequency to 23.625 kHz. Pin 8 shall be released from connection with V_{CC} after adjustment.
   1.2 Vertical F/V adjustment
      (1) The volume of Pin 36 shall be adjusted to set Pin 35's frequency to 35 Hz at no signal input.
      (2) The volume of Pin 30 shall be adjusted to set Pin 28's voltage to $V_{CC}/5$ (e.g. 2.4 V at V_{CC} = 12 V) after input of 40 Hz vertical synchronous signal to Pin 47.

2. f_H = 20 kHz to 60 kHz
   2.1 Horizontal F/V adjustment
      (1) Frequency is measured at Pin 23 by frequency counter after Pin 18 is connected to GND. Then, the volume of Pin 19 shall be adjusted to set Pin 23's frequency to 18.000 kHz.
      (2) Horizontal synchronous signal (40.000 kHz) is input to Pin 41 and Pin 8 is connected to V_{CC}. Then, the volume of Pin 9 shall be adjusted to set Pin 23's frequency to 40.000 kHz. Pin 8 shall be released from connection with V_{CC} after adjustment.
   2.2 Vertical F/V adjustment
      (1) The volume of Pin 36 shall be adjusted to set Pin 35's frequency to 35 Hz at no signal input.
      (2) The volume of Pin 30 shall be adjusted to set Pin 28's voltage to $V_{CC}/5$ (e.g. 2.4 V at V_{CC} = 12 V) after input of 40 Hz vertical synchronous signal to Pin 47.

3. f_H = 30 kHz to 90 kHz
   3.1 Horizontal F/V adjustment
      (1) Frequency is measured at Pin 23 by frequency counter after Pin 18 is connected to GND. Then, the volume of Pin 19 shall be adjusted to set Pin 23's frequency to 28.0 kHz.
      (2) Horizontal synchronous signal (60.0 kHz) is input to Pin 41. Then, the volume of Pin 23 shall be adjusted to set Pin 23's frequency to 60.0 kHz.
   3.2 Vertical F/V adjustment
      (1) Pin 36 shall be adjusted to set Pin 35's Peak-to-Peak to 2.5 $V_{p\text{-}p}$ at no signal input.
      (2) The volume of Pin 30 shall be adjusted to set Pin 28's voltage to $V_{CC}/5$ (e.g. 2.4 V at V_{CC} = 12 V) after input of 40 Hz vertical synchronous signal to Pin 47.

WAVEFORM OF EACH PIN



μPC1880CA FEATURES OF EACH BLOCK

1. Horizontal and vertical synchronization signal processing part

(1) This part discriminates horizontal and vertical synchronization signals for positive or negative, stabilizes the polarity of a synchronization signal, and supplies the synchronization signal to horizontal and vertical circuits.

[Synchronization components that can be discriminated]

Horizontal synchronization signal Duty = 25 % max.

Vertical synchronization signal Duty = 15 % max.

(2) Synchronization signal precedence circuit

(a) Horizontal and vertical separate synchronization signal

(b) Horizontal and vertical composite synchronization signal

(c) Composite video signal

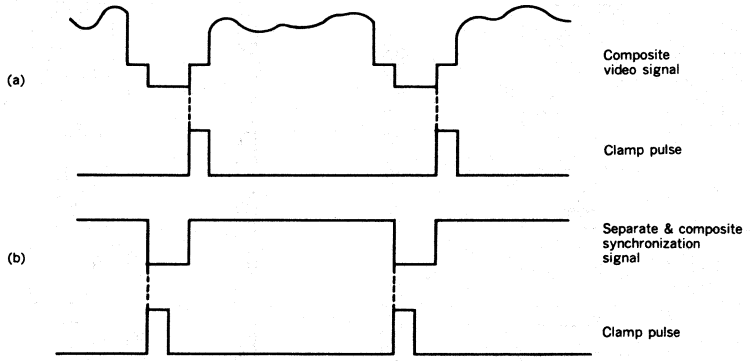
The three kinds of signals above are given priority in order of (a), (b) and (c), and this part automatically selects the best synchronization signal and supplies it to the horizontal and vertical circuits.

(3) Synchronization signal regeneration circuit

When a personal computer is in use, this circuit regenerates a synchronization signal of a fixed width of pulses irrespective of the horizontal frequency, and a horizontal sweep range in proportion to the input frequency can be obtained. However, when a TV or VTR set is in use, pin 42 is connected to V_{CC} so that it will not work.

(4) Clamp pulse generation circuit

For use with a TV or personal computer, timings are automatically changed at the time of a composite video signal input, separate synchronization signal input, and composite synchronization signal input.



2. Horizontal deflection circuits

(1) Sampling hold circuit

A voltage error is generated between a composite synchronization input signal and a separate synchronization input in the horizontal frequency — voltage conversion circuit. This is the influence of the pulse of a vertical synchronization signal, and it also depends on the presence or absence of a spiked pulse contained in a vertical synchronization signal. The longer the vertical synchronization signal is, the great this influence will become. This voltage error is reduced by a factor of about 10 by holding the voltage during the vertical synchronization period in this IC.

(2) Delay circuit

When a horizontal input frequency is switched, it is converted to a voltage through a horizontal F/V circuit, and is supplied to the mode output circuit, switching constants of each part of the horizontal deflection output circuit. For this switching, the constants of each part must be switched with a given delay time to protect a deflection output stage.

This circuit is used to delay the voltage supplied to the mode output circuit. The ratio of the delay time at the horizontal frequency increase time and that at the decrease time is made 1:2 in view of the deflection circuit operation. The setting of the delay time is determined by an external constant.

(3) Mode output circuit

This circuit is a control voltage output circuit used to switch the deflection circuit constants in each mode by dividing an applicable horizontal frequency into four. A stable no-chattering switching operation with hysteresis added can be performed for output. The threshold level for switching the mode can be set using external constants.

(4) Limiter circuit

Since the oscillation frequency must be controlled to protect the horizontal output stage, the limiter is set in this IC by clamping the upper and lower limits on which a frequency-voltage conversion is performed through the horizontal F/V circuit. When the corresponding frequency is low, mode 4 is not used, and the upper limiter is made to switch by grounding.

(5) Horizontal output circuit

The width of an output pulse can be set externally so that the horizontal output transistor can be driven under the best conditions according to the horizontal frequency.

(6) Screen horizontal position adjustment circuit

To be able to change the horizontal position of a screen, the phases of a horizontal synchronization signal and a horizontal output pulse must be changed. In this circuit, the method employed is to change the phase of a flyback pulse that is equal to a horizontal output pulse, since composite video signals such as a TV signal with an inferior S/N are handled.

(7) AFC circuit

Automatic switching of two time constants can be performed for an input horizontal frequency, and external switching circuits can be reduced.

(8) Horizontal oscillation circuit

Good tracking characteristics have been obtained because of the use of a current-controlled oscillation circuit.

(9) Mute pulse generation circuit

This circuit is used so that the distortion of a screen will not be seen at the mode switching time. This is made possible by generating a mute pulse at a timing voltage earlier than a voltage that controls an oscillation circuit at the mode switching time.

3. Vertical circuits

(1) Oscillation circuit

This is a CR oscillation circuit by means of a three differential comparator. This circuit automatically tracks an input vertical synchronization frequency under current control by vertical F/V/I-converted currents.

(2) Vertical output circuit

The saw-tooth wave obtained by an oscillator and the saw-tooth wave from the deflection output are output using a differential amplifier. Thus, in this circuit, the raster size will not change in the case of no signal, or if the input vertical frequency changes.

(3) Vertical flyback line erase circuit

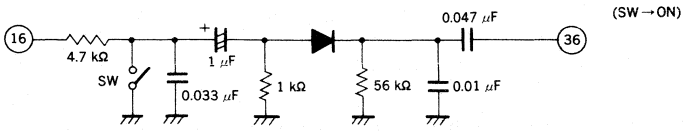
For a vertical flyback pulse, pulse width in synchronization with the rise of the vertical oscillation can be obtained. The pulse width can be set externally.

NOTES ON APPLICATIONS OF μPC1880CA

1. Free-run frequency measurement method during capturing signal

   (1) Vertical

   When free-run frequency is measured, input terminal of vertical integrating circuit shall be connected to ground.



   (2) Horizontal

   Frequency can be measured when pin 8 (mute output) is connected to V_{CC}.

2. Precision of external parts

   (1) Vertical

   (a) Vertical oscillation capacitor of pin 35 shall be used ±5 % precision metalized polypropylene film capacitor etc, which is good enough to fit tan δ and temperature characteristics.

   (b) F/V capacitor of pin 30 shall be used ±2 % precision polypropylene film capacitor which is good enough to fit temperature characteristics and the resistor shall be used ±1 % precision resistor.

   (2) Horizontal

   (a) F/V capacitor of pin 9 shall be used ±2 % precision polypropylene film capacitor which is good enough to fit temperature characteristics and the resistor shall be used ±1 % precision resistor.

   (b) Free-run frequency resistor of pin 19 shall be used ±1 % precision resistor.

   (c) Oscillation capacitor of pin 20 shall be used ±2 % precision polypropylene film capacitor which is good enough to fit temperature characteristics.

   (d) Resistor of pin 21 shall be used ±1 % precision resistor as to fix horizontal duty of pin 23.

   (e) Resistor of pin 48 shall be used ±1 % precision resistor as to fix switching frequency.

DUAL ATTENUATOR

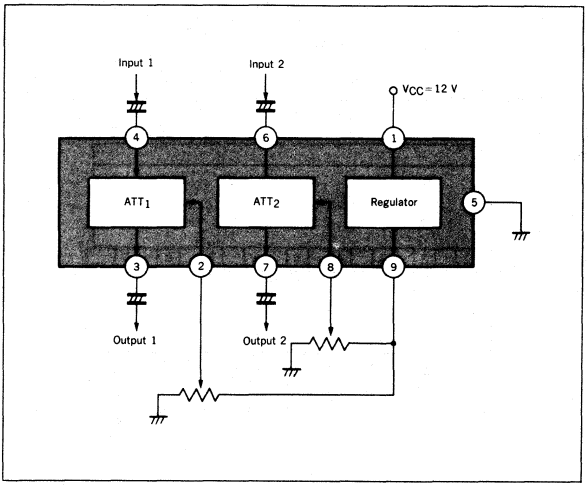
DESCRIPTION

The μPC1406HA is a silicon monolithic integrated circuit for sound control (e.g. Volume, Balance). This IC has a good characteristic control curve ('A' Curve), and is very suitable for remote control applications. The two attenuators are completely separate, and it is easy to control the balance between the two attenuators. This IC is manufactured in a 9 Pin slim SIP.

FEATURES

- Each attenuator is completely separate, and is very easy to control with remote control. (e.g. Volume, Balance)
- This IC's characteristic control curve is linear against logarithmic output, and offers smooth control.
- Channel Separation : 64 dB MIN.
- Typical Application : Sound MPX attenuator for TV, Radio and mobile receiver.

BLOCK DIAGRAM



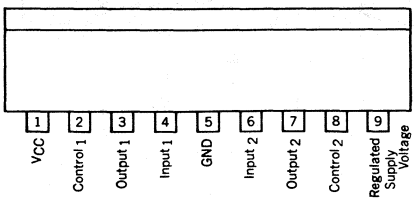
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC}	0 (MIN.), 15 (MAX.)	V
Signal Input Voltage at pins 4 and 6	V_{in}	3	V_{p-p}
Control Input Voltage at pins 2 and 8	V_{cont}	0 (MIN.), 15 (MAX.)	V
Power Dissipation	P_D	350 (T_a = 75 °C)	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_a = 25 °C, f = 1 kHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	8.0	12.0	14.4	V	
Supply Current	I_{CC}	6.0	8.5	13.5	mA	NO SIGNAL
Relative Output	A_v	−2	0	+2	dB	V_{cont} = 1 V, V_{in} = 500 $mV_{r.m.s.}$
Channel Separation	Sep	64.0	70.0	–	dB	V_{cont} = 5 V, V_{in} = 500 $mV_{r.m.s.}$
Total Harmonic Distortion	THD	–	0.5	1.0	%	V_{cont} = 5 V, V_{in} = 500 $mV_{r.m.s.}$
Power Sourse Noise Rejection	R.R.	30	–	–	dB	H_{um} f = 60 Hz, H_{um} Level = 1 V_{p-p}
Output Voltage 1	ATT_1	−1.5	0	+1	dB	V_{cont} = 5 V, V_{in} = 500 $mV_{r.m.s.}$
Output Voltage 2	ATT_2	−34	−30	−26	dB	V_{cont} = 5 V, V_{in} = 500 $mV_{r.m.s.}$
Output Voltage 3	ATT_3	–	−77	−71	dB	V_{cont} = 5 V, V_{in} = 500 $mV_{r.m.s.}$
Input Resistance	R_i	12	–	24	kΩ	f = 1 kHz
Output Resistance	R_o	200	–	450	Ω	f = 1 kHz

CONNECTION DIAGRAM



TEST CIRCUIT

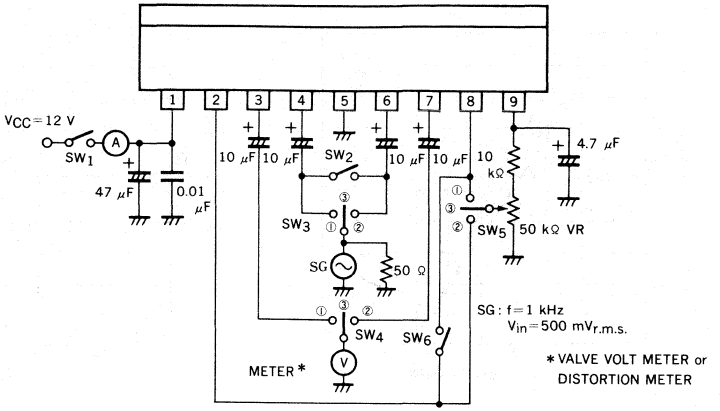


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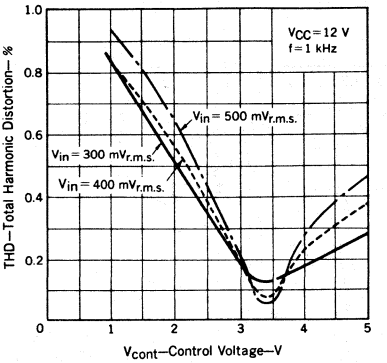
TABLE OF SWITCH CONDITIONS IN THE TEST CIRCUIT

CHARACTERISTIC		SWITCH CONDITION						
		SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	VR
Supply Voltage		ON	ON	*	*	*	ON	5 V
Supply Current		ON	OFF	3	3	*	ON	0 V
Relative Output		ON	ON	*	1 (ch1) 2 (ch2)	*	ON	1 V
Channel Separation	ch1 → ch2	ON	OFF	1	1	2	OFF	5 V
	ch2 → ch1	ON	OFF	2	2	1	OFF	5 V
Distortion Ratio		ON	ON	*	1 (ch1) 2 (ch2)	*	OFF	5 V
Power Source Noise Rejection		ON	*	3	1 (ch1) 2 (ch2)	*	ON	5 V
Output Voltage		ON	ON	*	1 (ch1) 2 (ch2)	*	ON	5 V
Output Voltage 2		ON	ON	*	1 (ch1) 2 (ch2)	*	ON	1 V
Output Voltage 3		ON	ON	*	1 (ch1) 2 (ch2)	*	ON	0 V
Input Resistance		ON	*	*	*	*	*	5 V
Output Resistance		ON	*	*	*	*	*	5 V

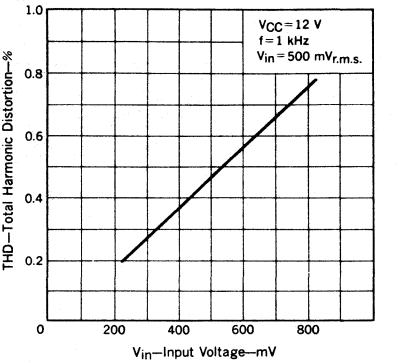
* ON, OFF, 1, 2 as convenient

TYPICAL CHARACTERISTICS (T_a = 25 °C)

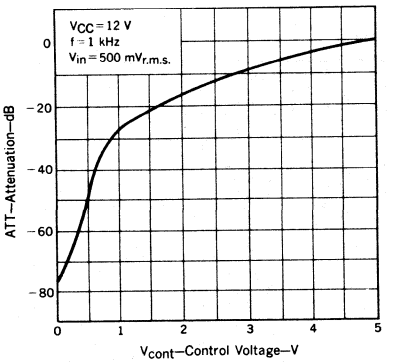
THD–V_{cont}



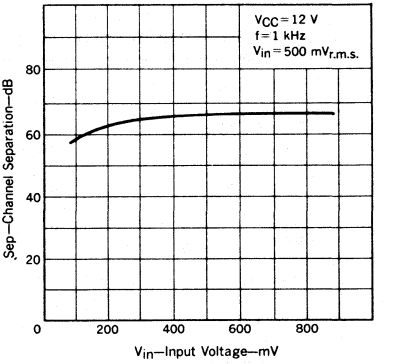
THD–V_i



ATT–V_{cont}

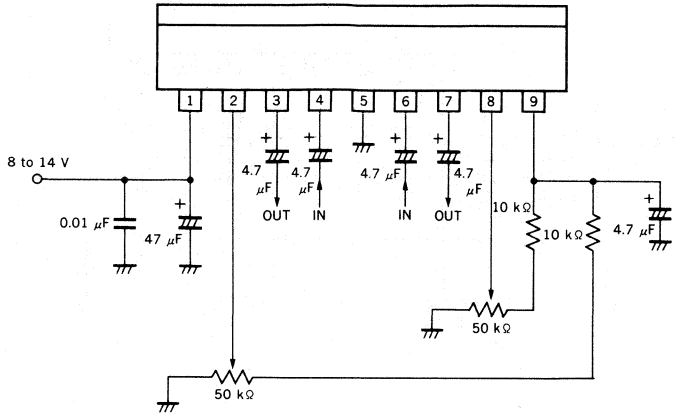


Sep–V_i

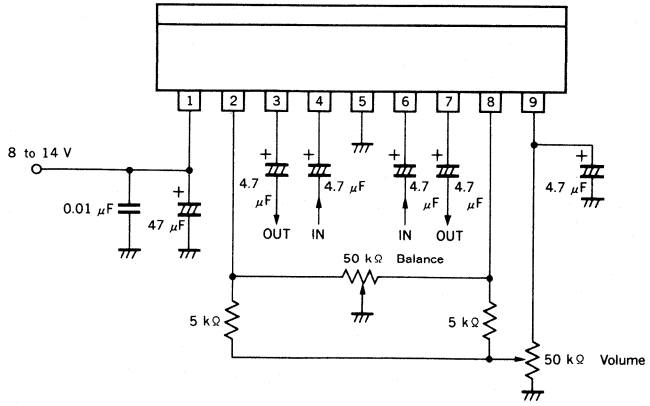


EXTERNAL COMPONENTS FOR μPC1406HA

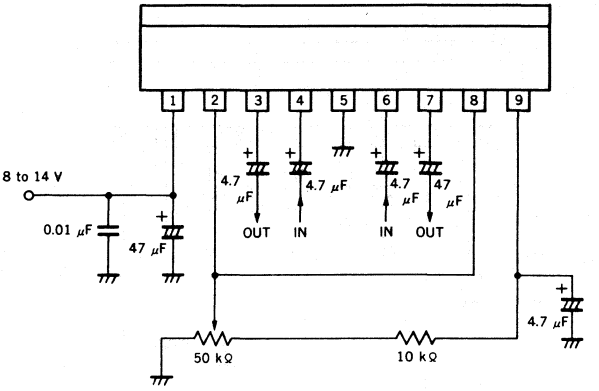
(1) To Control Each Attenuator Separately



(2) To Balance The Two Attenuators



(3) To Control Both Attenuators Simultaneously



EEPROM-Memory

Section 6 - EEPROM-Memory

EEPROMs

Device	Density (bit)	Organization	Features	Supply voltage (V)	Pins/Package
µPD6252C/G	2K	256 x 8	2/3-wire serial bus interface	5	C: 8/DIP G: 16/FLAT
µPD6253CX/GS-BA1	1K	128 x 8		5	CX: 8/DIP GS: 8/FLAT
µPD6254CX/GS-BA1	4K	512 x 8		5	CX: 8/DIP GS: 8/FLAT

2 048 bit EEPROM

DESCRIPTION

μPD6252 is a 2 048-bit (256 words x 8 bits) Electrically Erasable Programmable Read Only Memory (EEPROM) device.

The 2/3-wire serial bus interface is used to read/write data from/to this device. μPD6252 can be used for a wide range of applications such as the preset memory for TV, VTR, and OA equipment and the ID code memory for home automation equipment.

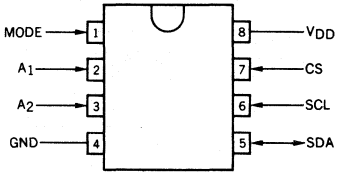
FEATURES

- Built-in 2 048-bit (256 x 8) EEPROM
- Two/three-wire serial interface
- Number of write operations: 100 000
- Memory retention period: 10 years
- Operation voltage: 5 V ±10 %, single power supply

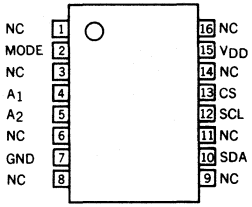
ORDER INFORMATION

Part Number	Package
μPD6252C	8 PIN PLASTIC DIP (300 mil)
μPD6252G	16 PIN PLASTIC SOP (300 mil)

PIN CONFIGURATION (Top View)



μPD6252C

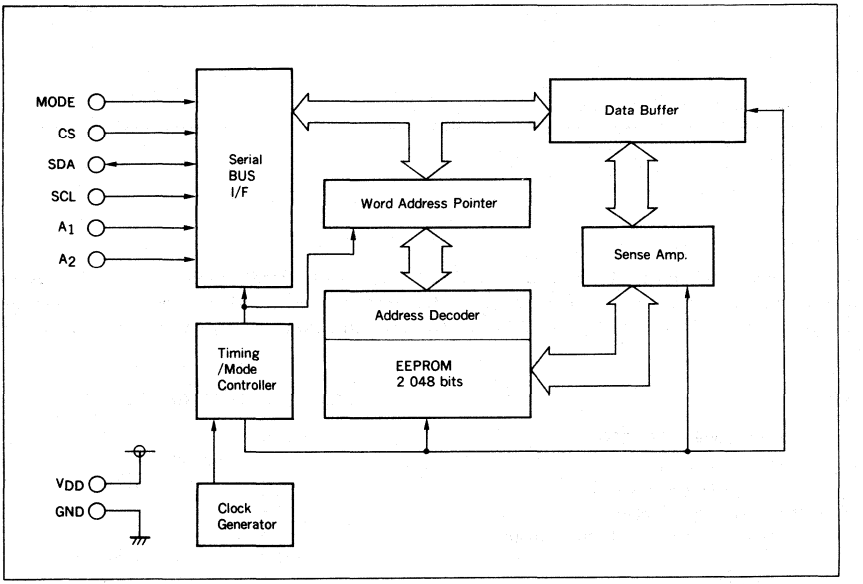


μPD6252G

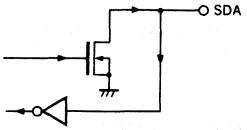
(8 Pin 50P-Version under development)

BLOCK DIAGRAM

Fig. 1



PIN FUNCTIONS

PIN NO. DIP/SOP	PIN NAME	INPUT/ OUTPUT	FUNCTION
1/2	MODE	Input	This is the terminal for selecting the system to interface with external devices. "H" ..... Three-wire serial bus interface. This can be controlled by setting the CS terminal to "H" or "L." "L" ..... Two-wire serial bus interface. The CS terminal can be used with the device set to "H."
2/4 3/5	A_1 A_2	Input	These pins are used only when the 2-wire serial bus interface is selected by setting the ODE terminal to "L." Setting A_1 and A_2 enables a slave address to be determined "H" level ..... Set to "1." "L" level ..... Set to "0." Slave address. 1 0 1 0 A_2 A_1 0 MSB → Variable by external setting. Slave address. Variable by external setting. If the MODE terminal is set to "H" and the 3-wire serial bus interface is selected, these terminals have no meaning. Use these terminals by setting them to "H" or "L" level.
4/7	GND	Input	(–) power terminal
5/10	SDA	Input/ Output	This is a data input/output terminal. Since this is an Nch open drain input/output, be sure to add an external pull-up resistor. 
6/12	SCL	Input	This is the clock input terminal for data transfer. For detailed operation, see the explanation provided later.
7/13	CS	Input	This is a chip-select terminal. When this signal is "H," this IC becomes operational. Setting this signal to "L" disables data reading/writing from/to each memory cell. If the MODE terminal is set to "H," changing this terminal from "L" to "H" when the SDL terminal is "H" signals the start of the serial bus interface operation; changing this terminal from "H" to "L" signals the end of the serial bus interface operation. The MODE terminal can be set to "L" when this terminal is always set to "H."
8/15	V_{DD}	Input	(+) power supply terminal 5 V ±10 %

6

1. FUNCTION OUTLINE

1.1 Mode Selection (three/two-wire Serial Bus Interface Mode)

Setting the MODE terminal (Pin 1/2) to "H" ("L") selects the three-wire serial bus interface mode (two-wire serial bus mode).

MODE terminal (Pin 1/2)
"H" ..... Three-wire serial bus interface mode
"L" ..... Two-wire serial bus interface mode

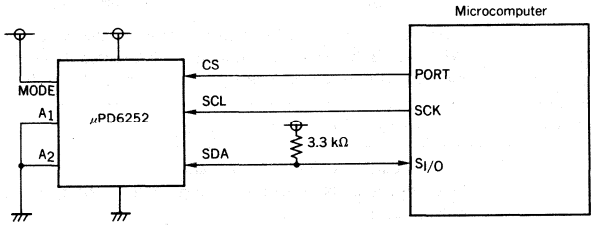
NOTE: Do not change the setting (H or L) of the MODE terminal during data transfer. To change the setting of the MODE terminal, be sure to set the CS terminal (Pin 7/13) to "H."

Setting both the MODE and CS terminals to "L" enables the device to enter the standby state and reduce power consumption.

1.2 Three-wire Serial Bus Interface Mode (MODE = H)

In the three-wire serial bus interface mode, three terminals CS (Pin 7/13), SCL (Pin 6/12), and SDA (Pin 5/10) can be used to read and write data.

(Connection) Fig. 2

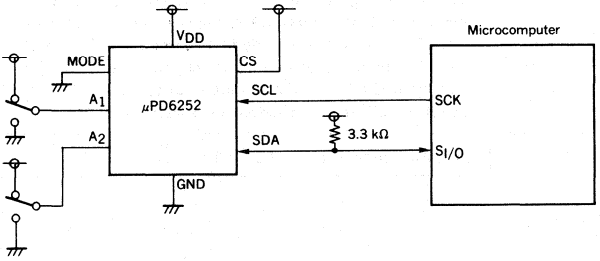


* Be sure to set terminals A_1 and A_2 to "H" or "L".

1.3 Two-wire Serial Bus Interface Mode (MODEL = L)

In the two-wire serial bus interface mode, two terminals, SCL (Pin 6/12) and SDA (Pin 5/10), can be used to read and write data.

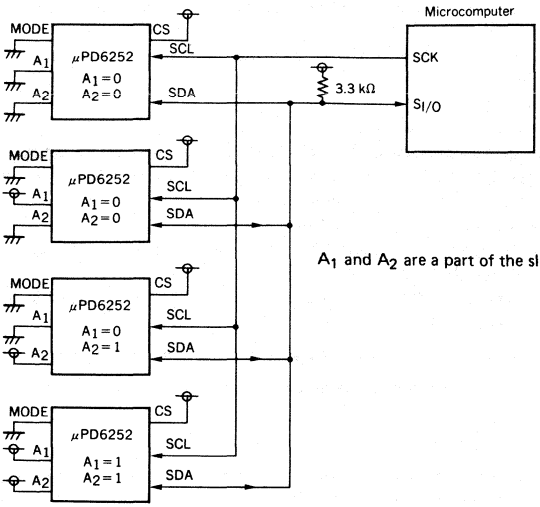
(Connection) Fig. 3



* Be sure to set A_1 and A_2 to "H" or "L" (set slave address).

Using multiple μPD6252 devices (up to four devices can be cascaded)

Fig. 4



A_1 and A_2 are a part of the slave address.

In the two-wire serial bus interface mode, data transfer is enabled only when the input slave address matches the slave address of this device.

Slave address configuration (7 bits)

1	0	1	0	A_2	A_1	0

A_2 and A_1 can be set by external terminals.

1.4 Write Protect Function

When supply voltage V_{DD} is 2.0 V or lower, write operation is inhibited.

2. THREE-WIRE SERIAL BUS INTERFACE OPERATION (MODE = H)

2.1 Basic Operation Sequence

(1) Start condition (STA).
To start the interface, set the SCL terminal to "H" then change the CS terminal from "L" to "H". Data transfer starts at the rising edge of the CS terminal.

(2) After the rising edge is input to the CS terminal, the microcomputer sends an 8-bit command.
SDA ..... Data input
SCL ..... Serial clock input
Serial data is read at the rising edge of the serial clock.

(3) After reception of the 8-bit command data, the SDA terminal of μPD6252 enters the output mode.
If this 8-bit command is accepted, the SDA terminal outputs the "L" level; if not, it outputs the "H" level.*
This status lasts until eight clock pulses have been input to the SCL terminal.
The data output from the SDA terminal changes at the falling edge of the serial clock.
This mode is used to check the internal status of μPD6252. If the signal output from the SDA terminal is "H" in this mode, the device is in the Write Busy [WB] state, so stop the data transfer.
To suspend the data transfer, change the CS terminal from "H" to "L." To restart the data transfer, change the CS terminal from "L" to "H" and input the 8-bit command.

* **NOTE:** The SDA terminal configuration is Nch opendrain so that the "H" level output is the high impedance state.

(4) If μPD6252 is not in the WB state, the internal status can be determined according to the 8-bit command shown below.

MSB
1. RANDOM WRITE command [$0\,0\,0\,0\,0\,0\,0\,0_B$]
After inputting the word address (WA, 8 bits) from the SDA terminal, input the write data (8 bits). Write data of up to three bytes can be continuously received. Data bytes 1 to 3 are sequentially written to the memory from the specified word address according to the number of data bytes in the internal write cycle after the falling edge of the CS terminal. In the internal write cycle, the device enters the WB state to disable the input of any command, so suspend data transfer until after the internal write cycle as previously described.

MSB
2. CURRENT READ command [$1\,0\,0\,0\,0\,0\,0\,0_B$]
Reads data from the word address at execution of the 8-bit command. After eight data bits are read from the SDA terminal, the word address is incremented by 1 to enable sequential reading of data. To end data reading, set the CS terminal from "H" to "L."

MSB
3. RANDOM READ command [$1\,1\,0\,0\,0\,0\,0\,0_B$]
When a word address (WA, 8 bits) is input from the SDA terminal, the memory contents specified by this word address are transferred to the read data buffer. After eight data bits are read from the SDA terminal, the word address (WA) is incremented by 1 to enable sequential reading of data.
To end data reading, set the CS terminal from "H" to "L."

(5) Stop condition (STP)
To end data transfer, be sure to set the CS terminal low. This causes this LSI to recognize the end of data transfer and enables it to receive a new command. To set the CS terminal low, be sure to keep the SCL terminal to "H."

2.2 Three-wire Serial Bus Interface Command List

The command to be used in the three-wire serial bus interface are shown in Table 1. Each command consists of eight bits.

Table 1 Three-wire Serial Bus Interface Command List

COMMAND NAME	COMMAND	OPERATION
RANDOM WRITE	00000000_B [00_H] MSB C_7 to C_0	Transfers write data after a word address (WA, 8 bits) is set. Up to three write data bytes can be set sequentially. Correspondence between word addresses and data bytes: WA . . . . . Data byte 1 WA+1 . . . . . Data byte 2 WA+2 . . . . . Data byte 3 Writing is performed in the internal write cycle after the CS terminal is set low.
CURRENT READ	10000000_B [80_H] MSB C_7 to C_0	Transfers the memory contents specified by the word address (current address) at the input of this command to the read data buffer. After eight data bits are read, the word address is incremented and the corresponding memory contents are transferred to the read data buffer.
RANDOM READ	11000000_B [$C0_H$] MSB C_7 to C_0	After a word address is set, starts reading data with the set word address. This command differs from the CURRENT READ command in that the word address is set after execution of the command. After the word address is set, this command performs the same operation as the CURRENT READ command.

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2.3 Updating Word Address

The word address is updated if an 8-bit word address is input in the RANDOM READ/WRITE mode. After every data byte is read in the READ mode, the word address is incremented by 1 and is thus sequentially updated.

In the write mode, after the stop bit is recognized, the word address is updated in the internal write cycle to write the internally transferred data to memory.

In the WRITE mode, if the start bit is recognized again after the stop bit is recognized (before data is written to memory), the word address retains the value at the recognition of the start bit and data is not written to memory.

If the word address is incremented when it is "FF_H," it is reset to "$0\ 0_H$" to continue the read or write operation.

2.4 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the CS terminal to "H" when the SCL terminal is "H."

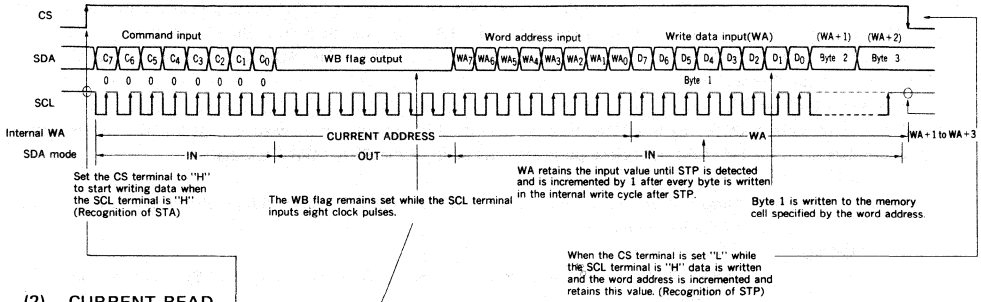
(2) Recognition of the stop bit (STP)
To end data transfer, set the CS terminal to "L" when the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, the transferred data is not written to memory.

If the data transfer start operations are executed sequentially, a command can be input after the last data transfer starts. If the data transfer end operations are executed sequentially, the internal status is determined during the first data transfer end operation.

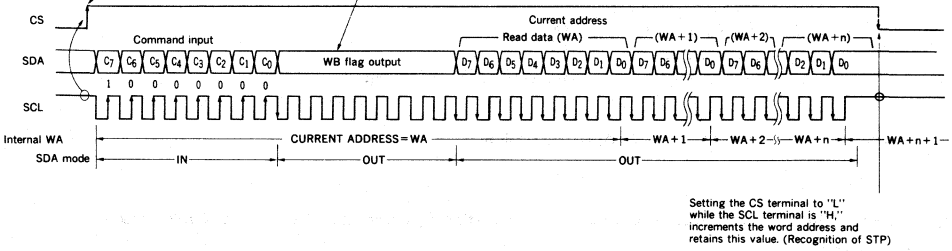
If the CS terminal is changed between "H" and "L" when the SCL terminal is "L," the internal status remains unchanged.

2.5 Three-wire Serial Bus Interface Timing

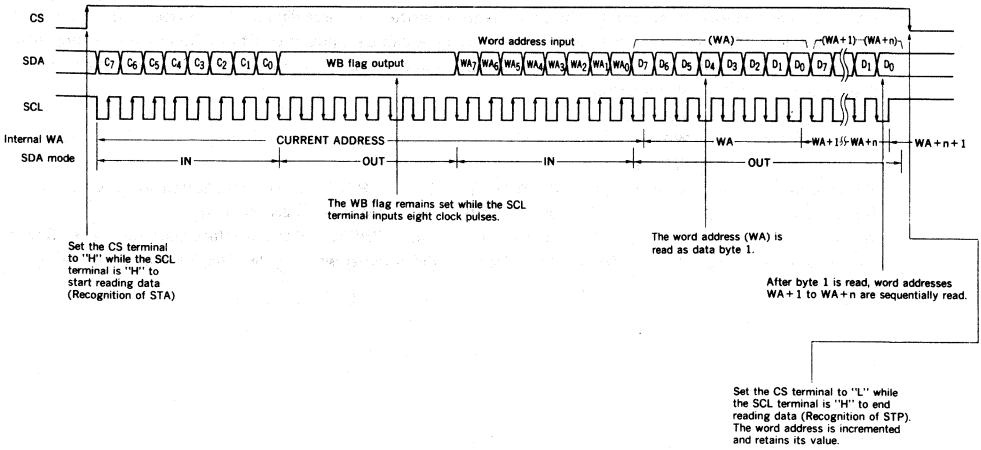
(1) RANDOM WRITE



(2) CURRENT READ



(3) RANDOM READ



3. TWO-WIRE SERIAL BUS INTERFACE OPERATION EXPLANATION (MODEL = L)

3.1 Basic Operation Sequence

Two-wire serial bus interface can be used when the CS terminal is set to "H," not when it is set to "L."

(1) To use the interface, set the SCL terminal to "H" and the SDA terminal to "L" (Recognition of the start bit (STA)).

(2) After starting the interface operation (after recognition of STA), input the clock from the SDL terminal.
In synchronization with this clock, input seven slave address bits and one *READ/$\overline{\text{WRITE}}$ mode selection bit to this LSI from the SDA terminal.
Data is input on the rising edge of the clock.

(3) If the input slave address matches **the slave address of this LSI, one acknowledge signals (ACK) bit is output syncronized with the fall of the eight clock pulse after the input of the READ/$\overline{\text{WRITE}}$ signal.

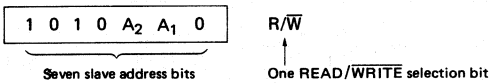
$\overline{\text{ACK}}$ signal

H ..... Output if the input slave address does not match the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

$\overline{\text{ACK}}$ signal

L ..... Output if the input slave address matches the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

*, ** Slave address and READ/$\overline{\text{WRITE}}$ signal data configurations after the start of the interface operation



A_1 and A_2 can be determined by setting the A_1 and A_2 terminals.
"H" 1
"L" 0

(4) After this LSI outputs the ACK signal properly, the operation is performed in the READ or WRITE mode.

1. WRITE mode

After the output of the SCK signal, input an 8-bit word address from the SDA terminal. If the word address is correctly set, one ACK signal bit (set to "L") is output synchronized with the fall edge of the clock pulse right after the clock pulse input to the SCL terminal.

After the word address is set, input eight data bits to be written. If these data bits are correctly input, the ACK signal (set to "L") is output. Up to three write data bytes can be input at one time. Continue inputting eight data bits and confirming the ACK signal (set to "L") three times. The correspondence between the word addresses and data bytes is shown below.

Byte 1 ..... WA
Byte 2 ..... WA + 1
Byte 3 ..... WA + 2

To write more than three bytes of data, the $\overline{\text{ACK}}$ signal (set to "H") is output as bit 9 after the input of byte 4 (the three bytes immediately before the stop bit (STP) is recognized are actually written).

When the SDA terminal goes to "H" while the SCK terminal is "H" to end the interface operation (when STP is recognized), data starts being written automatically in the internal write cycle. The internal word address is incremented by 1 after every byte is written.

2. READ mode

After the output of the ACK signal, the memory contents specified by the internal word address already set are sequentially read synchronized with the fall of the clock pulse input to the SCL terminal. After eight data bits have been input, the ACK signal (set to "L") is input. This ACK signal is fetched at the rising edge of the clock. After the ACK signal is fetched, the word address is automatically incremented to allow sequential reading of data.

If the $\overline{ACK}$ signal (set to "H") is input, the word address is not incremented and the SDA terminal enters the input state. Input the stop bit (STP) and the start bit (STA) again to start the interface operation or continues inputting the clock pulses and input the ACK signal (set to "L") as the ninth clock pulse to restart the interface operation. If the interface operation is restarted by the input of the ACK signal (set to "L"), the word address (WA) is incremented at this ACK signal input. (See the Fig. 5)

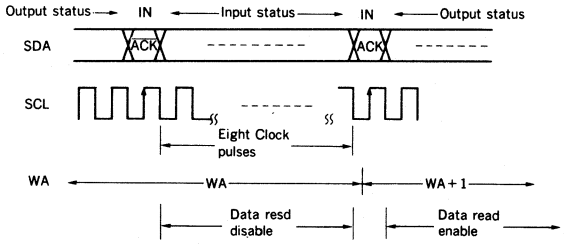
To end the READ mode, input the $\overline{ACK}$ signal (set to "H") instead of the ACK signal (set to "L") and set the SDA terminal to "L" when the SCL terminal has been already set to "H" (recognition of STP). In this case, the word address is not incremented so that the data in this address is read when the interface enters the READ mode again.

To read the data in a word address, set the word address in the WRITE mode, Input the start bit (STA) again to set the interface in the READ mode, and read the data.

Data Transfer Restart Method at Input of $\overline{ACK}$ Signal in READ Mode

1. Input STP, Input STA again, and input the slave address and the R/$\overline{W}$ signal.
2. Input the ACK signal (set to "L") at the input of the ninth clock pulse.

Fig. 5



(5) To end data transfer, set the SDA terminal to "H" after the SCL terminal is set to "H" (recognition of stop bit (STP)).

3.2 Updating Word Address

In the WRITE mode, update the word address at the end of the input of eight word address bits and at the start of the internal memory write operation by recognition of the stop bit after the input of write data.

In the READ mode, the word address is incremented at the input of the ACK signal (set to "L") after data is read.

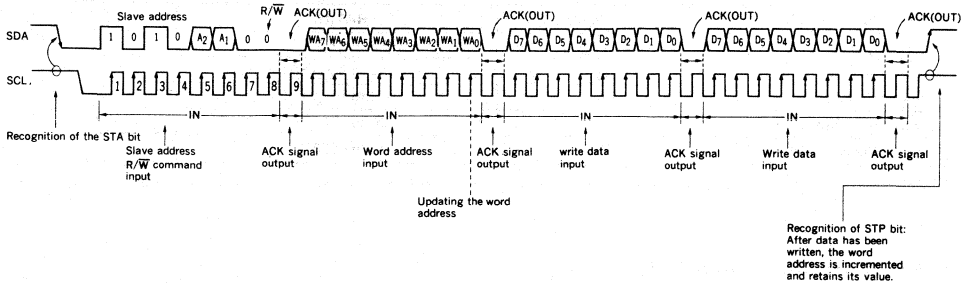
3.3 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the SDA terminal to "L" while the SCL terminal is "H."

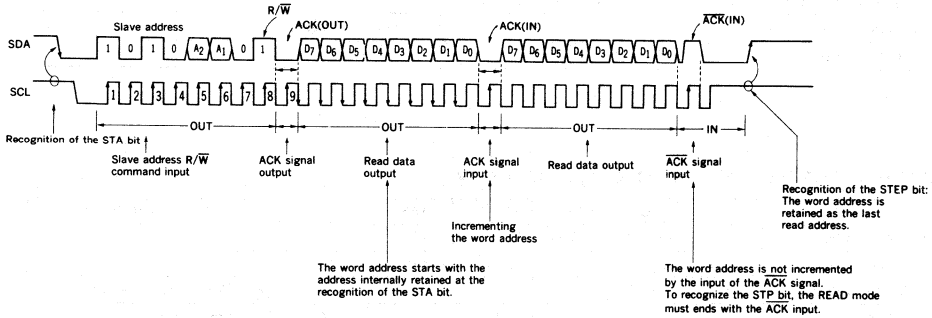
(2) Recognition of stop bit (STP)
To end data transfer, set the SDA terminal to "H" while the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, data cannot be written to memory.

3.4 Two-wire Serial Bus Interface Operation Timing

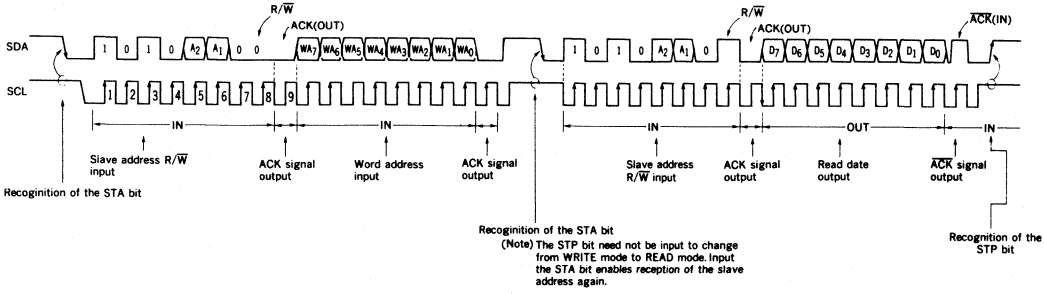
(1) WRITE mode (two bytes)



(2) READ mode (two bytes)



(3) READ mode



ELECTRICAL CHARACTERISTICS

MAXIMUM ABSOLUTE RATING (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	0.3 to V_{DD} +0.3	V
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V
Operation Temperature	T_a	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +125	°C

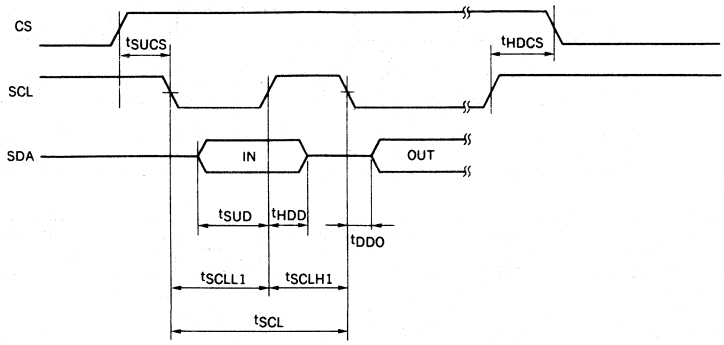
RECOMMENDED OPERATION RANGE (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Data Retaining Voltage	V_{DR}	0		5.5	V	
Number of Data Write/Erase Operation	N	10^5			Time	
Number of Data Retaining Years	Y	10			Year	
Operation Temperature	T_a	−20		+70	°C	

DC CHARACTERISTICS (T_a = −20 °C to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High-level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low-level Input Voltage	V_{IL}			0.3 V_{DD}	V	
Low-level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3 mA, Nch open drain
Input Leak Current	I_{IL}	−10	0	10	μA	V_I = 0 to V_{DD}
Circuit Current 1	I_{DD1}			4	mA	In operation
Circuit Current 2	I_{DD2}			100	μA	At standby (CS = L, MODE = L)

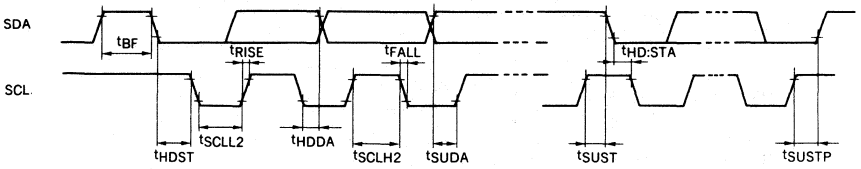
AC CHARACTERISTIC 1 (three-wire serial bus interface, T_a = −20 °C to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
CS Setup Time	t_{SUCS}	100			ns	
CS Hold Time	t_{HDCS}	100			ns	
SCL Cycle Time	t_{SCL}	1.0			μs	
SCL Low-level Time	t_{SCLL1}	400			ns	
SCL High-level Time	t_{SCLH1}	400			ns	
Input Data Setup Time	t_{SUD}	100			ns	
Input Data Hold Time	t_{HDD}	100			ns	
Output Data Delay Time	t_{DDO}			300	ns	R_L = 3.3 kΩ, C_L = 20 pF
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

6

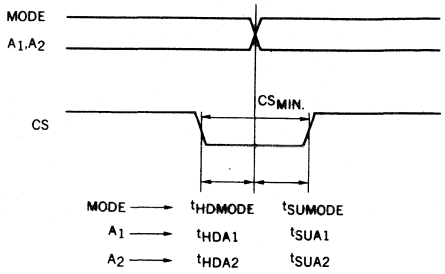
AC CHARACTERISTIC 2 (two-wire serial bus interface, T_a = −20 °C to +70 °C, V_{DD} = 4.5 V to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
SCL Input Clock Frequency	f_{SCL}	0		100	kHz	
Bus Opening Time Before the Start of Data Transfer	t_{BF}	4.7			μs	
Start Condition Hold Time	t_{HDST}	4.0			μs	
SCL Low-level Time	t_{SCLL2}	4.7			μs	
SCL High-level Time	t_{SCLH2}	4.0			μs	
Start Condition Setup Time	t_{SUST}	4.7			μs	
Data Hold Time	t_{HDDA}	0			μs	**Note:** Data is retained when SCL is set to "H."
Data Setup Time	t_{SUDA}	250			ns	
SDA/SCL Signal Rise Time	t_{RISE}			1	μs	
SDA/SCL Signal Fall Time	t_{FALL}			300	ns	
Stop Condition Setup Time	t_{SUSTP}			4.7	μs	
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

Note 1: Internal write cycle time is defined to be the period when μPD6252 is in WB (WRITE BUSY) mode.
Following operation indicates that μPD6252 is in WB mode:
(1) In case that three-wire serial bus interface is in operation, "H" level is output for WB flog output.
(2) In case that two-wire serial bus interface is in operation, $\overline{ACK}$ signal ("H" level) is output after slave address is input.
In WB mode, data writing and reading operation are not available.

AC CHARACTERISTIC 3 (CS ↔ MODE A_1, A_2 T_a = −20 °C to +70 °C, V_{DD} = 4.5 V to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
MODE A_1 A_2 Setup Time	t_{SUMODE} t_{SUA1} t_{SUA2}	10			μs	
MODE A_1 A_2 Hold Time	t_{HDMODE} t_{HDA1} t_{HDA2}	10			μs	
CS Pulse Width	$CS_{MIN.}$	10			μs	

6

1 024 bit EEPROM

DESCRIPTION

μPD6253 is a 1 024 bit (128 words x 8 bits) Electrically Erasable Programmable Read Only Memory (EEPROM) device.

The 2/3-wire serial bus interface is used to read/write data from/to this device. μPD6253 can be used for a wide range of applications such as the preset memory for TV, VTR, and OA equipment and the ID code memory for home automation equipment.

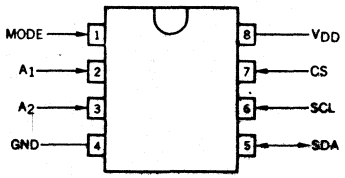
FEATURES

- Built-in 1 024-bit (128 x 8) EEPROM
- Two/three-wire serial interface
- Number of write operations: 100 000
- Memory retention period: 10 years
- Operation voltage: 5 V ±10 %, single power supply

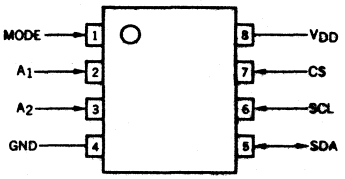
ORDERING INFORMATION

Order Code	Package
μPD6253CX	8 PIN PLASTIC DIP (300 mil)
μPD6253GS-BA1	8 PIN PLASTIC SOP (300 mil)

PIN CONFIGURATION (Top View)



μPD6253CX

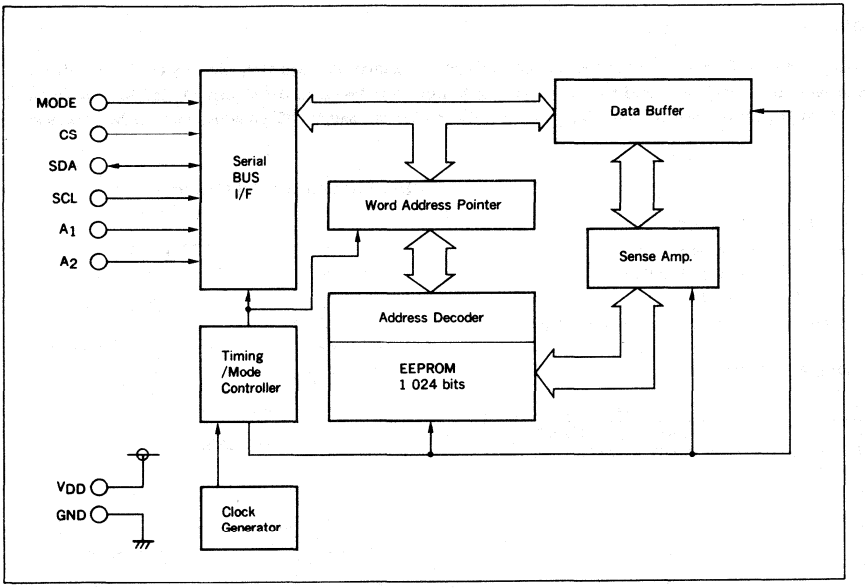


μPD6253GS

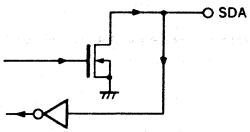
6

BLOCK DIAGRAM

Fig. 1



PIN FUNCTIONS

PIN No.	PIN NAME	INPUT/ OUTPUT	FUNCTION
1	MODE	Input	This is the terminal for selecting the system to interface with external devices. "H" ..... Three-wire serial bus interface. This can be controlled by setting the CS terminal to "H" or "L." "L" ..... Two-wire serial bus interface. The CS terminal can be used with the device set to "H."
2 3	A_1 A_2	Input	These pins are used only when the 2-wire serial bus interface is selected by setting the ODE terminal to "L." Setting A_1 and A_2 enables a slave address to be determined "H" level ..... Set to "1." "L" level ..... Set to "0." Slave address. 1 0 1 0 A_2 A_1 0 MSB → Variable by external setting. Slave address. Variable by external setting. If the MODE terminal is set to "H" and the 3-wire serial bus interface is selected, these terminals have no meaning. Use these terminals by setting them to "H" or "L" level.
4	GND	Input	(–) power terminal
5	SDA	Input/ Output	This is a data input/output terminal. Since this is an Nch open drain input/output, be sure to add an external pull-up resistor. 
6	SCL	Input	This is the clock input terminal for data transfer. For detailed operation, see the explanation provided later.
7	CS	Input	This is a chip-select terminal. When this signal is "H," this IC becomes operational. Setting this signal to "L" disables data reading/writing from/to each memory cell. If the MODE terminal is set to "H," changing this terminal from "L" to "H" when the SDL terminal is "H" signals the start of the serial bus interface operation; changing this terminal from "H" to "L" signals the end of the serial bus interface operation. The MODE terminal can be set to "L" when this terminal is always set to "H."
8	V_{DD}	Input	(+) power supply terminal 5 V ±10 %

6

1. FUNCTION OUTLINE

1.1 Mode Selection (three/two-wire Serial Bus Interface Mode)

Setting the MODE terminal (Pin 1) to "H" ("L") selects the three-wire serial bus interface mode (two-wire serial bus mode).

MODE terminal (Pin 1)
"H" ..... Three-wire serial bus interface mode
"L" ..... Two-wire serial bus interface mode

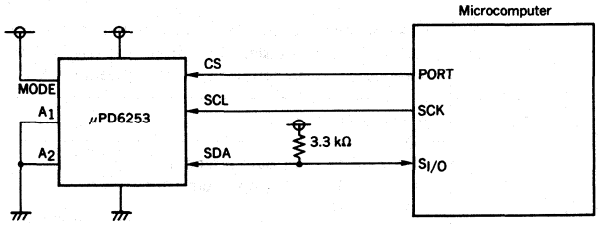
NOTE: Do not change the setting (H or L) of the MODE terminal during data transfer. To change the setting of the MODE terminal, be sure to set the CS terminal (Pin 7) to "H."

Setting both the MODE and CS terminals to "L" enables the device to enter the standby state and reduce power consumption.

1.2 Three-wire Serial Bus Interface Mode (MODE = H)

In the three-wire serial bus interface mode, three terminals CS (Pin 7), SCL (Pin 6), and SDA (Pin 5) can be used to read and write data.

(Connection) Fig. 2

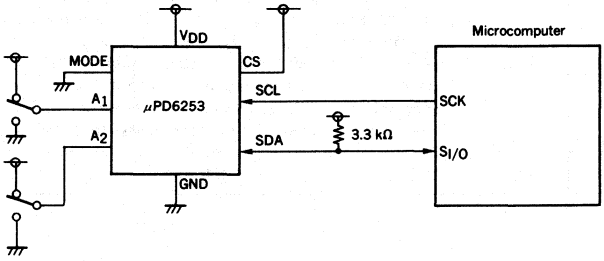


* Be sure to set terminals A_1 and A_2 to "H" or "L".

1.3 Two-wire Serial Bus Interface Mode (MODEL = L)

In the two-wire serial bus interface mode, two terminals, SCL (Pin 6) and SDA (Pin 5), can be used to read and write data.

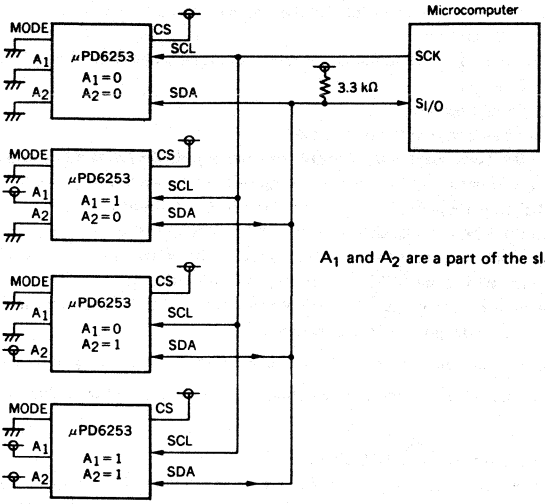
(Connection) Fig. 3



* Be sure to set A_1 and A_2 to "H" or "L" (set slave address).

Using multiple μPD6253 devices (up to four devices can be cascaded)

Fig. 4



A_1 and A_2 are a part of the slave address.

In the two-wire serial bus interface mode, data transfer is enabled only when the input slave address matches the slave address of this device.

Slave address configuration (7 bits)

1	0	1	0	A_2	A_1	0

A_2 and A_1 can be set by external terminals.

1.4 Write Protect Function

When supply voltage V_{DD} is 2.0 V or lower, write operation is inhibited.

2. THREE-WIRE SERIAL BUS INTERFACE OPERATION (MODE = H)

2.1 Basic Operation Sequence

(1) Start condition (STA).
To start the interface, set the SCL terminal to "H" then change the CS terminal from "L" to "H". Data transfer starts at the rising edge of the CS terminal.

(2) After the rising edge is input to the CS terminal, the microcomputer sends an 8-bit command.
SDA ..... Data input
SCL ..... Serial clock input
Serial data is read at the rising edge of the serial clock.

(3) After reception of the 8-bit command data, the SDA terminal of μPD6253 enters the output mode.
If this 8-bit command is accepted, the SDA terminal outputs the "L" level; if not, it outputs the "H" level.*
This status lasts until eight clock pulses have been input to the SCL terminal.
The data output from the SDA terminal changes at the falling edge of the serial clock.
This mode is used to check the internal status of μPD6253. If the signal output from the SDA terminal is "H" in this mode, the device is in the Write Busy [WB] state, so stop the data transfer.
To suspend the data transfer, change the CS terminal from "H" to "L." To restart the data transfer, change the CS terminal from "L" to "H" and input the 8-bit command.

* **NOTE:** The SDA terminal configuration is Nch opendrain so that the "H" level output is the high impedance state.

(4) If μPD6253 is not in the WB state, the internal status can be determined according to the 8-bit command shown below.

1. RANDOM WRITE command [$\overset{\text{MSB}}{0}0000000_B$]
After inputting the word address (WA, 8 bits but WA_7 is a dummy bit : to input "0") from the SDA terminal, input the write data (8 bits). Write data of up to three bytes can be continuously received. Data bytes 1 to 3 are sequentially written to the memory from the specified word address according to the number of data bytes in the internal write cycle after the falling edge of the CS terminal. In the internal write cycle, the device enters the WB state to disable the input of any command, so suspend data transfer until after the internal write cycle as previously described.

2. CURRENT READ command [$\overset{\text{MSB}}{1}0000000_B$]
Reads data from the word address at execution of the 8-bit command. After eight data bits are read from the SDA terminal, the word address is incremented by 1 to enable sequential reading of data. To end data reading, set the CS terminal from "H" to "L."

3. RANDOM READ command [$\overset{\text{MSB}}{1}1000000_B$]
When a word address (WA, 8 bits but WA_7 is a dummy bit : to input "0") is input from the SDA terminal, the memory contents specified by this word address are transferred to the read data buffer. After eight data bits are read from the SDA terminal, the word address (WA) is incremented by 1 to enable sequential reading of data.
To end data reading, set the CS terminal from "H" to "L."

(5) Stop condition (STP)
To end data transfer, be sure to set the CS terminal low. This causes this LSI to recognize the end of data transfer and enables it to receive a new command. To set the CS terminal low, be sure to keep the SCL terminal to "H."

2.2 Three-wire Serial Bus Interface Command List

The command to be used in the three-wire serial bus interface are shown in Table 1. Each command consists of eight bits.

Table 1 Three-wire Serial Bus Interface Command List

COMMAND NAME	COMMAND	OPERATION
RANDOM WRITE	00000000_B [00H] MSB C_7 to C_0	Transfers write data after a word address (WA, 8 bits) is set. Up to three write data bytes can be set sequentially. Correspondence between word addresses and data bytes: WA . . . . . Data byte 1 WA+1 . . . . . Data byte 2 WA+2 . . . . . Data byte 3 Writing is performed in the internal write cycle after the CS terminal is set low.
CURRENT READ	10000000_B [80H] MSB C_7 to C_0	Transfers the memory contents specified by the word address (current address) at the input of this command to the read data buffer. After eight data bits are read, the word address is incremented and the corresponding memory contents are transferred to the read data buffer.
RANDOM READ	11000000_B [C0H] MSB C_7 to C_0	After a word address is set, starts reading data with the set word address. This command differs from the CURRENT READ command in that the word address is set after execution of the command. After the word address is set, this command performs the same operation as the CURRENT READ command.

2.3 Updating Word Address

The word address is updated if an 8-bit word address is input in the RANDOM READ/WRITE mode. After every data byte is read in the READ mode, the word address is incremented by 1 and is thus sequentially updated.

In the write mode, after the stop bit is recognized, the word address is updated in the internal write cycle to write the internally transferred data to memory.

In the WRITE mode, if the start bit is recognized again after the stop bit is recognized (before data is written to memory), the word address retains the value at the recognition of the start bit and data is not written to memory.

If the word address is incremented when it is "7FH," it is reset to "0 0H" to continue the read or write operation.

2.4 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the CS terminal to "H" when the SCL terminal is "H."

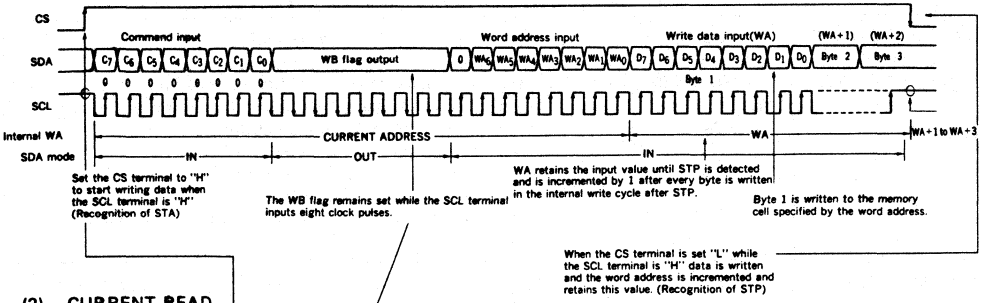
(2) Recognition of the stop bit (STP)
To end data transfer, set the CS terminal to "L" when the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, the transferred data is not written to memory.

If the data transfer start operations are executed sequentially, a command can be input after the last data transfer starts. If the data transfer end operations are executed sequentially, the internal status is determined during the first data transfer end operation.

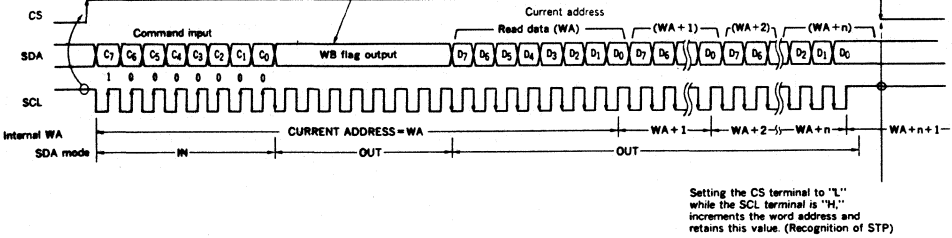
If the CS terminal is changed between "H" and "L" when the SCL terminal is "L," the internal status remains unchanged.

2.5 Three-wire Serial Bus Interface Timing

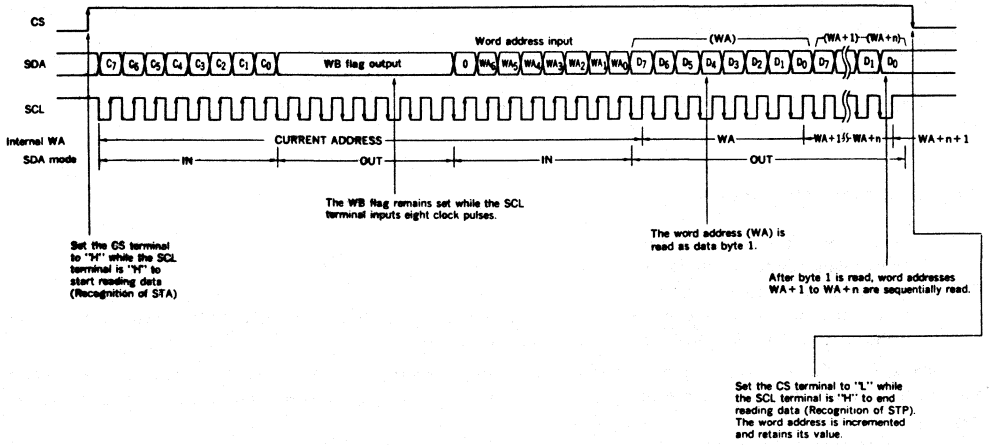
(1) RANDOM WRITE



(2) CURRENT READ



(3) RANDOM READ



3. TWO-WIRE SERIAL BUS INTERFACE OPERATION EXPLANATION (MODEL = L)

3.1 Basic Operation Sequence

Two-wire serial bus interface can be used when the CS terminal is set to "H," not when it is set to "L."

(1) To use the interface, set the SCL terminal to "H" and the SDA terminal to "L" (Recognition of the start bit (STA)).

(2) After starting the interface operation (after recognition of STA), input the clock from the SDL terminal.
In synchronization with this clock, input seven slave address bits and one *READ/$\overline{\text{WRITE}}$ mode selection bit to this LSI from the SDA terminal.
Data is input on the rising edge of the clock.

(3) If the input slave address matches **the slave address of this LSI, one acknowledge signals (ACK) bit is output syncronized with the fall of the eight clock pulse after the input of the READ/$\overline{\text{WRITE}}$ signal.

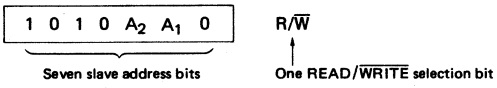
$\overline{\text{ACK}}$ signal

H ..... Output if the input slave address does not match the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

$\overline{\text{ACK}}$ signal

L ..... Output if the input slave address matches the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

*, ** Slave address and READ/$\overline{\text{WRITE}}$ signal data configurations after the start of the interface operation



A_1 and A_2 can be determined by setting the A_1 and A_2 terminals.

"H" 1

"L" 0

(4) After this LSI outputs the ACK signal properly, the operation is performed in the READ or WRITE mode.

1. WRITE mode

After the output of the SCK signal, input an 8-bit word address (WA_7 is a dummy bit : to input "0") from the SDA terminal. If the word address is correctly set, one ACK signal bit (set to "L") is output synchronized with the fall edge of the clock pulse right after the clock pulse input to the SCL terminal.

After the word address is set, input eight data bits to be written. If these data bits are correctly input, the ACK signal (set to "L") is output. Up to three write data bytes can be input at one time. Continue inputting eight data bits and confirming the ACK signal (set to "L") three times. The correspondence between the word addresses and data bytes is shown below.

Byte 1 ..... WA

Byte 2 ..... WA + 1

Byte 3 ..... WA + 2

To write more than three bytes of data, the $\overline{\text{ACK}}$ signal (set to "H") is output as bit 9 after the input of byte 4 (the three bytes immediately before the stop bit (STP) is recognized are actually written).

When the SDA terminal goes to "H" while the SCK terminal is "H" to end the interface operation (when STP is recognized), data starts being written automatically in the internal write cycle. The internal word address is incremented by 1 after every byte is written.

2. READ mode

After the output of the ACK signal, the memory contents specified by the internal word address already set are sequentially read synchronized with the fall of the clock pulse input to the SCL terminal. After eight data bits have been input, the ACK signal (set to "L") is input. This ACK signal is fetched at the rising edge of the clock. After the ACK signal is fetched, the word address is automatically incremented to allow sequential reading of data.

If the $\overline{ACK}$ signal (set to "H") is input, the word address is not incremented and the SDA terminal enters the input state. Input the stop bit (STP) and the start bit (STA) again to start the interface operation or continues inputting the clock pulses and input the ACK signal (set to "L") as the ninth clock pulse to restart the interface operation. If the interface operation is restarted by the input of the ACK signal (set to "L"), the word address (WA) is incremented at this ACK signal input. (See the Fig. 5)

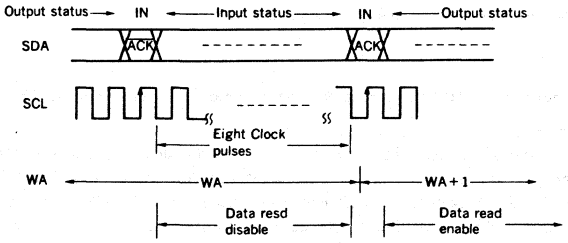
To end the READ mode, input the $\overline{ACK}$ signal (set to "H") instead of the ACK signal (set to "L") and set the SDA terminal to "L" when the SCL terminal has been already set to "H" (recognition of STP). In this case, the word address is not incremented so that the data in this address is read when the interface enters the READ mode again.

To read the data in a word address, set the word address in the WRITE mode, Input the start bit (STA) again to set the interface in the READ mode, and read the data.

Data Transfer Restart Method at Input of $\overline{ACK}$ Signal in READ Mode

1. Input STP, Input STA again, and input the slave address and the R/$\overline{W}$ signal.
2. Input the ACK signal (set to "L") at the input of the ninth clock pulse.

Fig. 5



(5) To end data transfer, set the SDA terminal to "H" after the SCL terminal is set to "H" (recognition of stop bit (STP)).

3.2 Updating Word Address

In the WRITE mode, update the word address at the end of the input of eight word address bits and at the start of the internal memory write operation by recognition of the stop bit after the input of write data.

In the READ mode, the word address is incremented at the input of the ACK signal (set to "L") after data is read.

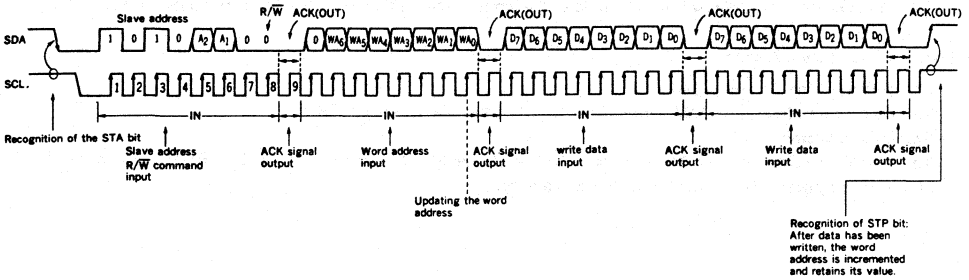
3.3 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the SDA terminal to "L" while the SCL terminal is "H."

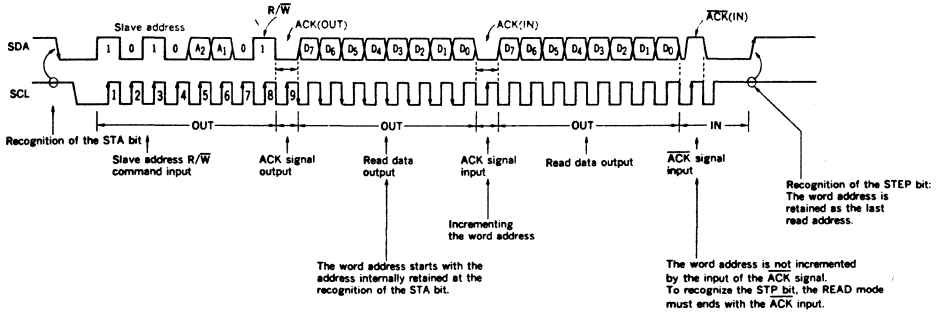
(2) Recognition of stop bit (STP)
To end data transfer, set the SDA terminal to "H" while the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, data cannot be written to memory.

3.4 Two-wire Serial Bus Interface Operation Timing

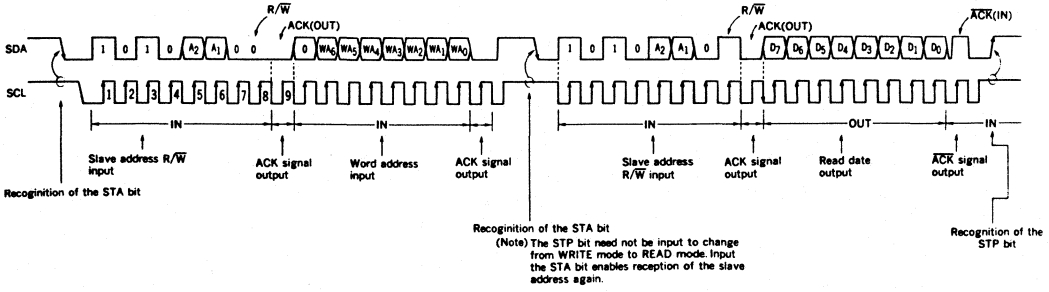
(1) WRITE mode (two bytes)



(2) READ mode (two bytes)



(3) READ mode



ELECTRICAL CHARACTERISTICS

MAXIMUM ABSOLUTE RATING (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	0.3 to V_{DD}+0.3	V
Output Voltage	V_O	−0.3 to V_{DD}+0.3	V
Operation Temperature	T_a	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +125	°C

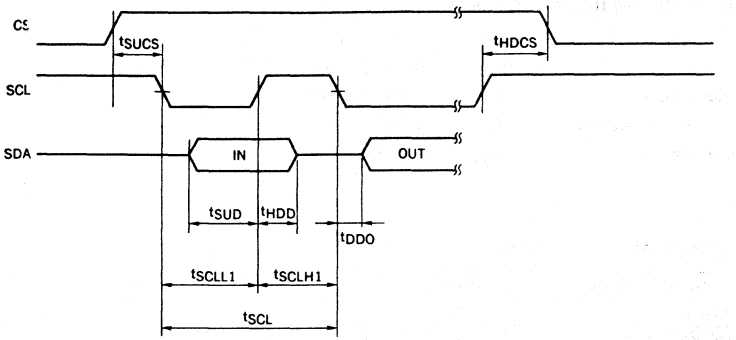
RECOMMENDED OPERATION RANGE (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Data Retaining Voltage	V_{DR}	0		5.5	V	
Number of Data Write/Erase Operation	N	10^6			Time	
Number of Data Retaining Years	Y	10			Year	
Operation Temperature	T_a	−20		+70	°C	

DC CHARACTERISTICS (T_a = −20 °C to +70 °C, V_{DD} = 4.5 to 5.5 V)

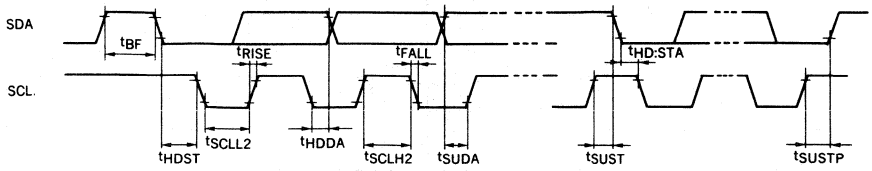
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High-level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low-level Input Voltage	V_{IL}			0.3 V_{DD}	V	
Low-level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3 mA, Nch open drain
Input Leak Current	I_{IL}	−10	0	10	μA	V_I = 0 to V_{DD}
Circuit Current 1	I_{DD1}			4	mA	In operation
Circuit Current 2	I_{DD2}			100	μA	At standby (CS = L, MODE = L)

AC CHARACTERISTIC 1 (three-wire serial bus interface, T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
CS Setup Time	t_{SUCS}	100			ns	
CS Hold Time	t_{HDCS}	100			ns	
SCL Cycle Time	t_{SCL}	1.0			μs	
SCL Low-level Time	t_{SCLL1}	400			ns	
SCL High-level Time	t_{SCLH1}	400			ns	
Input Data Setup Time	t_{SUD}	100			ns	
Input Data Hold Time	t_{HDD}	100			ns	
Output Data Delay Time	t_{DDO}			300	ns	R_L = 3.3 kΩ, C_L = 20 pF
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

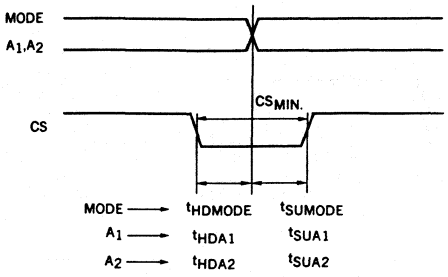
AC CHARACTERISTIC 2 (two-wire serial bus interface, T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
SCL Input Clock Frequency	f_{SCL}	0		100	kHz	
Bus Opening Time Before the Start of Data Transfer	t_{BF}	4.7			μs	
Start Condition Hold Time	t_{HDST}	4.0			μs	
SCL Low-level Time	t_{SCLL2}	4.7			μs	
SCL High-level Time	t_{SCLH2}	4.0			μs	
Start Condition Setup Time	t_{SUST}	4.7			μs	
Data Hold Time	t_{HDDA}	0			μs	**Note:** Data is retained when SCL is set to "H."
Data Setup Time	t_{SUDA}	250			ns	
SDA/SCL Signal Rise Time	t_{RISE}			1	μs	
SDA/SCL Signal Fall Time	t_{FALL}			300	ns	
Stop Condition Setup Time	t_{SUSTP}	4.7			μs	
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

Note 1: Internal write cycle time is defined to be the period when μPD6253 is in WB (WRITE BUSY) mode.
Following operation indicates that μPD6253 is in WB mode:
(1) In case that three-wire serial bus interface is in operation, "H" level is output for WB flog output.
(2) In case that two-wire serial bus interface is in operation, $\overline{ACK}$ signal ("H" level) is output after slave address is input.
In WB mode, data writing and reading operation are not available.

AC CHARACTERISTIC 3 (CS ↔ MODE A_1, A_2 T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
MODE A_1 Setup Time A_2	t_{SUMODE} t_{SUA1} t_{SUA2}	10			μs	
MODE A_1 Hold Time A_2	t_{HDMODE} t_{HDA1} t_{HDA2}	10			μs	
CS Pulse Width	$CS_{MIN.}$	10			μs	

4 096 bit EEPROM

DESCRIPTION

μPD6254 is a 4 096-bit (512 words x 8 bits) Electrically Erasable Programmable Read Only Memory (EEPROM) device.

The 2/3-wire serial bus interface is used to read/write data from/to this device. μPD6254 can be used for a wide range of applications such as the preset memory for TV, VTR, and OA equipment and the ID code memory for home automation equipment.

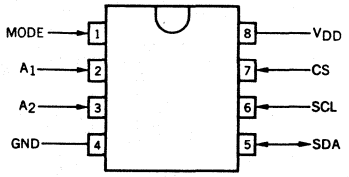
FEATURES

- Built-in 4 096-bit (512 x 8) EEPROM
- Two/three-wire serial interface
- Number of write operations: 100 000
- Memory retention period: 10 years
- Operation voltage: 5 V ±10 %, single power supply

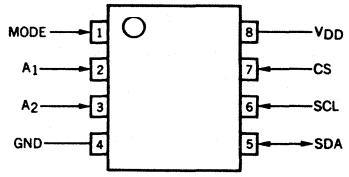
ORDERING INFORMATION

Order Code	Package
μPD6254CX	8-Pin Plastic DIP (300 mil)
μPD6254GS-BA1	8-Pin Plastic SOP (300 mil)

PIN CONFIGURATION (Top View)



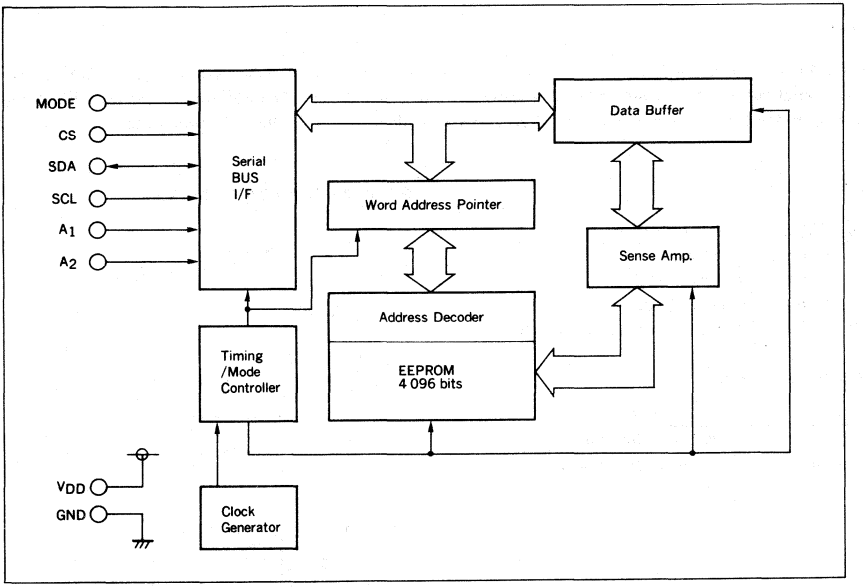
μPD6254CX



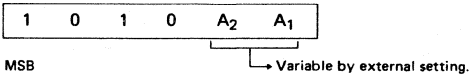
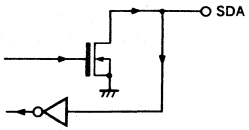
μPD6254GS

BLOCK DIAGRAM

Fig. 1



PIN FUNCTIONS

PIN NO.	PIN NAME	INPUT/ OUTPUT	FUNCTION
1	MODE	Input	This is the terminal for selecting the system to interface with external devices. "H" ..... Three-wire serial bus interface. This can be controlled by setting the CS terminal to "H" or "L." "L" ..... Two-wire serial bus interface. The CS terminal can be used with the device set to "H."
2 3	A_1 A_2	Input	These pins are used only when the 2-wire serial bus interface is selected by setting the ODE terminal to "L." Setting A_1 and A_2 enables a slave address to be determined "H" level ..... Set to "1." "L" level ..... Set to "0." Slave address.  Slave address. Variable by external setting. If the MODE terminal is set to "H" and the 3-wire serial bus interface is selected, these terminals have no meaning. Use these terminals by setting them to "H" or "L" level.
4	GND	Input	(–) power terminal
5	SDA	Input/ Output	This is a data input/output terminal. Since this is an Nch open drain input/output, be sure to add an external pull-up resistor. 
6	SCL	Input	This is the clock input terminal for data transfer. For detailed operation, see the explanation provided later.
7	CS	Input	This is a chip-select terminal. When this signal is "H," this IC becomes operational. Setting this signal to "L" disables data reading/writing from/to each memory cell. If the MODE terminal is set to "H," changing this terminal from "L" to "H" when the SDL terminal is "H" signals the start of the serial bus interface operation; changing this terminal from "H" to "L" signals the end of the serial bus interface operation. The MODE terminal can be set to "L" when this terminal is always set to "H."
8	V_{DD}	Input	(+) power supply terminal 5 V ±10 %

1. FUNCTION OUTLINE

1.1 Mode Selection (three/two-wire Serial Bus Interface Mode)

Setting the MODE terminal (Pin 1) to "H" ("L") selects the three-wire serial bus interface mode (two-wire serial bus mode.)

MODE terminal (Pin 1)
"H" ..... Three-wire serial bus interface mode
"L" ..... Two-wire serial bus interface mode

NOTE: Do not change the setting (H or L) of the MODE terminal during data transfer. To change the setting of the MODE terminal, be sure to set the CS terminal (Pin 7/13) to "H."

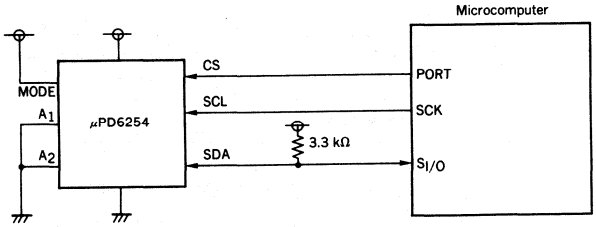
Setting both the MODE and CS terminals to "L" enables the device to enter the standby state and reduce power consumption.

1.2 Three-wire Serial Bus Interface Mode (MODE = H)

In the three-wire serial bus interface mode, three terminals CS (Pin 7), SCL (Pin 6), and SDA (Pin 5) can be used to read and write data.

(Connection)

Fig. 2



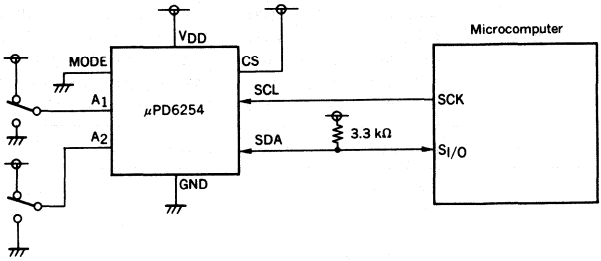
* Be sure to set terminals A_1 and A_2 to "H" or "L".

1.3 Two-wire Serial Bus Interface Mode (MODEL = L)

In the two-wire serial bus interface mode, two terminals, SCL (Pin 6) and SDA (Pin 5), can be used to read and write data.

(Connection)

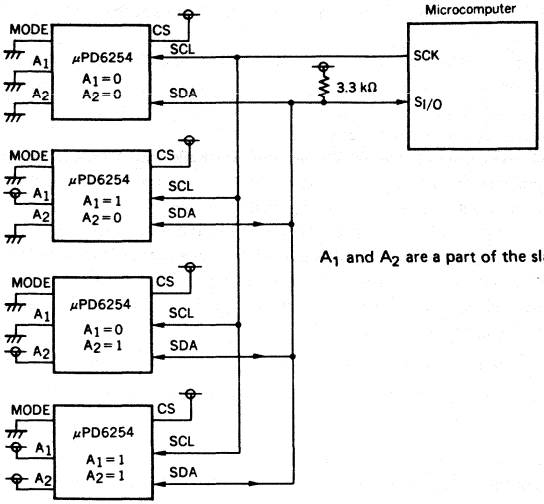
Fig. 3



* Be sure to set A_1 and A_2 to "H" or "L" (set slave address).

Using multiple μPD6254 devices (up to four devices can be cascaded)

Fig. 4



A_1 and A_2 are a part of the slave address.

In the two-wire serial bus interface mode, data transfer is enabled only when the input slave address matches the slave address of this device.

Slave address configuration (6 bits)

1	0	1	0	A_2	A_1

A_2 and A_1 can be set by external terminals.

1.4 Write Protect Function

When supply voltage V_{DD} is 2.0 V or lower, write operation is inhibited.

2. THREE-WIRE SERIAL BUS INTERFACE OPERATION (MODE = H)

2.1 Basic Operation Sequence

(1) Start condition (STA).
To start the interface, set the SCL terminal to "H" then change the CS terminal from "L" to "H". Data transfer starts at the rising edge of the CS terminal.

(2) After the rising edge is input to the CS terminal, the microcomputer sends an 8-bit command.
SDA ..... Data input
SCL ..... Serial clock input
Serial data is read at the rising edge of the serial clock.

(3) After reception of the 8-bit command data, the SDA terminal of μPD6254 enters the output mode.
If this 8-bit command is accepted, the SDA terminal outputs the "L" level; if not, it outputs the "H" level.*
This status lasts until eight clock pulses have been input to the SCL terminal.
The data output from the SDA terminal changes at the falling edge of the serial clock.
This mode is used to check the internal status of μPD6254. If the signal output from the SDA terminal is "H" in this mode, the device is in the Write Busy [WB] state, so stop the data transfer.
To suspend the data transfer, change the CS terminal from "H" to "L." To restart the data transfer, change the CS terminal from "L" to "H" and input the 8-bit command.

* **NOTE:** The SDA terminal configuration is Nch opendrain so that the "H" level output is the high impedance state.

(4) If μPD6254 is not in the WB state, the internal status can be determined according to the 8-bit command shown below.

1. RANDOM WRITE command [$\overset{\text{MSB}}{0}\ 0\ 0\ WA_8\ 0\ 0\ 0\ 0_B$]
After inputting the word address (WA, 9 bits but WA_8 is determined in the command) from the SDA terminal, input the write data (8 bits). Write data of up to three bytes can be continuously received. Data bytes 1 to 3 are sequentially written to the memory from the specified word address according to the number of data bytes in the internal write cycle after the falling edge of the CS terminal. In the internal write cycle, the device enters the WB state to disable the input of any command, so suspend data transfer until after the internal write cycle as previously described.

2. CURRENT READ command [$\overset{\text{MSB}}{1}\ 0\ 0\ 0\ 0\ 0\ 0\ 0_B$]
Reads data from the word address at execution of the 8-bit command. After eight data bits are read from the SDA terminal, the word address is incremented by 1 to enable sequential reading of data. To end data reading, set the CS terminal from "H" to "L."

3. RANDOM READ command [$\overset{\text{MSB}}{1}\ 1\ 0\ WA_8\ 0\ 0\ 0\ 0_B$]
When a word address (WA, 9 bits but WA_8 is determined in the command) is input from the SDA terminal, the memory contents specified by this word address are transferred to the read data buffer. After eight data bits are read from the SDA terminal, the word address (WA) is incremented by 1 to enable sequential reading of data.
To end data reading, set the CS terminal from "H" to "L."

(5) Stop condition (STP)
To end data transfer, be sure to set the CS terminal low. This causes this LSI to recognize the end of data transfer and enables it to receive a new command. To set the CS terminal low, be sure to keep the SCL terminal to "H."

2.2 Three-wire Serial Bus Interface Command List

The command to be used in the three-wire serial bus interface are shown in Table 1. Each command consists of eight bits.

Table 1 Three-wire Serial Bus Interface Command List

COMMAND NAME	COMMAND	OPERATION
RANDOM WRITE	$000WA_8 0000_B$ MSB C_7 to C_0	Transfers write data after a word address (WA, 8 bits) is set. Up to three write data bytes can be set sequentially. Correspondence between word addresses and data bytes: WA ..... Data byte 1 WA+1 ..... Data byte 2 WA+2 ..... Data byte 3 Writing is performed in the internal write cycle after the CS terminal is set low.
CURRENT READ	10000000_B MSB C_7 to C_0	Transfers the memory contents specified by the word address (current address) at the input of this command to the read data buffer. After eight data bits are read, the word address is incremented and the corresponding memory contents are transferred to the read data buffer.
RANDOM READ	$110WA_8 0000_B$ MSB C_7 to C_0	After a word address is set, starts reading data with the set word address. This command differs from the CURRENT READ command in that the word address is set after execution of the command. After the word address is set, this command performs the same operation as the CURRENT READ command.

2.3 Updating Word Address

The word address is updated if a 9-bit word address is input in the RANDOM READ/WRITE mode. After every data byte is read in the READ mode, the word address is incremented by 1 and is thus sequentially updated.

In the write mode, after the stop bit is recognized, the word address is updated in the internal write cycle to write the internally transferred data to memory.

In the WRITE mode, if the start bit is recognized again after the stop bit is recognized (before data is written to memory), the word address retains the value at the recognition of the start bit and data is not written to memory.

If the word address is incremented when it is "1FFH," it is reset to "000H" to continue the read or write operation.

2.4 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the CS terminal to "H" when the SCL terminal is "H."

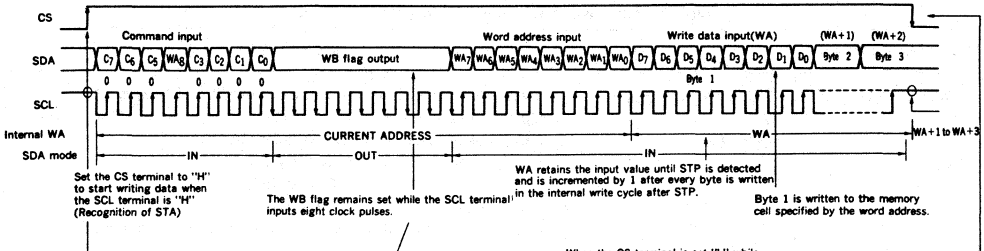
(2) Recognition of the stop bit (STP)
To end data transfer, set the CS terminal to "L" when the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, the transferred data is not written to memory.

If the data transfer start operations are executed sequentially, a command can be input after the last data transfer starts. If the data transfer end operations are executed sequentially, the internal status is determined during the first data transfer end operation.

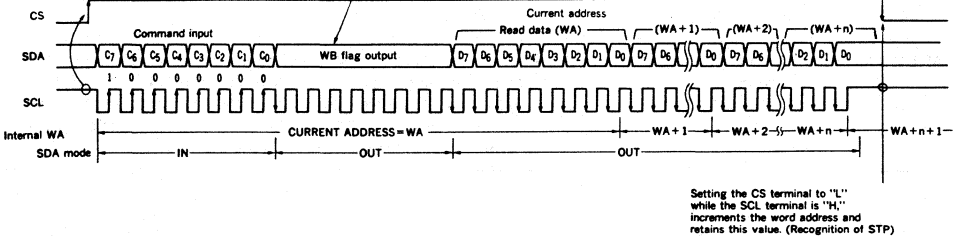
If the CS terminal is changed between "H" and "L" when the SCL terminal is "L," the internal status remains unchanged.

2.5 Three-wire Serial Bus Interface Timing

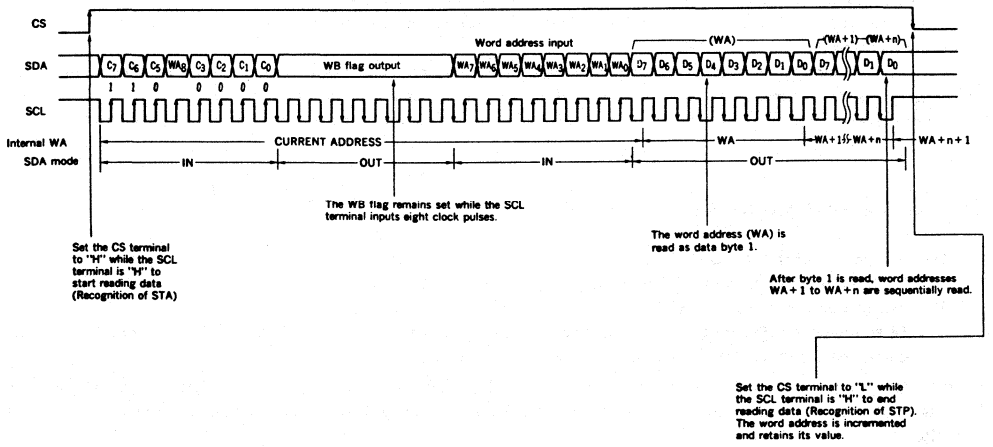
(1) RANDOM WRITE



(2) CURRENT READ



(3) RANDOM READ



3. TWO-WIRE SERIAL BUS INTERFACE OPERATION EXPLANATION (MODEL = L)

3.1 Basic Operation Sequence

Two-wire serial bus interface can be used when the CS terminal is set to "H," not when it is set to "L."

(1) To use the interface, set the SCL terminal to "H" and the SDA terminal to "L" (Recognition of the start bit (STA)).

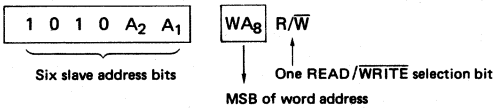
(2) After starting the interface operation (after recognition of STA), input the clock from the SDL terminal.
In synchronization with this clock, input six slave address bits, MSB of word address and one *READ/$\overline{\text{WRITE}}$ mode selection bit to this LSI from the SDA terminal.
Data is input on the rising edge of the clock.

(3) If the input slave address matches **the slave address of this LSI, one acknowledge signals (ACK) bit is output syncronized with the fall of the eight clock pulse after the input of the READ/$\overline{\text{WRITE}}$ signal.

$\overline{\text{ACK}}$ signal
H ..... Output if the input slave address does not match the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

$\overline{\text{ACK}}$ signal
L ..... Output if the input slave address matches the slave address of this LSI after the input of the R/$\overline{\text{W}}$ signal.

* ** Slave address and READ/$\overline{\text{WRITE}}$ signal data configurations after the start of the interface operation



A_1 and A_2 can be determined by setting the A_1 and A_2 terminals.
"H" 1
"L" 0

(4) After this LSI outputs the ACK signal properly, the operation is performed in the READ or WRITE mode.

1. WRITE mode
After the output of the SCK signal, input a remained 8-bit word address from the SDA terminal. If the word address is correctly set, one ACK signal bit (set to "L") is output synchronized with the fall edge of the clock pulse right after the clock pulse input to the SCL terminal.
After the word address is set, input eight data bits to be written. If these data bits are correctly input, the ACK signal (set to "L") is output. Up to three write data bytes can be input at one time. Continue inputting eight data bits and confirming the ACK signal (set to "L") three times. The correspondence between the word addresses and data bytes is shown below.

Byte 1 ..... WA
Byte 2 ..... WA + 1
Byte 3 ..... WA + 2

To write more than three bytes of data, the $\overline{\text{ACK}}$ signal (set to "H") is output as bit 9 after the input of byte 4 (the three bytes immediately before the stop bit (STP) is recognized are actually written).
When the SDA terminal goes to "H" while the SCK terminal is "H" to end the interface operation (when STP is recognized), data starts being written automatically in the internal write cycle. The internal word address is incremented by 1 after every byte is written.

2. READ mode

After the output of the ACK signal, the memory contents specified by the internal word address already set are sequentially read synchronized with the fall of the clock pulse input to the SCL terminal. After eight data bits have been input, the ACK signal (set to "L") is input. This ACK signal is fetched at the rising edge of the clock. After the ACK signal is fetched, the word address is automatically incremented to allow sequential reading of data.

If the $\overline{ACK}$ signal (set to "H") is input, the word address is not incremented and the SDA terminal enters the input state. Input the stop bit (STP) and the start bit (STA) again to start the interface operation or continues inputting the clock pulses and input the ACK signal (set to "L") as the ninth clock pulse to restart the interface operation. If the interface operation is restarted by the input of the ACK signal (set to "L"), the word address (WA) is incremented at this ACK signal input. (See the Fig. 5)

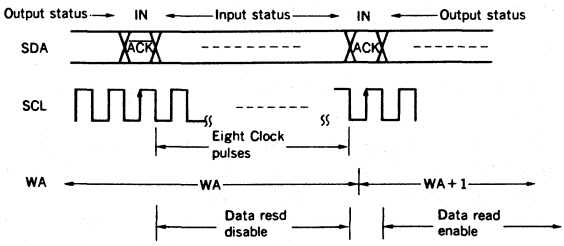
To end the READ mode, input the $\overline{ACK}$ signal (set to "H") instead of the ACK signal (set to "L") and set the SDA terminal to "L" when the SCL terminal has been already set to "H" (recognition of STP). In this case, the word address is not incremented so that the data in this address is read when the interface enters the READ mode again.

To read the data in a word address, set the word address in the WRITE mode, Input the start bit (STA) again to set the interface in the READ mode, and read the data.

Data Transfer Restart Method at Input of $\overline{ACK}$ Signal in READ Mode

1. Input STP, Input STA again, and input the slave address and the R/$\overline{W}$ signal.
2. Input the ACK signal (set to "L") at the input of the ninth clock pulse.

Fig. 5



(5) To end data transfer, set the SDA terminal to "H" after the SCL terminal is set to "H" (recognition of stop bit (STP)).

3.2 Updating Word Address

In the WRITE mode, update the word address at the end of the input of nine word address bits and at the start of the internal memory write operation by recognition of the stop bit after the input of write data.

In the READ mode, the word address is incremented at the input of the ACK signal (set to "L") after data is read.

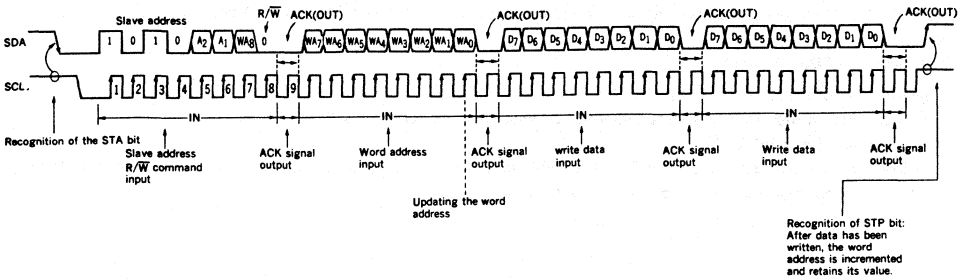
3.3 Start and End of Data Transfer

(1) Recognition of the start bit (STA)
To start data transfer, set the SDA terminal to "L" while the SCL terminal is "H."

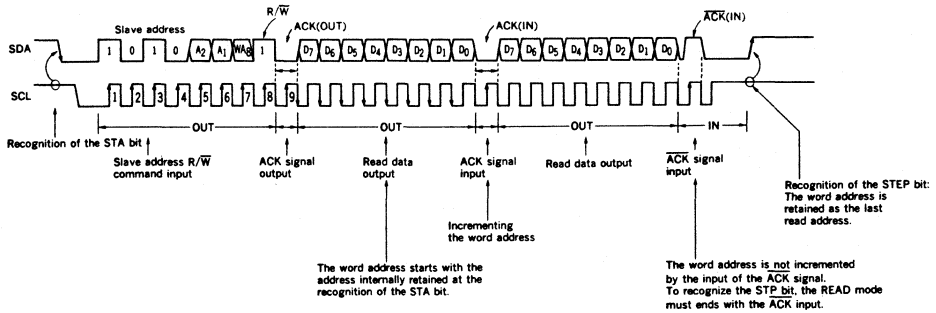
(2) Recognition of stop bit (STP)
To end data transfer, set the SDA terminal to "H" while the SCL terminal is "H." In the WRITE mode, if the stop bit is not recognized, data cannot be written to memory.

3.4 Two-wire Serial Bus Interface Operation Timing

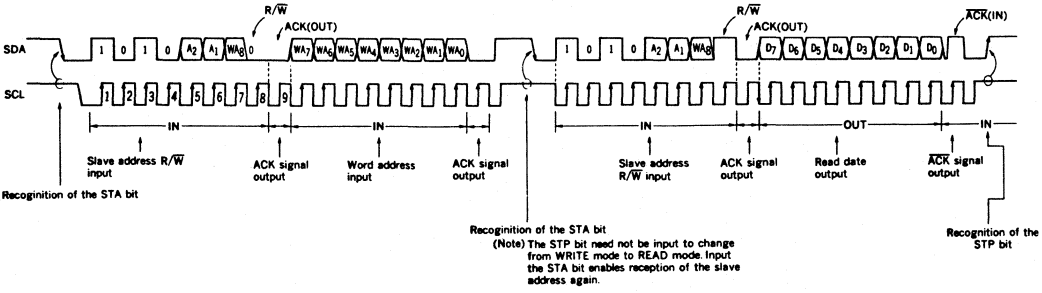
(1) WRITE mode (two bytes)



(2) READ mode (two bytes)



(3) READ mode



ELECTRICAL CHARACTERISTICS

MAXIMUM ABSOLUTE RATING (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	0.3 to V_{DD} +0.3	V
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V
Operation Temperature	T_a	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +125	°C

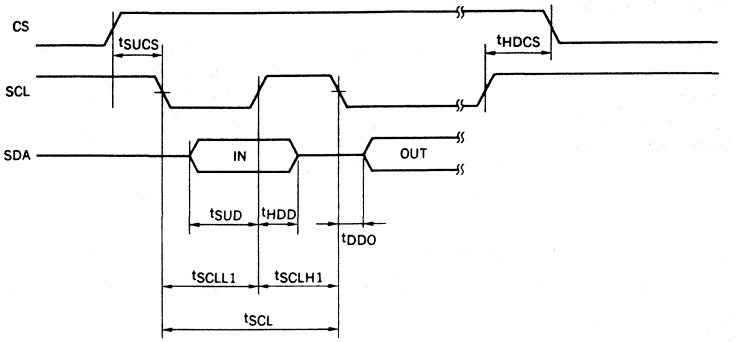
RECOMMENDED OPERATION RANGE (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Data Retaining Voltage	V_{DR}	0		5.5	V	
Number of Data Write/Erase Operation	N	10^6			Time	
Number of Data Retaining Years	Y	10			Year	
Operation Temperature	T_a	−20		+70	°C	

DC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

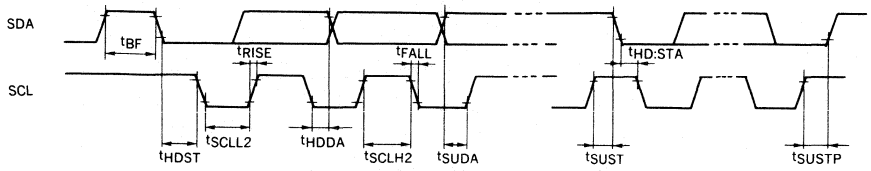
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High-level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low-level Input Voltage	V_{IL}			0.3 V_{DD}	V	
Low-level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3 mA, Nch open drain
Input Leak Current	I_{IL}	−10	0	10	μA	V_I = 0 to V_{DD}
Circuit Current 1	I_{DD1}			4	mA	In operation
Circuit Current 2	I_{DD2}			100	μA	At standby (CS = L, MODE = L)

AC CHARACTERISTIC 1 (three-wire serial bus interface, T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
CS Setup Time	t_{SUCS}	100			ns	
CS Hold Time	t_{HDCS}	100			ns	
SCL Cycle Time	t_{SCL}	1.0			μs	
SCL Low-level Time	t_{SCLL1}	400			ns	
SCL High-level Time	t_{SCLH1}	400			ns	
Input Data Setup Time	t_{SUD}	100			ns	
Input Data Hold Time	t_{HDD}	100			ns	
Output Data Delay Time	t_{DDO}			300	ns	R_L = 3.3 kΩ, C_L = 20 pF
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

AC CHARACTERISTIC 2 (two-wire serial bus interface, T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

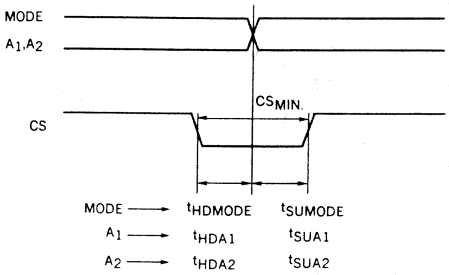


CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
SCL Input Clock Frequency	f_{SCL}	0		100	kHz	
Bus Opening Time Before the Start of Data Transfer	t_{BF}	4.7			μs	
Start Condition Hold Time	t_{HDST}	4.0			μs	
SCL Low-level Time	t_{SCLL2}	4.7			μs	
SCL High-level Time	t_{SCLH2}	4.0			μs	
Start Condition Setup Time	t_{SUST}	4.7			μs	
Data Hold Time	t_{HDDA}	0			μs	**Note:** Data is retained when SCL is set to "H."
Data Setup Time	t_{SUDA}	250			ns	
SDA/SCL Signal Rise Time	t_{RISE}			1	μs	
SDA/SCL Signal Fall Time	t_{FALL}			300	ns	
Stop Condition Setup Time	t_{SUSTP}	4.7			μs	
Internal Write Cycle Time (Note 1)	t_{WC}			40	ms	per 1 byte

Note 1: Internal write cycle time is defined to be the period when μPD6254 is in WB (WRITE BUSY) mode.
Following operation indicates that μPD6254 is in WB mode:
(1) In case that three-wire serial bus interface is in operation, "H" level is output for WB flog output.
(2) In case that two-wire serial bus interface is in operation, $\overline{ACK}$ signal ("H" level) is output after slave address is input.
In WB mode, data writing and reading operation are not available.

6

AC CHARACTERISTIC 3 (CS ↔ MODE A_1, A_2 T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
MODE A_1 Setup Time A_2	t_{SUMODE} t_{SUA1} t_{SUA2}	10			μs	
MODE A_1 Hold Time A_2	t_{HDMODE} t_{HDA1} t_{HDA2}	10			μs	
CS Pulse Width	$CS_{MIN.}$	10			μs	

Real-Time-Clock

Section 7 - Real-Time-Clock

Clock ICs

Device	Data type	I/O interface	Features	Supply voltage (V)	Pins/Package
μPD4990AC	BCD Hex (mont only)	Serial I/O (3 lines)	Built-in counter for time and date	2 to 5.5	14/DIP
μPD4990AG	BCD Hex (mont only)	Serial I/O (3 lines)	Leap years determined automatically	2 to 5.5	16/SOP
μPD4991ACX	BCD	4-bit parallel		2 to 5.5	18/DIP
μPD4991AGS	BCD	4-bit parallel		2 to 5.5	20/SOP

SERIAL I/O CALENDAR & CLOCK
CMOS LSI

DESCRIPTION

The μPD4990AC, μPD4990AG are a CMOS LSI chip developed to input/output calendar clock data serially to/from the micro computer.

The crystal frequency is 32.768 kHz and the data items included are about time, minute, second, year, month day, and week.

This chip is encased in a 14 pin DIP (dual in-line package) (μPD4990AC), and a 16 pin mini flat package (SOG) (μPD4990AG).

FEATURES

- The counters for time (hour, minute, and second) and date (year, month, day, and week) are built in.
- Leap years are determined automatically.
- Data is represented in BCD notation (only months are represented in hexadecimal notation) and input/output serially.
- Commands can be set by inputting data serially.
- Selective timing pulses (TPs) are 64 Hz, 256 Hz, 2 048 Hz, and 4 096 Hz and selective output intervals are 1, 10, 30, and 60 seconds.

ORDERING INFORMATION

Part Number	Package
μPD4990AC	14-pin plastic DIP (300 mil)
μPD4990AG	16-pin plastic SOP (300 mil)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$V_{DD}-V_{SS}$	7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating Temperature Range	T_{opt}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Output Terminal Voltage	V_{OUT}	7.0	V

ELECTRICAL CHARACTERISTICS (f=32.768 kHz, $C_G=C_D$=20 pF, CI=20 kΩ, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Operating Voltage	$V_{DD}-V_{SS}$	2.00		5.50	V	
Current Consumption	I_{DD}		8	20	μA	$V_{DD}-V_{SS}$=3.60 V
				100	μA	$V_{DD}-V_{SS}$=5.50 V
Low Level Output Voltage	V_{OL}			0.4*	μA	$V_{DD}-V_{SS}$=2.0~5.5 V I_{OL}=500 μA
CLK Input Frequency	f_{CLK}	DC		500	kHz	$V_{DD}-V_{SS}$=2.0 V, Duty 50 %
Input Leakage Current	I_{IN}			1	μA	$V_{DD}-V_{SS}$=5.50 V
High Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	V_{SS}		0.3 V_{DD}	V	

* TP and DATA OUT are N-channel open drain output.

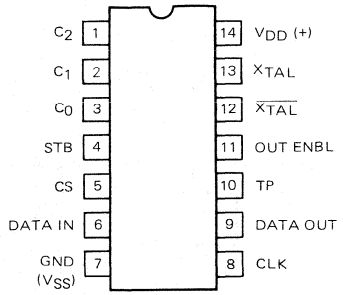
A.C. ELECTRICAL CHARACTERISTICS (FOR REFERENCE --- NOT SPECIFIED)

(f=32.768 kHz, $V_{DD}-V_{SS}$=2.0 V, T_a=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_0~2, CS–STB Set-up Time	t_{SU}	1			μs	
STB Pulse Width	t_{STB}	1			μs	
C_0~2, CS–STB Hold Time	t_{HLD}	1			μs	
STB LATCH Delay Time	t_{d1}			1**	μs	escept Time Read mode
CLK-DATA OUT Delay time	$t_{d(c-o)}$			1	μs	R_L=33 kΩ, C_L=15 pF
DATA IN Set-up Time	t_{DSU}	1			μs	
DATA IN Hold Time	t_{DHLD}	1			μs	

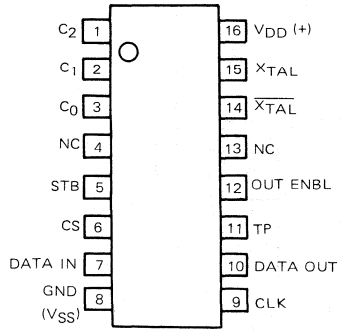
** **Note:** When a function mode is Time Read mode (other than Test mode), STB LATCH delay time is 20 μs MAX. (t_{d2}).

CONNECTION DIAGRAM (Top View)



μPD4990AC

NO.	Terminology	NO.	Terminology
1	C_2	8	CLK
2	C_1	9	DATA OUT
3	C_0	10	TP
4	STB	11	OUT ENBL
5	CS	12	$\overline{X_{TAL}}$
6	DATA IN	13	X_{TAL}
7	GND(V_{SS})	14	V_{DD}(+)



μPD4990AG

NO.	Terminology	NO.	Terminology
1	C_2	9	CLK
2	C_1	10	DATA OUT
3	C_0	11	TP
4	NC	12	OUT ENBL
5	STB	13	NC
6	CS	14	$\overline{X_{TAL}}$
7	DATA IN	15	X_{TAL}
8	GND(V_{SS})	16	V_{DD}(+)

NC: NO CONNECTION

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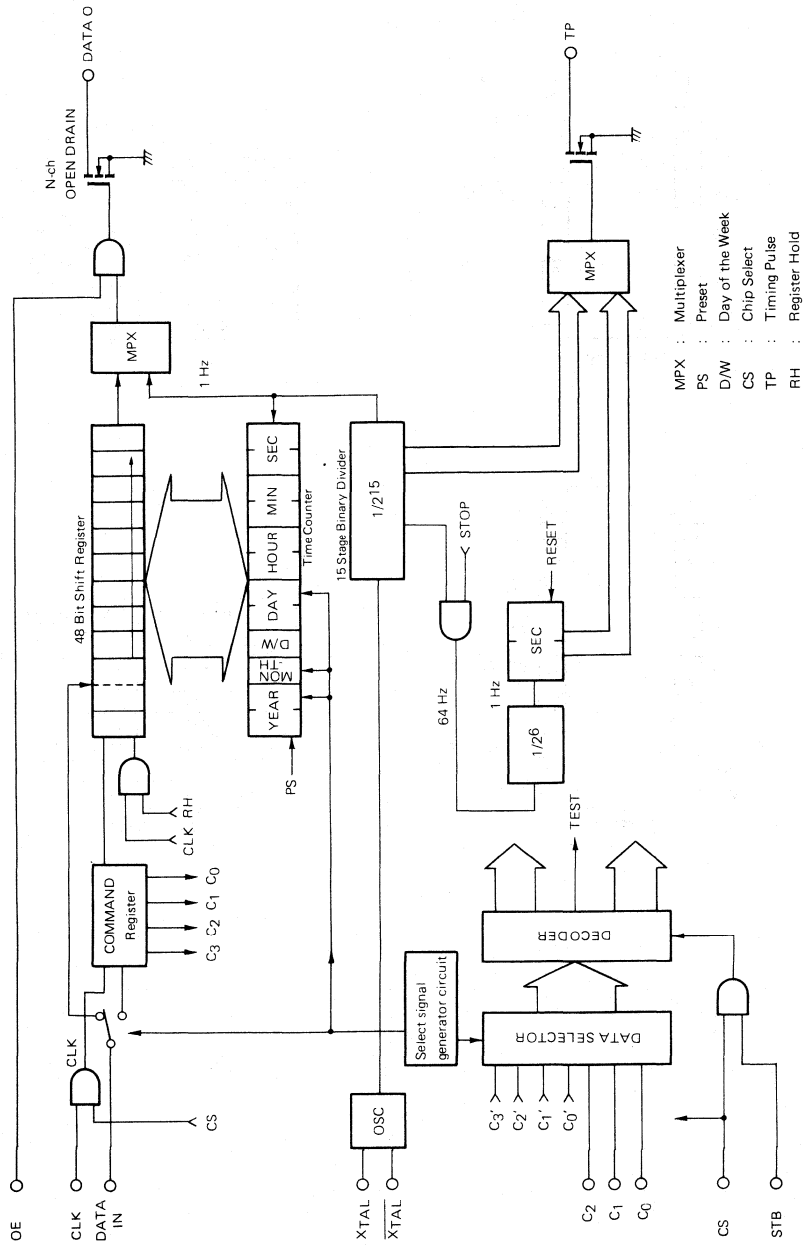
BLOCK DIAGRAM



FUNCTION SPECIFICATIONS

- Crystal frequency (X tal osc.).
  - 32.768 kHz

- Data

  Data types are: second, minute, day, week,month, and year.
  Leap years, 31-day months, and months with 30 or less days are determined automatically.
  A 24-hour system is used and last two digits of Gregorian year are indicated.
  It is assumed that leap years are expressed by multiples of 4.

- Data format

  Data is represented in BCD notation. Only months are represented in hexadecimal notation.

- Data input-output and Clock

  Data is input/output synchronously with reference to the external clocks input from the CLK pin using the serial input/output system. (See Fig. 1.)

- Timing pulse output

  Three frequencies, 64 Hz, 256 Hz, and 2 048 Hz, can be set with C_0, C_1, and C_2 pins.
  Using serial data input command, selective timing pulses (TPs) are 64 Hz, 256 Hz, 2 048 Hz, and 4 096 Hz and selective output intervals are 1, 10, 30, and 60 seconds.

- Function mode selection

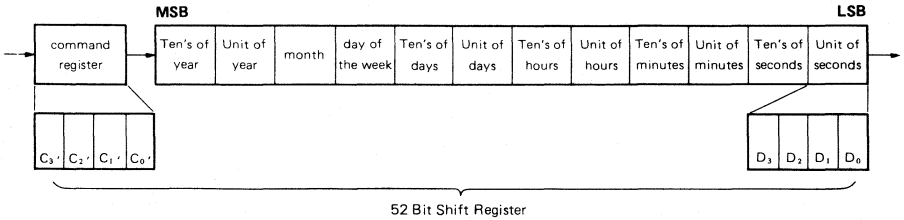
  A function mode can be selected by the inputs from C_0, C_1, and C_2. Also a function mode can be selected through serial data input. ($C_0 = C_1 = C_2 = V_{DD}$)
  Each command is latched with STB (strobe).

- Chip select

  Connecting the CS pin to the ground level inhibits CLK and STB inputs.

- Data output inhibition

  Connecting the OUT ENBL pin to the ground level sets the DATA OUT pin at high impedance.



* DATA of 52 Bit Shift Register appears on DATA OUT terminal from LSB of seond.

Fig. 1

TERMINALS

- Input terminals
  - DATA IN — Data input of 40-/52-bit shift register
  - CLK — Shift clock input of 40-/52-bit shift register
  - C_0, C_1, C_2 — Command input (3 bit)
  - STB — Strobe input
  - CS — Chip select input (Prohibits CLK & STB)
  - OUT ENBL — Output control input (Makes the DATA OUT high impedance by inputting low level).
- Output terminals (N-channel Open Drain)
  - DATA OUT — Data output of 40-/52-bit shift register
  - TP — Timing pulse output
- Oscillation terminals
  - X_{TAL} — Oscillation inverter input (OSC IN)
  - $\overline{X_{TAL}}$ — Oscillation inverter output (OSC OUT)
- Power supply terminals
  - V_{DD} — Plus power supply
  - GND (V_{SS}) — Common line

COMMAND SPECIFICATIONS

○ Commands input from C_0, C_1, and C_2 pins (1 . . . H, 0 . . . L)
Shift register 40 bit (The year function is ineffective.)
(Operates as the existing μPD1990AC in other than test mode)

C_2	C_1	C_0	FUNCTION	
0	0	0	Register Hold	DATA OUT = 1 Hz
0	0	1	Register Shift	DATA OUT = [LSB] = 0 or 1
0	1	0	Time Set & Counter Hold	DATA OUT = [LSB] = 0 or 1
0	1	1	Time Read	DATA OUT = 1 Hz
1	0	0	TP = 64 Hz	
1	0	1	TP = 256 Hz	
1	1	0	TP = 2 048 Hz	
1	1	1	Serial command transfer mode	

* The test mode is cancelled by $[C_2, C_1, C_0] = [0, 0, 0]$ to $[1, 1, 0]$.

○ Serial data commands
Set $[C_2, C_1, C_0] = [1, 1, 1]$
Shift register 52 bit (The year function is effective.)

C_3'	C_2'	C_1'	C_0'	FUNCTION	
0	0	0	0	Register Hold	DATA OUT = 1 Hz
0	0	0	1	Register Shift	DATA OUT = [LSB] = 0 or 1
0	0	1	0	Time Set & Counter Hold	DATA OUT = [LSB] = 0 or 1
0	0	1	1	Time Read	DATA OUT = 1 Hz
0	1	0	0	TP = 64 Hz	
0	1	0	1	TP = 256 Hz	
0	1	1	0	TP = 2 048 Hz	
0	1	1	1	TP = 4 096 Hz	
1	0	0	0	TP = 1 s Interrupt set (counter reset & start)	
1	0	0	1	TP = 10 s Interrupt set (counter reset & start)	
1	0	1	0	TP = 30 s Interrupt set (counter reset & start)	
1	0	1	1	TP = 60 s Interrupt set (counter reset & start)	
1	1	0	0	Interrupt Output Flag Reset	
1	1	0	1	Interrupt Timer Clock Run	
1	1	1	0	Interrupt Timer Clock Stop	
1	1	1	1	TEST MODE SET	

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- Command input
  (1) 3-bit binary code input: C_2, C_1, C_0
  (2) 4-bit serial transfer command input: C_3', C_2', C_1', C_0'

- Number of commands

	C_2, C_1, C_0	C'_3, C'_2, C'_1, C'_0
Register control	4	4
TP select	3	8
TP control	0	3
Test mode set	1	1

- Commands (C_3', C_2', C_1', C_0' commands are made effective only when $[C_2, C_1, C_0] = [1, 1, 1]$.)
  (1) Register control $[C_2, C_1, C_0] / [C_3', C_2', C_1', C_0']$
  - **Register Hold Mode** $[0, 0, 0] / [0, 0, 0, 0]$

    $[C_2, C_1, C_0]$
    The 40-bit shift register is held. The year function is ineffective.
    $[C_3', C_2', C_1', C_0']$
    The 48-bit shift register is held.
    The command register is not held.
    * The DATA OUT output frequency is 1 Hz.

  - **Register Shift Mode** $[0, 0, 1] / [0, 0, 0, 1]$

    $[C_2, C_1, C_0]$
    The 40-bit shift register data can be shifted. The year function is ineffective.
    $[C_3', C_2', C_1', C_0']$
    Data in 52-bit shift registers (including command registers) can be shifted. For command register, data can be always shifted using the serial command transfer mode.
    * The DATA OUT output is LSB data from the shift register.

  - **Time Set and Counter Hold Mode** $[0, 1, 0] / [0, 0, 1, 0]$

    $[C_2, C_1, C_0]$
    Data is transferred from the 40-bit shift register to the time counter. The year function is ineffective.
    $[C_3', C_2', C_1', C_0']$
    Data is transferred from the 48-bit shift register to the time counter.
    * This command is used to reset the last 10–15 of 15 Stage Binary Divider and holds the time counter.
      15 Stage Binary Divider resetting and time counter release are executed by the following:
      $[C_2, C_1, C_0] = [0, 0, 0]\ [0, 0, 1]\ [0, 1, 1]\ [C_3', C_2', C_1', C_0'] = [0, 0, 0, 0]\ [0, 0, 0, 1]\ [0, 0, 1, 1]$
      The time setting accuracy is ±15.625 ms.
      The DATA OUT pin outputs LSB data (0 or 1) from the shift register.
      After this command is executed, the 40-/48-bit shift register is held and data cannot be shifted.

  - **Time Read Mode** $[0, 1, 1] / [0, 0, 1, 1]$

    $[C_2, C_1, C_0]$
    Data is transferred from the time-counter to the 40-bit shift register. The year function is ineffective.
    $[C_3', C_2', C_1', C_0']$
    Data is transferred from the time counter to the 48-bit shift register.
    * The DATA OUT pin output is a 1 Hz frequency.
      After this command is executed, the 40-/48-bit shift register is held and data cannot be shifted.

(2) TP selection and control $[C_2, C_1, C_0]/[C_3', C_2', C_1', C_0']$

- **TP = 64 Hz** Set Mode [1, 0, 0]/[0, 1, 0, 0]
  64 Hz (50 % duty) is output to the TP pin.
  $[C_2, C_1, C_0]$: The year function is ineffective and the interrupt timer stops.
- **TP = 256 Hz** Set Mode [1, 0, 1]/[0, 1, 0, 1]
  256 Hz (50 % duty) is output to the TP pin.
  $[C_2, C_1, C_0]$: The year function is ineffective and the interrupt timer stops.
- **TP = 2 048 Hz** Set Mode [1, 1, 0]/[0, 1, 1, 0]
  2 048 Hz (50 % duty) is output to the TP pin.
  $[C_2, C_1, C_0]$: The year function is ineffective and the interrupt timer stops.

Modes permitted only for serial commands $[C_3', C_2', C_1', C_0']$

- **TP = 4 098 Hz** Set Mode [0, 1, 1, 1]
  4 098 Hz (50 % duty) is output to the TP pin. The interrupt timer stops.
- **TP = 1-second** Interrupt Set Mode (counter reset & start) [1, 0, 0, 0]
  A 1-second interrupt signal is output to the TP pin.
- **TP = 10-second** Interrupt Set Mode (counter rest & start) [1, 0, 0, 1]
  A 10-second interrupt signal is output to the TP pin.
- **TP = 30-second** Interrupt Set Mode (counter reset & start) [1, 0, 1, 0]
  A 30-second interrupt signal is output to the TP pin.
- **TP = 60-second** Interrupt Set Mode (counter reset & start) [1, 0, 1, 1]
  A 60-second interrupt signal is output to the TP pin.
- **Interrupt Output Flag Reset** [1, 1, 0, 0]
  The interrupt signal output to the TP pin is reset.
  The interrupt timer counter continue the operation.
- **Interrupt Timer Clock Run** [1, 1, 0, 1]
  The timer for outputting interrupt signals is reset then started.
- **Interrupt Timer Clock Stop** [1, 1, 1, 0]
  The timer for outputting interrupt signals stops.
  The output status does not change.

(3) Serial command transfer mode setting
Set $[C_2, C_1, C_0] = [1, 1, 1]$

(4) Test mode setting
Set $[C_2, C_1, C_0] = [1, 1, 1]$ $[C_3', C_2', C_1', C_0'] = [1, 1, 1, 1]$

- ○ 3-bit parallel command setting mode $[C_2, C_1, C_0]$
  The year function is ineffective when commands are input through C_2, C_1, and C_0 pins.
  Generally, February involves 28 days. The 29th day can be set optionally. The next day of the February 29th can be set the March 1st automatically. The interval timer is in the halt state.
  * The test mode is cancelled by $[C_2, C_1, C_0] = [0, 0, 0]$ to [1, 1, 0].
- ○ Serial command transfer mode $[C_3', C_2', C_1', C_0']$
  If a strobe signal is input with C_2, C_1, and C_0 pins set at the V_{DD} level ([1, 1, 1]), the contents of the serial command register ($[C_3', C_2' C_1', C_0']$ are received as a command; the year function is effective.
  * The test mode is cancelled by $[C_3', C_2', C_1', C_0']$
    $= [0, 0, 0]$
    $= [0, 1, 0, 0]$ to [1, 1, 1, 0]

  In this mode, the serial command register is not held with the Register Hold command. Accordingly, the serial command can be executed irrespective of the mode if the CS pin is active.
  The year function is effective in the serial command transfer mode.

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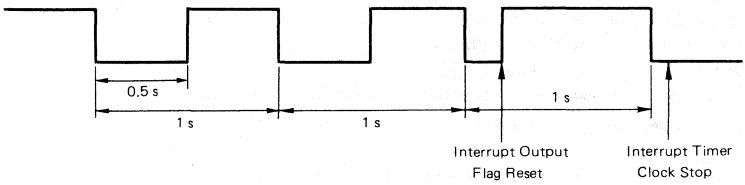
○ Interrupt output function

An interrupt signal can be output by selecting an output from TP.

Interrupt signals are output repeatedly at specified intervals until their output is suppressed by a command.

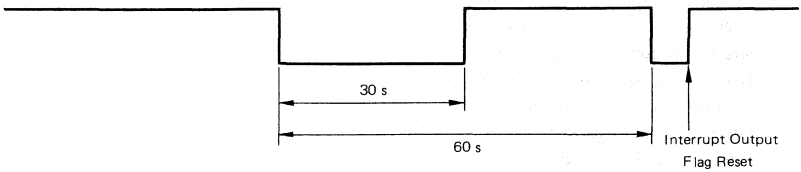
Only output flags can be reset to operate the timer continuously.



Interrupt of 1 second

The interrupt signal waveform is rectangular (50 % duty) if not reset.

The interrupt timer is independent of the Timer Counter, so it is not affected by the resetting of the current time timer.



The interrupt timer accuracy is ±15.625 ms.

* The interrupt timer counter is reset by [1, 0, 0, 0] through [1, 0, 1, 1].

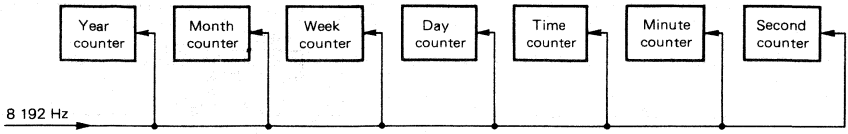
○ Test mode

In the test mode, data is output to the DATA OUT pin regardless of whether data has been input to OUT ENBL.

There are two different test modes depending on the OUT ENBL data.

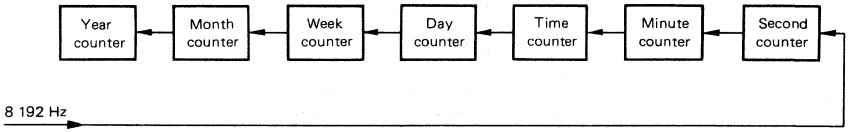
(1) Test mode 1 (OUT ENBL = 0)

8 192 Hz signals are set parallel in the counters for year, month, week, day, time, minute, and second. There is no carry from these counters.



(2) Test mode 2 (OUT ENBL = 1)

A 8 192 Hz signal is input to the second counter instead of the 1 Hz signal. There is carry from counters.



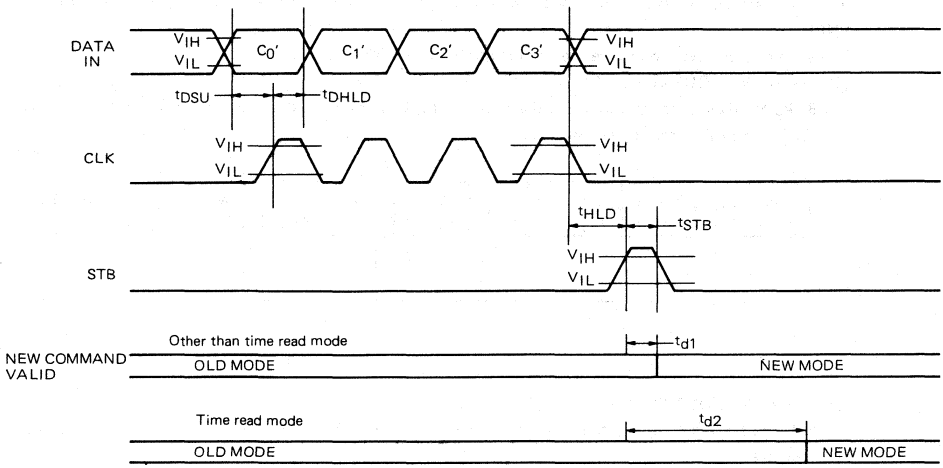
Outputs from DATA OUT and TP OUT pins in different function modes are listed below.

MODE	DATA OUT	TP	Others	
REGISTER HOLD	1 Hz	64 Hz	By this command, TEST MODE is released.	
REGISTER SHIFT	LSB of shift register	32 Hz	Test mode	8 192 Hz input to time counter
TIME SET	LSB of shift register	L Level		
TIME READ	1 Hz	32 Hz		8 192 Hz input to time counter

When the REGISTER HOLD command cancels the test mode, 64 Hz is output to the TP pin.

7

TIMING DIAGRAM FOR SETTING COMMANDS (C_0', C_1', C_2', C_3')



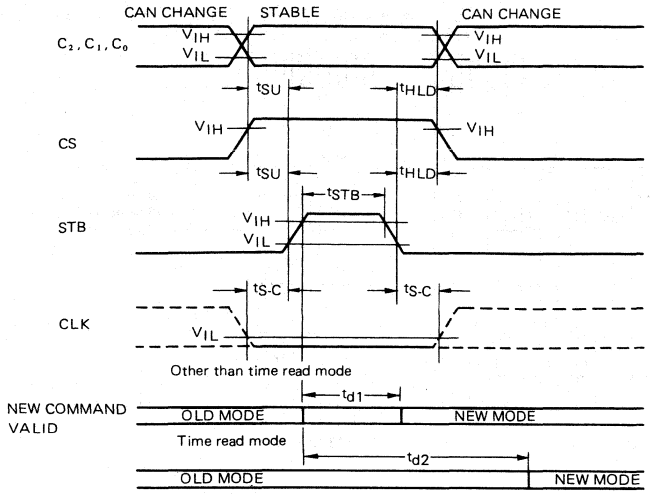
$V_{DD}-V_{SS}$=2.0 V

t_{DSU} = 1 μs MIN.
t_{DHLD} = 1 μs MIN.
t_{HLD} = 1 μs MIN.
t_{STB} = 1 μs MIN.
t_{d1} = 1 μs MAX. (Other than time read mode)
t_{d2} = 20 μs MAX. (Time read mode)

Note: Command (C_2, C_1, C_0) is set to (1, 1, 1)
CS = "H"
A mode is latched by STB and held until another mode in the same group is set.

Fig. 2

TIMING DIAGRAM FOR SETTING COMMANDS (C_0, C_1, C_2)



$V_{DD}-V_{SS}$ = 2.0 V

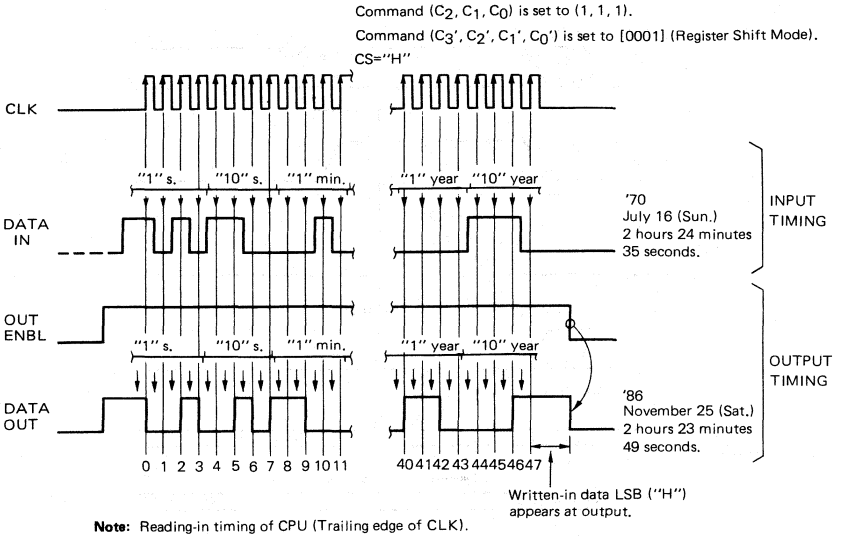
t_{SU}	=	1 μs MIN.
t_{HLD}	=	1 μs MIN.
t_{STB}	=	1 μs MIN.
t_{d1}	=	1 μs MAX. (Other than time read mode)
t_{d2}	=	20 μs MAX. (Time read mode)
t_{S-C}	=	1 μs MIN.

Note: A mode is latched by STB and held until another mode in the same group is set.

Fig. 3

7

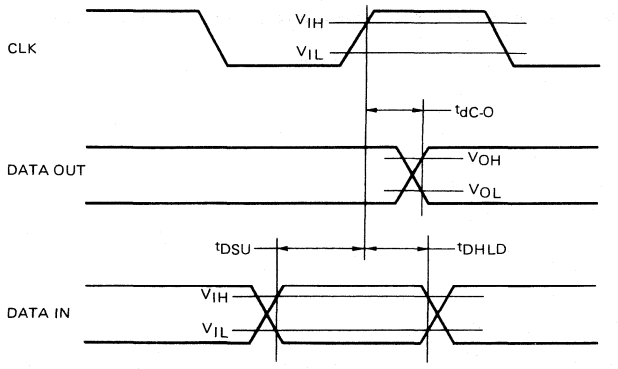
DATA INPUT/OUTPUT TIMING DIAGRAM



Note: Reading-in timing of CPU (Trailing edge of CLK).

Fig. 4

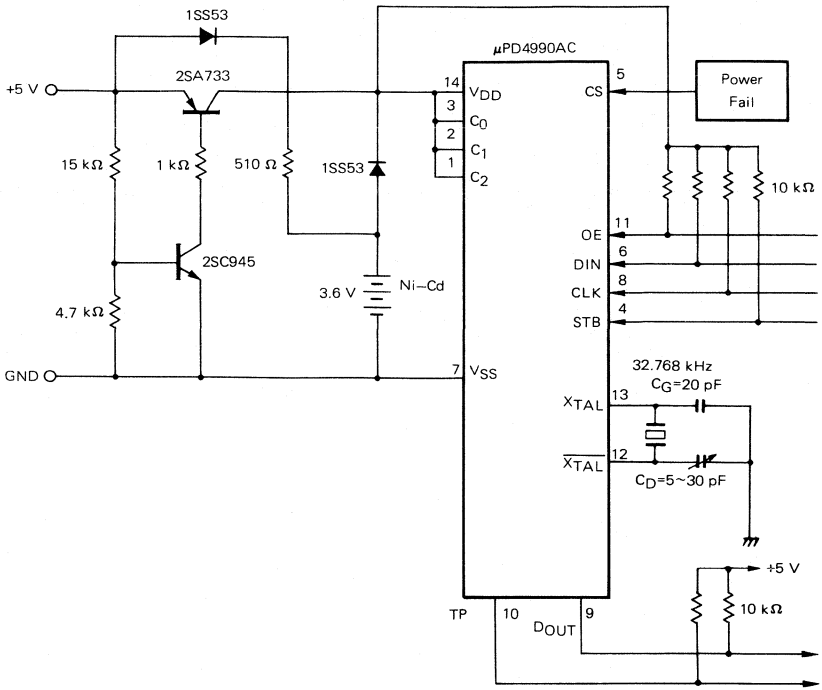
TIMING DIAGRAM OF DATA INPUT AND OUTPUT



t_{dC-O} : 1 μs MAX. (R_L = 33 kΩ, C_L = 25 pF)
t_{DSU} : 1 μs MIN.
t_{DHLD} : 1 μs MIN.

Fig. 5

POWER SUPPLY CIRCUIT



4-BIT PARALLEL I/O REAL TIME CLOCK

DESCRIPTION

The μPD4991A is CMOS integrated circuit designed for microcomputer systems which require real time clock, alarm timer and interval timer functions.

Reference frequency of the μPD4991A is 32.768 kHz.

The μPD4991A incorporates counters for seconds, minutes, hours, days of week, days, months, years, and leap year.

Current consumption of the μPD4991A reduced about 30 percent less than the μPD4991.

FEATURES

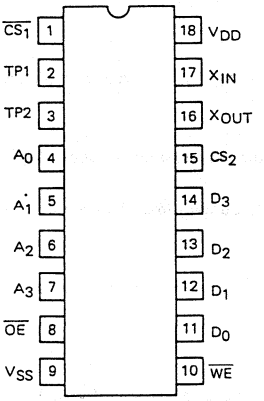
- Counts seconds, minutes, hours, days of week, days, months, years, and leap year
- Automatic leap year compensation
- 12 or 24 hour clock
- BCD data format and 4-bits parallel I/O
- Built-in alarm function (hours, minutes, seconds, months, days, and days of week)
- Selectable interval timer output (either of 0.1, 1.0, 10, 30 or 60 second)
- Selectable alarm output (either of 2048, 1024, 64, 16, 1 Hz or one pulse output, or H to L output)
- μPD4991 upward compatible
- Low current consumption 2 μA typ (V_{DD} = 2.4 V)

ORDERING INFORMATION

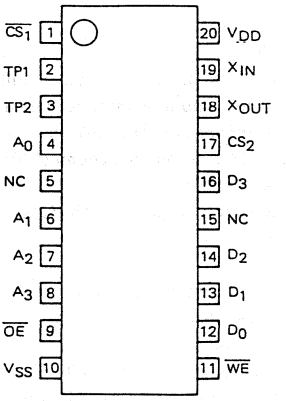
Part Number	Package	Quality Grade
μPD4991ACX	18-pin plastic DIP(300mil)	Standard
μPD4991AGS	18-pin plastic SOP(300mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

CONNECTION DIAGRAM (TOP VIEW)

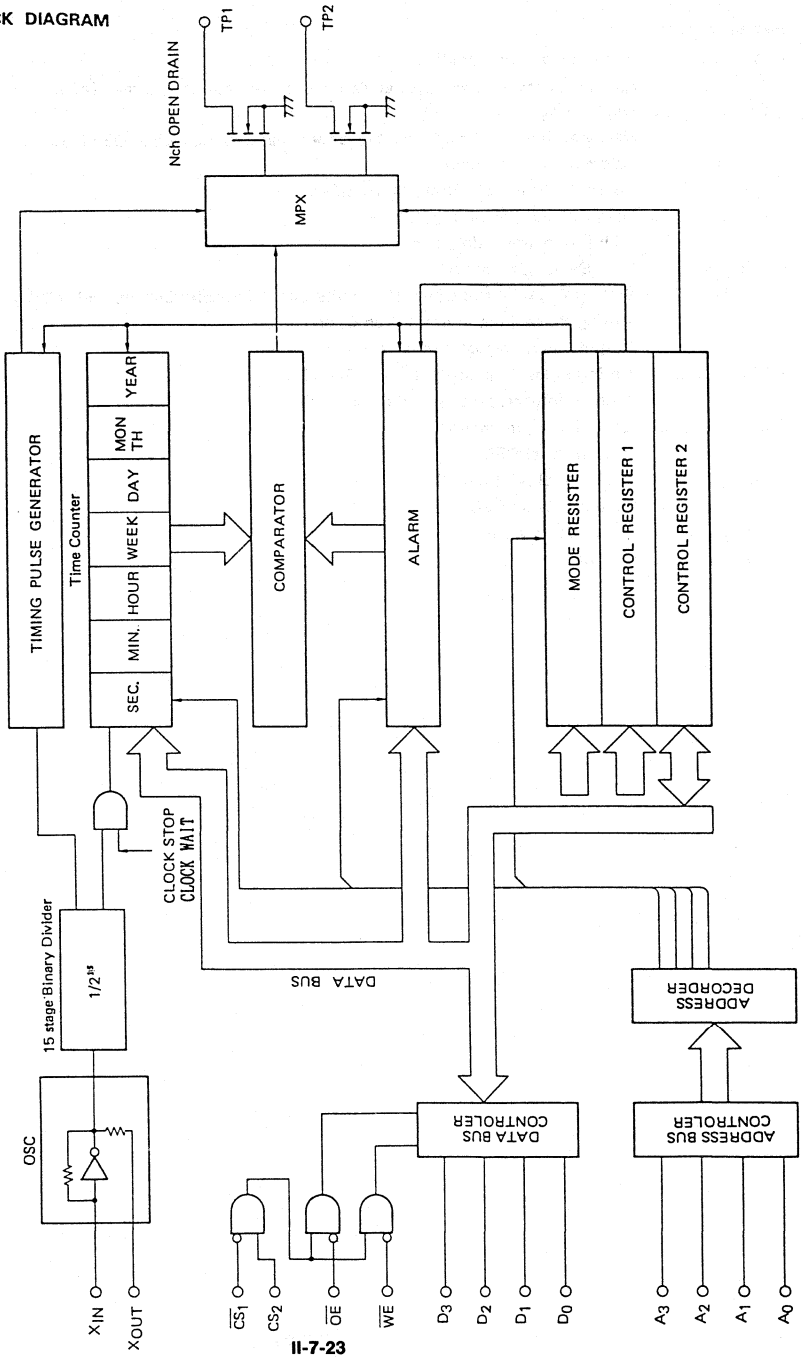


μPD4991ACX



μPD4991AGS

BLOCK DIAGRAM



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PIN FUNCTION

- $\overline{WE}$ ..... Write Enable pin (input)
  When $\overline{WE}$ go low to high, data at data bus is written to internal refister specified by the address.
- $\overline{OE}$ ..... Output Enable pin (input)
  Data specified by the address bus appears at data bus while $\overline{OE}$ is low.
- $A_3 \sim A_0$ ..... Address Bus pin (input)
  Internal address of μPD4991A specified.
- $D_3 \sim D_0$ ..... Data Bus pin (input/output)
  4 bit bidirectional data bus.
- $\overline{CS_1}$, CS_2 ..... Chip Select pin (input)
  Setting $\overline{CS_1}$ = 'L' and CS_2 = 'H' enables data to transfer between μPD4991A and CPU.
- TP_1 ..... Timing Pulse 1 pin (output) (Nch Open Drain)
  Outputs alarm signal or busy signal.
- TP_2 ..... Timing Pulse 2 pin (output) (Nch Open Drain)
  Outputs interval timer signal or busy signal.
- X_{IN} ..... X'tal Signal pin (input)
  Input of X'tal OSC
- X_{OUT} ..... X'tal Signal pin (output)
  Output of X'tal OSC
- V_{DD} ..... Power Supply pin
- V_{SS} ..... Ground pin

ABSOLUTE MAXIMUM RATINS (V_{SS} = 0 V)

Supply Voltage	V_{DD}	−0.3 to 7.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	7.0	V
Low-level output current (Nch Open Drain)	I_{OUT}	30	mA
Operating temperature range	$T_{opt.}$	−40 to +85	°C
Storage temperature range	$T_{stg.}$	−65 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, f = 32.768 kHz, C_G = C_D = 20 pF, C_I = 20 kΩ, T_a = −40 ~ +85 °C)

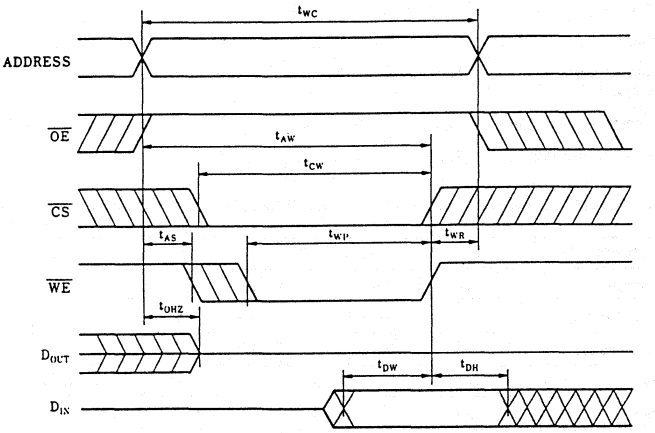
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Operating voltage	V_{DD}	2.0		5.5	V	
High-level input voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	
Low-level input voltage	V_{IL}	V_{SS}		0.3V_{DD}	V	
Supply current	I_{DD1}		5	14	μA	V_{DD}=3.6V, V_{IN}=V_{SS}, T_a=−40 to +70℃
Supply current	I_{DD2}		2	6	μA	V_{DD}=2.4V, V_{IN}=V_{SS}, T_a=−40 to +70℃
High-level input leak current	I_{LIH}			+1.0	μA	V_{DD} = 5.5 V, V_{IN} = V_{DD}
Low-level input leak current	I_{LIL}			−1.0	μA	V_{DD} = 5.5 V, V_{IN} = V_{SS}
High-level output voltage	V_{OH}	2.4			V	I_{OH} = −1.0 mA
Low-level output voltage	V_{OL1}			0.4	V	I_{OL} = 2.0 mA
Low-level output voltage (Nch Open Drain)	V_{OL2}			0.4	V	I_{OL} = 1.0 mA
High-level leak current (Nch Open Drain)	I_{LOH}			1.0	μA	T_{POUT}=V_{DD}

AC CHARACTERISTICS

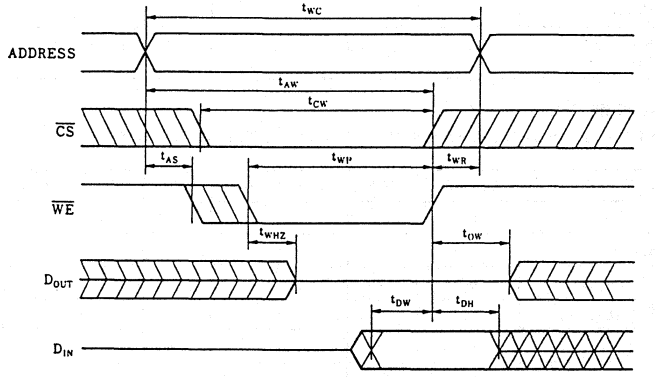
Write Cycle (Unless otherwise specified, V_{DD} = 5 V ±10 %, T_a = −40 ~ +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Cycle time	t_{WC}	150			ns	
$\overline{CS}$-$\overline{WE}$ reset time	t_{CW}	120				
Address-$\overline{WE}$ reset time	t_{AW}	120				
Address-$\overline{WE}$ setup time	t_{AS}	0				
Write pulse width	t_{WP}	90				
Address hold time	t_{WR}	20				
Input data setup time	t_{DW}	0				
Input data hold time	t_{DH}	0				
$\overline{WE}$-output floating time	t_{WHZ}		50			

WRITE CYCLE TIMING 1



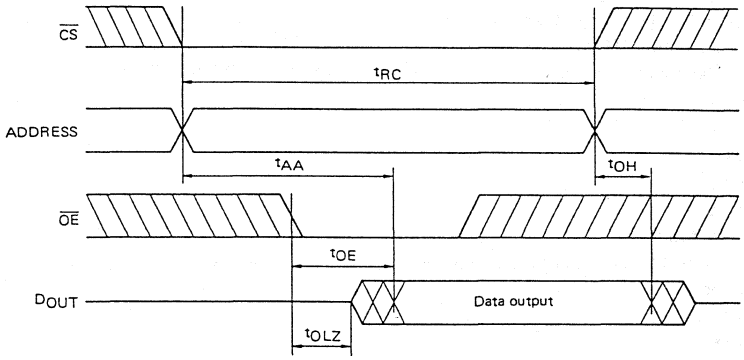
WRITE CYCLE TIMING 2 ($\overline{OE}$ = V_{IL})



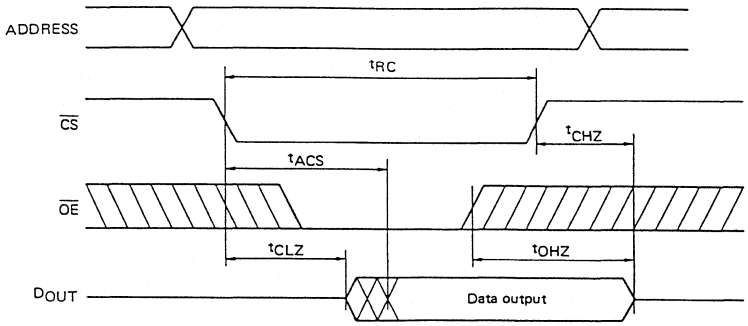
READ CYCLE (Unless otherwise specified, V_{DD} = 5 V ±10 %, T_a = −40 ~ +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150		
$\overline{CS}$-access time	t_{ACS}			150		
$\overline{OE}$-output delay time	t_{OE}			75		
$\overline{OE}$-output delay time	t_{OLZ}	5				
$\overline{OE}$-output delay time	t_{OHZ}			50		
Output hold time	t_{OH}	15				
$\overline{CS}$-output setup time	t_{CLZ}	10				
$\overline{CS}$-output floating time	t_{CHZ}	5				

READ CYCLE TIMING 1



READ CYCLE TIMING 2



FUNCTION SPECIFICATIONS

- Reference frequency (X'tal OSC)..... 32.768 kHz
- Data format ..... BCD format
- Data function

  Counters for clock and calendar are incorporated.

  Leap year and end of month are judged automatically.

  Leap year is judged each 4 years and can be set to the desired year.

  There are two year counters; units of year and tens of year.

  Hour counters are programmable for 12 or 24 hour operation.
- Data Input/Output (D_3, D_2, D_1, D_0)

  Data input/output is 4-bits parallel.

  Data is written to register when $\overline{WE}$ signal go low to high and read from register when $\overline{OE}$ signal is low.

  Data is written to register when $\overline{WE}$ signal is low and read from register when $\overline{OE}$ signal is low.
- Function mode selection

  The function mode is selected by the DATA (D_3, D_2, D_1, D_0) input when ADDRESS = "FH" (A_3, A_2, A_1, A_0 = 1, 1, 1, 1), and set on-going positive edge of $\overline{WE}$ signal.

  The function is selected by ADDRESS input.
- Timing pulse output (TP_1, TP_2)

  TP_1 ..... Alarm signal can be output one of the following signal from this terminal.

  2048 Hz

  1024 Hz

  64Hz

  16 Hz

  1 Hz

  one pulse "H" to "L"

  TP_2 ..... Interval timer signal can be output one of the following signal from this terminal.

  60 sec.

  30 sec.

  10 sec.

  1 sec.

  0.1 sec.
- Chip Select ($\overline{CS_1}$, CS_2)

  All the inputs are disable except for X_{IN} while $\overline{CS_1}$ = "H" or CS_2 = "L" (non-select).

  All the inputs are enable while $\overline{CS_1}$ = "L" and CS_2 = "H".

OUTLINE OF FUNCTION

- μPD4991A has three modes.

① BASIC TIME MODE

Can write and read data between timer counter and CPU, and Specify command of control register 1 and 2(see NOTE).

② ALARM SET AND TP_1 CONTROL MODE

Can set data to alarm register;
Set TP_1 function:
Judge leap year; and
Specify command of conrtol register 1 and 2(see NOTE).

③ ALARM SET AND TP_2 CONTROL MODE

Can set data to alarm register;
Set TP_2 function;
Change 12 or 24 hours operation;
Set leap year or not; and
Specify command of conrtol register 1 and 2(see NOTE).

NOTE Control register 1 and 2 are common to all the modes.

Each mode can be selected according to the DATA contents when ADDRESS = "F_H". Once this device is set in a mode, it retains this mode until another mode is set. For mode selection see Table 1 "Mode Data Correspondence Table."

Table 1 Mode Data Correspondence Table

ADDRESS = (1, 1, 1, 1)

DATA MSB			LSB	FUNCTION MODE
0	*	0	0	BASIC TIMER MODE
0	*	0	1	ALARM SET & TP_1 CONTROL MODE
0	*	1	0	ALARM SET & TP_2 CONTROL MODE
0	*	1	1	BASIC TIME MODE
1	*	*	*	Disable (Reserved mode)

*:The setting of the corresponding bit is ignored.

NOTE In mode (0, *, 0, 0), stages 10 through 15 can be reset during execution of the frequency divider stage command (±30 sec. ADJUST, RESET); in mode (0, *, 1, 1), all the stages can be reset.
Other commands are common to the both modes.

MODE EXPLANATION

1. BASIC TIME MODE (MODE = 0 * 0 0 B)

- Built in 13 counters; tens of year, units of year, tens of month, units of month, tens of day, units of day, days of week, tens of hour, units of hour, tens of minute, units of minute, tens of second and units of second digits.
- Day of week code ranges from 00H to 06H.
- If the leap year judgement result is invalid, the last day of February is February 28th.

The ADDRESS corresponding to each digit is shown in Table 2.
Control register 1 and 2 are common to all the modes. The functions corresponding to each data is shown in Table 3 and 4. For other mode, be sure to see these tables.

Table 2 ADDRESS Table–1

BASIC TIME MODE (MODE = 0, *, 0, 0)

ADDRESS MSB			LSB	FUNCTION MODE	
0	0	0	0	Units second digit	R/W
0	0	0	1	Tens second digit	R/W
0	0	1	0	Units minute digit	R/W
0	0	1	1	Tens minute digit	R/W
0	1	0	0	Units hour digit	R/W
0	1	0	1	Tens hour digit	R/W
0	1	1	0	Days of week digit	R/W
0	1	1	1	Units day digit	R/W
1	0	0	0	Tens day digit	R/W
1	0	0	1	Units month digit	R/W
1	0	1	0	Tens month digit	R/W
1	0	1	1	Units year digit	R/W
1	1	0	0	Tens year digit	R/W
1	1	0	1	CONTROL REGISTER 1	W/O
1	1	1	0	CONTROL REGISTER 2	R/W
1	1	1	1	MODE REGISTER	W/O

R/W: READ AND WRITE
W/O: WRITE ONLY

NOTE If the 12-hour system is selected, the second high-order bit of the tens hour digit data is the AM/PM flag (AM = 0/PM = 1).

Table 3 DATA Table-1

CONTROL REGISTER 1 (TIME COUNTER CONTROL)
ADDRESS = (1, 1, 0, 1)

		D3	D2	D1	D0
W/O	0	NOP	RUN	NOP	NOP
	1	CLOCK WAIT Note 4	CLOCK STOP Note 3	ADJUST (+/−)30 s Note 1	RESET Note 2

NOTE 1 ADJUST (+/−)30 s
Second digits 00 to 29 → 00 (second)
30 to 59 → 00 (second) +1 (minute)
BUSY flag is set until shift operation completes.
In MODE (0, *, 0, 0), stages 10 to 15 of the 15-stage frequency divider circuit are reset
In MODE (0, *, 1, 1), all the stages of the 15-stage frequency divider circuit are reset.

NOTE 2 RESET
In MODE (0, *, 0, 0), stages 10 to 15 of the 15-stage frequency divider circuit are reset.
In MODE (0, *, 1, 1), all the stages of the 15-stage frequency divider circuit are reset.

NOTE 3 CLOCK STOP
To set the time, stop the internal clock after clock reset while data is set into the time counters, or otherwise incorrect data will be set.

NOTE 4 CLOCK WAIT
When 1 is written in this bit, the clock stops. Delay to the real time does not result in if CLOCK RUN is executed within 0.5 second (it is used at the time read out).

Table 4 DATA Table-2

CONTROL REGISTER 2 (TP_1/TP_2 CONTROL)
ADDRESS = (1, 1, 1, 0)

	D3	D2	D1	D0
W/O	0 (TP_1)	Alarm Function	Alarm matching flag	Output Enable
		0 : ENABLE	0 : RESET	0 : ENABLE
		1 : DISABLE	1 : SET	0 : DISABLE
	1 (TP_2)	Interval clock	Interval counter	Output Enable
		0 : RUN	0 : NOP	0 : ENABLE
		1 : CLK STOP	1 : REST	1 : DISABLE
R/O	*	BUSY flag	Alarm flag	Interval flag
		0 : OFF	0 : OFF	0 : OFF
		1 : ON	1 : ON	1 : ON

* : Don't Care

R/O: READ ONLY
W/O: WRITE ONLY

2. ALARM SET & TP_1 CONTROL MODE (MODE = 0 * 0 1)
ALARM SET & TP_2 CONTROL MODE (MODE = 0 * 1 0)

(1) Setting of data in alarm register

The alarm register consists of a total of 44 bits; 4 bits are assigned to each of 11 counters: tens month, units month, tens day, units day, day of week, tens hour, units hour, tens minute, units minute, tens second, and units second counters.

- Alarm register operation

When an alarm register digit is set to "F_H", this digit is regarded as alarm regardless of the time counter data.

When all the alarm register digits are set to "F_H", they are regarded as alarm regardless of the time counter data.

The ADDRESS corresponding to each digit is shown in Table 5 "ADDRESS Table-2."

FUNCTION CONTROL of TP_1/TP_2 is shown in Table 6 and 7 "DATA Table-3 and -4."

ex.1 Alarm is generated for one second when 54 minutes 32 seconds have elapsed every hour.

Digit	tens month	units month	tens day	units day	Day of week	tens hour	units hour	tens minute	units minute	tens second	units second
Code	F_H	F_H	F_H	F_H	F_H	F_H	F_H	5_H	4_H	3_H	2_H

ex. 2 Alarm is generated for 10 to 19 minutes every hour.

Digit	tens month	units month	tens day	units day	Day of week	tens hour	units hour	tens minute	units minute	tens second	units second
Code	F_H	F_H	F_H	F_H	F_H	F_H	F_H	1_H	F_H	F_H	F_H

Table 5 ADDRESS Table–2

ALARM SET & TP_1 CONTROL MODE (MODE = 0, *, 0, 1)
ALARM SET & TP_2 CONTROL MODE (MODE = 0, *, 1, 0)

ADDRESS MSB			LSB	FUNCTION MODE	
0	0	0	0	Units second digit	R/W
0	0	0	1	Tens second digit	R/W
0	0	1	0	Units minute digit	R/W
0	0	1	1	Tens minute digit	R/W
0	1	0	0	Units hour digit	R/W
0	1	0	1	Tens hour digit	R/W
0	1	1	0	Days of week digit	R/W
0	1	1	1	Units day digit	R/W
1	0	0	0	Tens day digit	R/W
1	0	0	1	Units month digit	R/W
1	0	1	0	Tens month digit	R/W
1	0	1	1	TP_1/TP_2 FUNCTION CONTROL Note 1	W/O
1	1	0	0	Leap year/12.24 HOUR SELECT Note 2	R/W
1	1	0	1	CONTROL REGISTER 1	W/O
1	1	1	0	CONTROL REGISTER 2	R/W
1	1	1	1	MODE REGISTER	W/O

*: The setting of the corresponding bit is ignored.

R/W: READ AND WRITE
W/O: WRITE ONLY

NOTE 1 TP_1 FUNCTION CONTROL is performed in MODE (0, *, 0, 1).
TP_2 FUNCTION CONTROL is performed in MODE (0, *, 1, 0).
NOTE 2 The leap year counter is performed in MODE (0, *, 0, 1).
12/24 HOUR SELECT is performed in MODE (0, *, 1, 0).

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Table 6 DATA Table–3

TP_1 FUNCTION CONTROL
(MODE = 0, *, 0, 1 ADDRESS = 1, 0, 1, 1)

DATA MSB			LSB	FUNCTION MODE	
*	0	0	0	2048 Hz	W/O
*	0	0	1	1024 Hz	W/O
*	0	1	0	64 Hz	W/O
*	0	1	1	16 Hz	W/O
*	1	0	0	1 Hz	W/O
*	1	0	1	1 PULSE output	W/O
*	1	1	0	"H" → "L"	W/O
*	1	1	1	BUSY Signal	W/O
0	*	*	*	Alarm matching flag AUTO RESET	W/O
1	*	*	*	Alarm matching flag AUTO RESET not available	W/O

W/O: WRITE ONLY *: Don't Care.

Table 7 DATA Table–4

TP_2 FUNCTION CONTROL
(MODE = 0, *, 1, 0 ADDRESS = 1, 0, 1, 1)

DATA MSB			LSB	FUNCTION MODE	
*	0	0	0	0.1 sec. interval	W/O
*	0	0	1	1 sec. interval	W/O
*	0	1	0	10 sec. interval	W/O
*	0	1	1	30 sec. interval	W/O
*	1	0	0	60 sec. interval	W/O
*	1	1	1	BUSY Signal	W/O
0	*	*	*	REPEAT	W/O
1	*	*	*	1 SHOT	W/O

W/O: WRITE ONLY *: Don't Care.

(2) 12/24 hour selection

In the 12-hour operation, the 2 high-order bits of the 10-hour counter is used as the AM/PM flag.

AM = 0 0 * *

PM = 0 1 * *

Note Be sure to set the 12/24-hour selector before setting hour's data. Setting it after setting hour's data causes the time counter data to be destroyed.

12/24-hour selection is shown in Table 8 "DATA Table-5."

Table 8 DATA Table-5

Leap year and 12/24-hour selection

(MODE = 0, *, 1, 0 ADDRESS = 1, 1, 0, 0)

	D3	D2	D1	D0
R/W	1 : 24 hours 0 : 12 hours	Leap year Judge 0 : Enable 1 : Disable	*	*

* : Don't Care

ex.1 In the 12-hour system

	Tens-hour digit	Units hour digit	Hexadecimal
8:00 AM →	0 0 0 0	1 0 0 0	0 8 H
8:00 PM →	0 1 0 0	1 0 0 0	4 8 H
12:00 AM →	0 0 0 1	0 0 1 0	1 2 H
12:00 PM →	0 1 0 1	0 0 1 0	5 2 H

Note to 12-hour system operation:

To set 12:00 AM, write the data in order of lower to higher digit (write "2" to units digit and then "1" to tens digit). If "1" and "2" are written in order of higher to lower digit, 12:00 PM may be set.

(3) Leap year counter setting

The leap year counter is set automatically with writing of the year digit.

Based on the year of grace, a multiple of four will be a leap year.

User is able to set leap year counter too.

NOTE Be sure to set leap year counter after setting year's data. To set it before setting year's data, the leap year counter is set automatically.

When the leap year counter value is "* * 0 0 B," it is regarded as a leap year.

The leap year counter can be set regardless of the year value. This counter can be incremented synrhronizing with the units year counter.

Leap year judgment is shown in Table 9 "DATA Table-6."

Table 9 DATA Table–6

Leap year counter
(MODE = 0, *, 1, 0 ADDRESS = 1, 1, 0, 0)

	D3	D2	D1	D0
R/W	*	*	Leap year counter (Leap year = 0, 0)	

R/W:Read and Write

* : Don't Care

ex.

	Tens hour digit	units hour digit	Leap year counter	
	0 0 1 0	0 1 0 1	* * * *	
Write "3" to tens year digit	0 0 1 1	0 1 0 1	* * 1 1	Increment
Write "6" to units year digit	0 0 1 1	0 1 1 0	* * 0 0	1936 is a leap year → leap year counter is 00H
Write "4" to tens year digit	0 1 0 0	0 1 1 0	* * 1 0	
Write "**00B" to leap year counter	0 1 0 0	0 1 1 0	* * 0 0	1946 is not a leap year → leap year counter is not 00H

3. TIMING PULSES

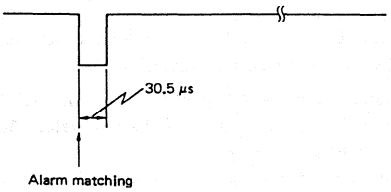
° TP_1

The output from the TP_1 terminal is the alarm signal. One of 2048 Hz, 1024 Hz, 64 Hz, 16 Hz, 1 Hz, 1 pulse output, and "H"–to–"L" is selected as the output waveform according to the contents of TP_1 CONTROL REGISTER.

• 1 pulse output

1 pulse is output when the alarm register's contents match with the time counter's contents.

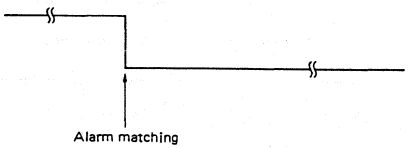
Fig. 1 1 Pulse Output Waveform



• "H"–to–"L" Output

The TP_1 output is changed from "H" to "L" when the alarm register's contents match with the time counter's contents.

Fig. 2 "H"–to–"L" Output Waveform



° Alarm flag, AUTO RESET

This signal continues to be output until the alarm register's contents unmatch with the time counter's contents after it starts being output to the TP_1 terminal when they match.

Fig. 3 TP_1 Output Waveform (AUTO RESET)

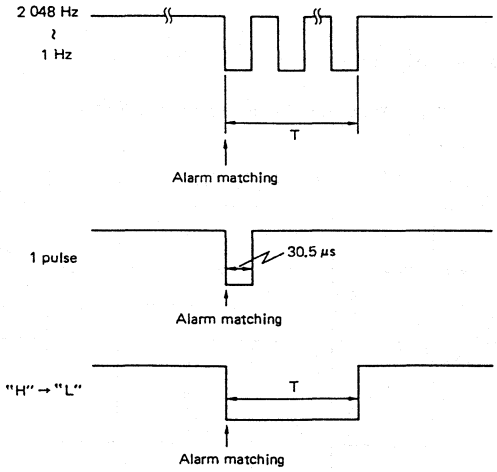


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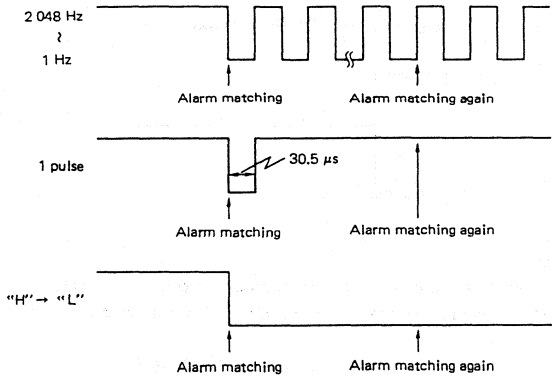
Fig. 4 TP_1 Output Waveform (without AUTO RESET)



The application examples using TP_1 are shown in Figures 5 and 6.

Fig. 5 TP_1 Output Status (AUTO RESET Mode)

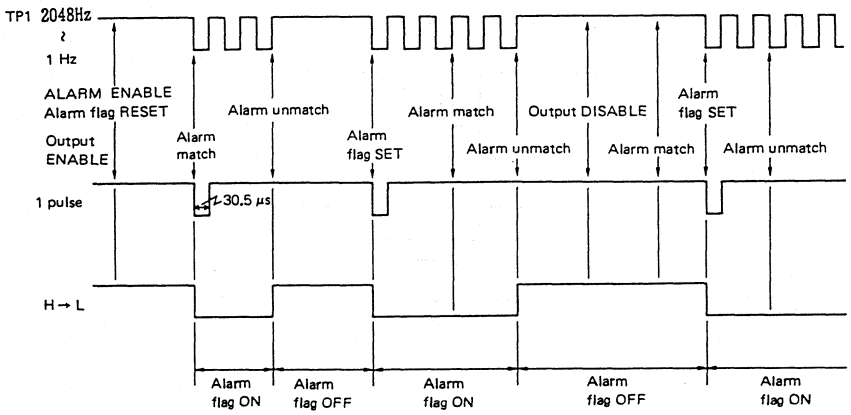
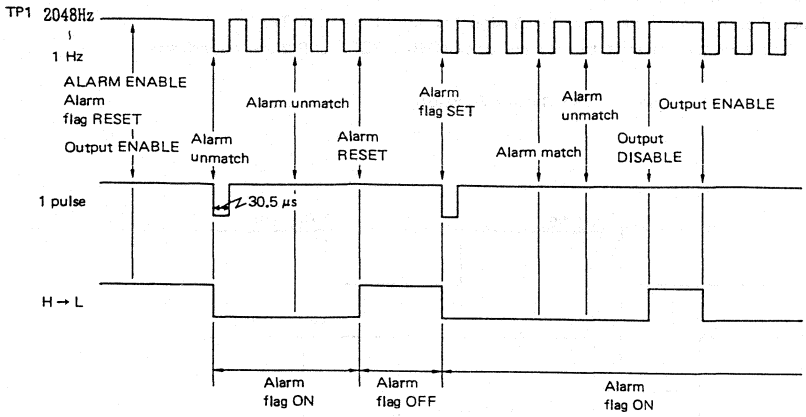


Fig. 6 TP_1 Output Status (without AUTO RESET)

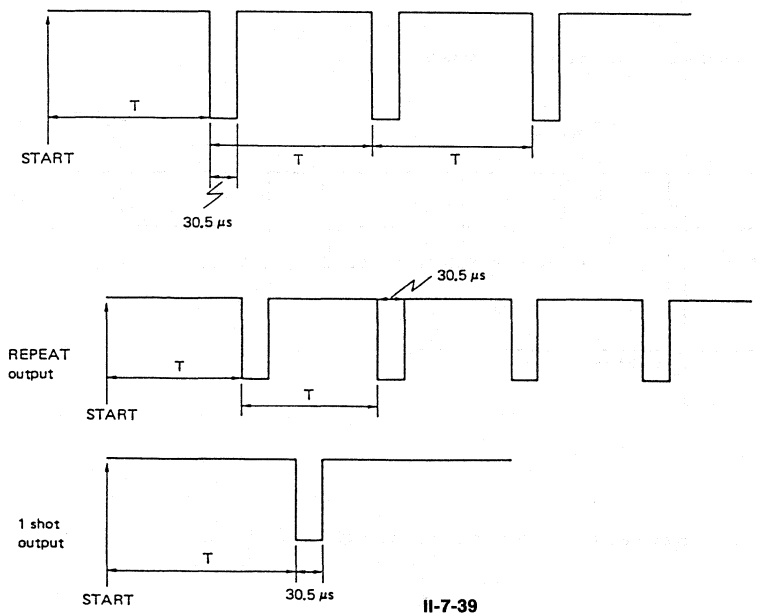


- TP_2 SET (MODE = 0 * 1 1 B)

The output from the TP_2 terminal will be the interval timer signal. This signal is output in a specific cycle. As the output cycle, one of 0.1, 1, 10, 30, or 60 seconds can be selected according to the contents of TP_2 CONTROL REGISTER.

Interval timer of 0.1 second is not just 0.1 second but just 0.5 second at 5 cycle.
The error of cycle is caused to use ±30 second ADJUST or RESET in MODE(0,*,1,1).

Fig. 7 TP_2 Output Waveform



- BUSY output

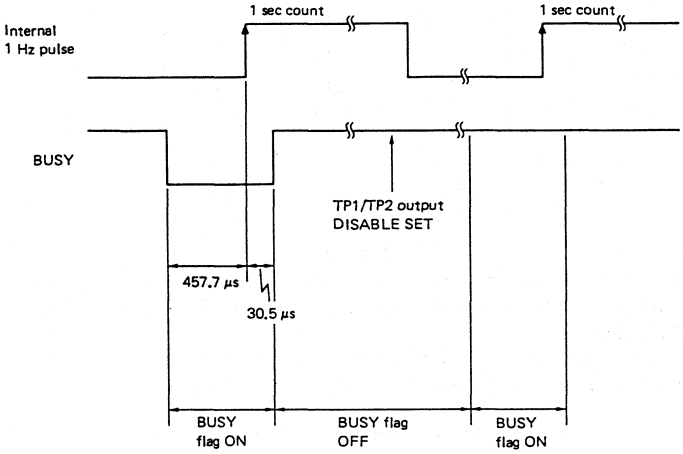
  BUSY signal can be output to TP_1/TP_2.

  When BUSY signal output is selected, only BUSY signal is output to TP_1 or TP_2.

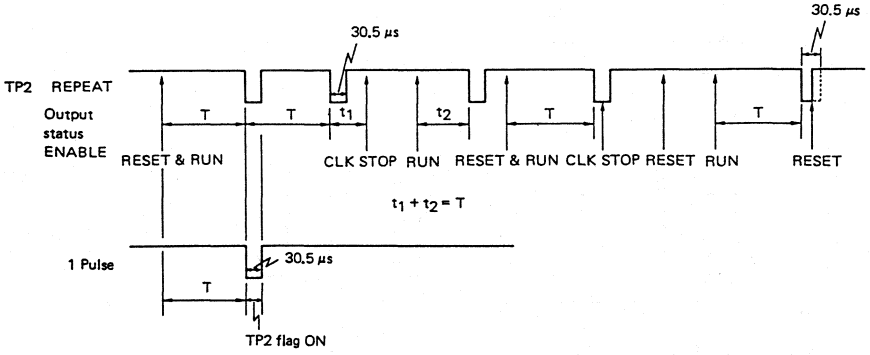
  At selection of BUSY signal, however, the contens of CONTROL REGISTER 2 are not affected.

Fig. 8 BUSY Output Waveform

Busy signal



The application example using TP_2 is shown in Figure 9.



Note: The output is "H" regardless of the TP_2 status when the output status DISABLE is set.

° Oscillation characteristics

When the crystal with the crystal impedance of nearly 20 kΩ is used for the circuit shown in Figure 10 to vary the ambient temperature (T_a) and supply voltage (V_{DD}), the frequency stability is shown in Figures 11 and 12.

The frequency stability in these figures are performed by the following expressions:

$$\text{Stability} = \frac{f - f_{\text{reference value}}}{f_{\text{reference value}}} \times 10^6 \text{ (ppm)}$$

Note In Figure 11, the reference value f is 2048 Hz.
In Figure 12, the reference value f is the frequency measured when V_{DD} = 3.5 V.

Fig. 10 Oscillation Characteristics Measurement Circuit

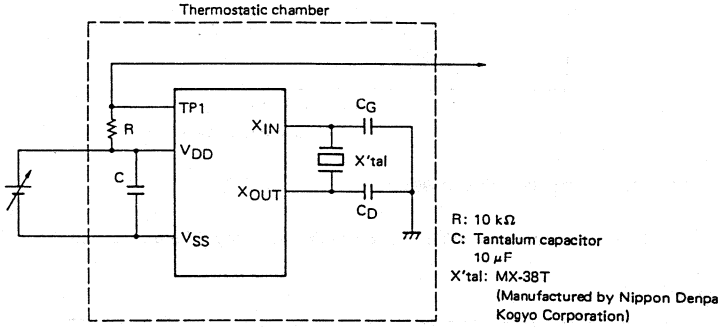


Fig. 11 Frequency Stability vs Temperature Characteristics

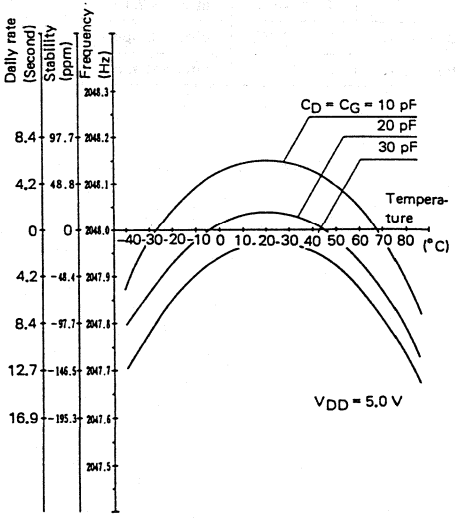


Fig. 12 Frequency Stability vs Supply Voltage

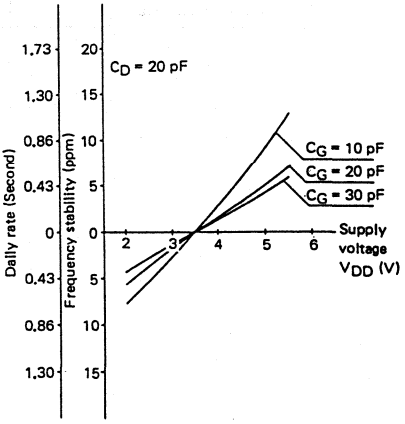
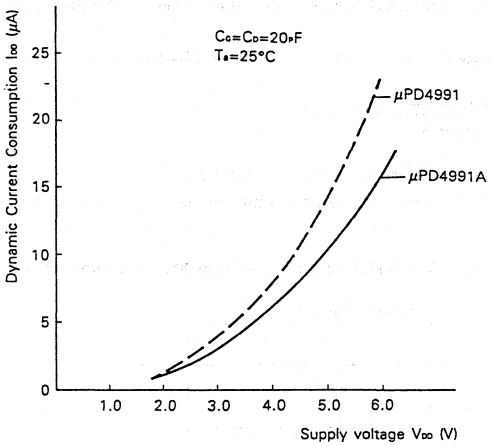


Fig. 13 Dynamic Current Consumption Characteristics



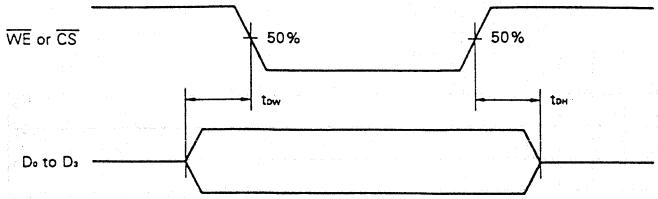
DIFFERENCES BETWEEN μPD4991 AND μPD4991A

The μPD4991A is an improved version of μPD4991 and has the following differences from the μPD4991:

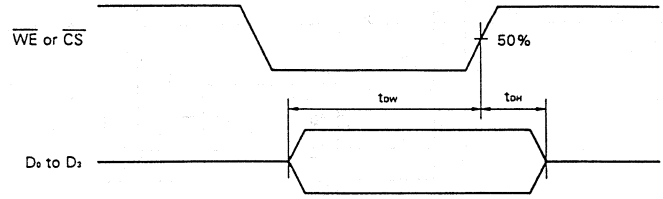
1. Specifications

CHARACTERISTIC	SYMBOL	μPD4991	μPD4991A	NOTE
Current consumption	I_{DD}	20 μA MAX.	14 μA MAX.	at V_{DD} = 3.6 V
Current consumption	I_{DD}	15 μA MAX.	–	at V_{DD} = 3.0 V
Current consumption	I_{DD}	–	4 μA MAX.	at V_{DD} = 2.4 V
Input data setup time	t_{DW}	0 ns MIN.	50 ns MIN.	different specs.
Input data hold time	t_{DH}	0 ns MIN.	0 ns MIN.	different specs.

AC Timing Specification for μPD4991



AC Timing Specification for μPD4991A



2. Functions

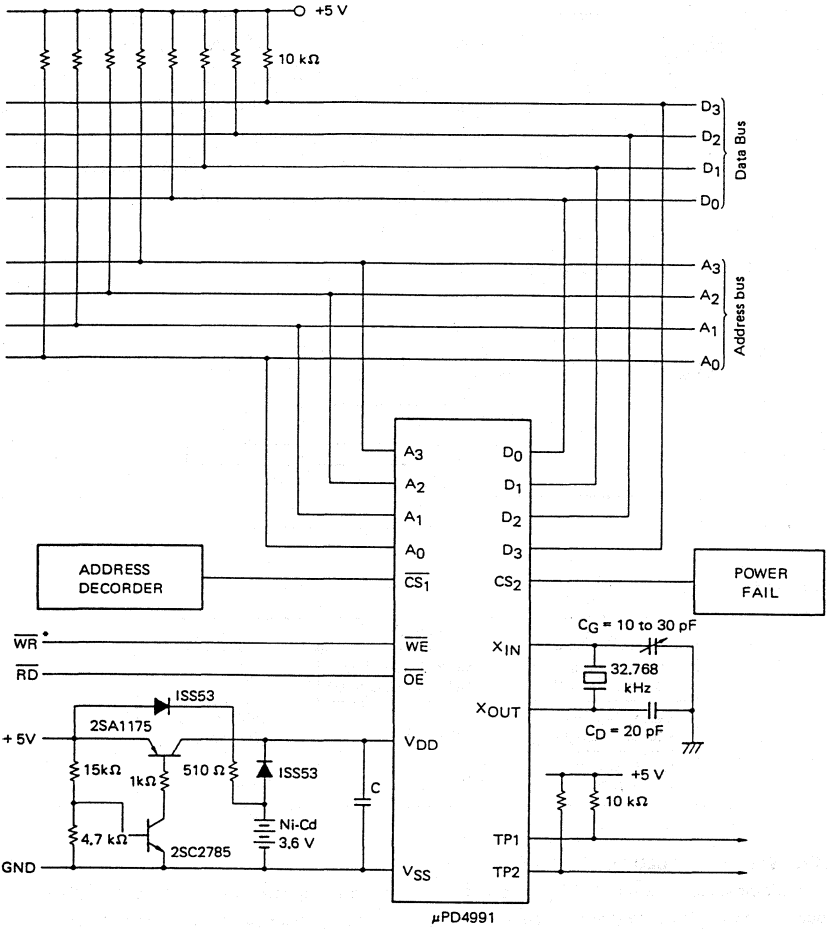
Item	μPD4991	μPD4991A
Effective range of ±30 sec. ADJUST	1 sec. to 1 min. digit (not shift to tens digit)	all digits
BUSY flag when ±30 sec. ADJUST	not to be BUSY	BUSY until all digits shifted
D3-bit of CONTROL REGISTER 1	NOP	CLOCK WAIT

CLOCK WAIT bit and CLOCK STOP bit

Each bit disables the input CLOCK (1 Hz) to the clock counter and stops the clock count. CLOCK STOP bit is used when time is set to the clock counter. Stop always the clock counter when time is set.

CLOCK WAIT bit is used to make sure that the CPU shall not read incorrect data due to the counts occurred during time reading. To read the time, there are some ways which use BUSY signal without using CLOCK WAIT or which read out the time two times. In both CLOCK STOP and CLOCK WAIT, no delay occurs to the real time if CLOCK RUN is executed within 0.5 second.

APPLICATION CIRCUIT EXAMPLE



C: Ceramic capacitor or tantalum capacitor
(Approximately ranging from 0.1 μF to 10 μF)

The application circuits and the circuit constants described in this document are shown as examples and shall not be applied to the mass production design.

Mobile radio ICs - amplifier

Section 8 - Mobile radio ICs - amplifier

Mobile radio ICs - amplifier

Product number	Function	Pins/Package
μPC1428HA	Low noise dual preamplifier	8/SIP
μPC1237HA	Protector IC for stereo power amplifier	8/SIP
μPC1207H	30-50W power amplifier driver	12/SIP
μPC1298V	50-80W power amplifier driver	14/V-DIP
μPD1342V	50-110W power amplifier driver	14/V-DIP
μPC2500H	45W power amplifier	12/SIP
μPC1308V	18W power amplifier	14/V-DIP
μPC1310V	7W dual power amplifier	14/V-DIP
μPC1313HA	Low noise dual preamplifier with automatic level control	9/SIP
μPC1316C	Dual 1.2W power amplifier	14/DIP
μPC1318AV	23W power amplifier	14/V-DIP
μPC1335V	Dual 20W power amplifier	14/V-DIP

LOW NOISE DUAL PREAMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1228HA, a silicon monolithic integrated circuit, is a low noise dual preamplifier designed for car stereo applications. The device consists of two separate amplification channels, and its major features are low noise, low distortion, high gain, large dynamic range and wide supply voltage range.

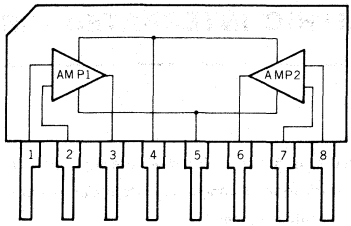
Outline is a 8-lead single in-line plastic package, for small mounting space and easy mounting on P. C. Board.

FEATURES

- Very low seated height : 5.72 mm MAX.
- High open loop gain : A_{VO} = 100 dB TYP.
- Low noise : V_{nin} = 1.1 μV TYP.
- Low distortion : T.H.D. = 0.05 % TYP.
- Large dynamic range : V_{OM} = 2.0 V TYP.
- Wide supply voltage range : V_{CC} = 6 to 16 V
- High output current : I_{ODC} = 1 mA MAX.
- Low impedance load driving capability : R_L = 1 kΩ MIN.
- Small feedback capacitance capability

8

CONNECTION DIAGRAM



Pin No.	Electrical connection
1	Input 1
2	Negative feed back 1
3	Output 1
4	Power supply: $+V_{CC}$
5	Ground
6	Output 2
7	Negative feed back 2
8	Input 2

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC}	18	V
Package Dissipation	P_D	270*	mW
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
		* T_a=75 °C	

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

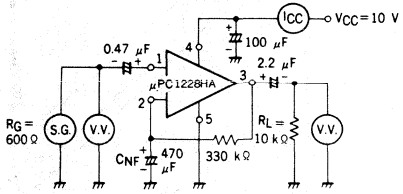
Operating Supply Voltage	V_{CC}	13.2	V
Supply Voltage Range	V_{CC}	6 to 16	V
Operating Ambient Tamperature	T_a	−30 to +75	°C
Load impedance	R_L	10	kΩ

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 10 V, f = 1 kHz, R_L = 10 kΩ)

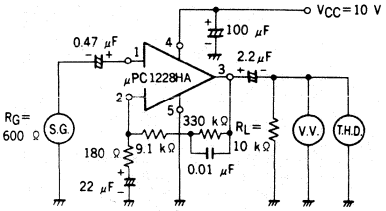
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Quiescent Current	I_{CC}	2.5	3.3	4.8	mA	(1)	V_{in} = 0
Open Loop Voltage Gain	A_{vo}	90	100		dB	(1)	V_O = 0.3 V, f = 100 Hz
Voltage Gain	A_v		40		dB	(2)	V_O = 0.3 V, NAB
Maximum Output Voltage	V_{OM}	1.0	2.0		V	(2)	T.H.D. = 1 %, NAB
Total Harmonic Distortion	T.H.D.		0.05	0.3	%	(2)	V_O = 0.3 V, NAB
Input Impedance	R_i	50	100		kΩ	(2)	
Equivalent Input Noise Voltage	V_{nin}		1.1	1.7	μV	(3)	R_G = 2.2 kΩ, NAB
Cross Talk	CT	−50	−65		dB	(4)	V_O = 1 V, (The other channel V_{in} = 0, R_G = 2.2 kΩ)
Channel Balance	Ch. B	−0.3	0	+0.3	dB	(4)	V_O = 0.3 V

TEST CIRCUITS

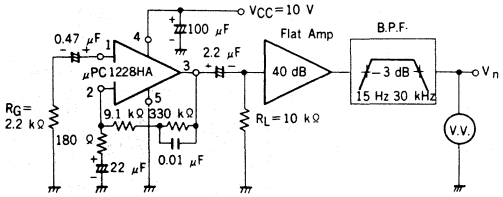
(1) I_{CC}, A_{vo} test circuit



(2) A_v, V_{OM}, T.H.D., Z_{in} test circuit (for Ch. 1)

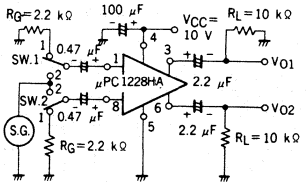


(3) V_{nin} test circuit (for Ch. 1)



NOTE: V_{nin} is calculated by V_n and amp. gain (A_v+40 dB).

(4) Cross talk, Channel balance test circuit

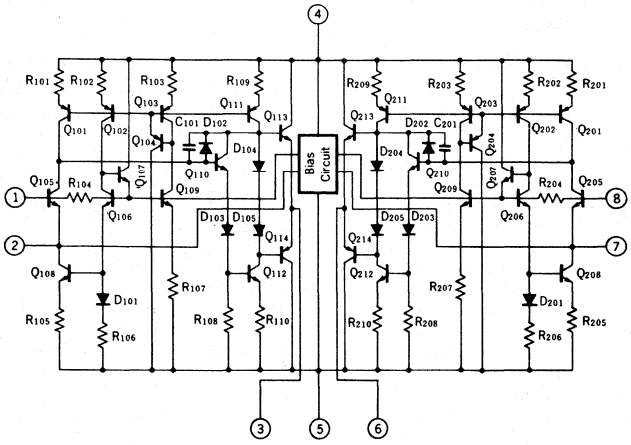


NOTE 1: External components of the IC are the same as the test circuit (2).

2: Cross talk procedure
Switch position SW.1 → 2, SW.2 → 1, 20 log V_{O2}/V_{O1}
Switch position SW.1 → 1, SW.2 → 2, 20log V_{O1}/V_{O2}

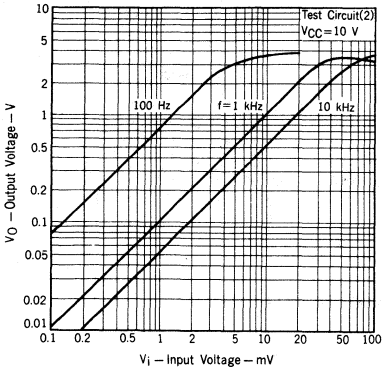
3: Channel balance
Switch position SW.1 → 2, SW.2 → 2, 20 log V_{O1}/V_{O2}

EQUIVALENT CIRCUIT

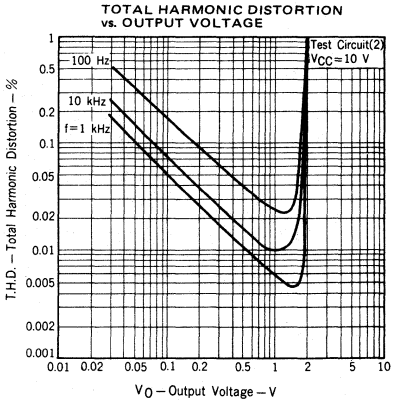


TYPICAL CHARACTERISTICS (T_a = 25 °C)

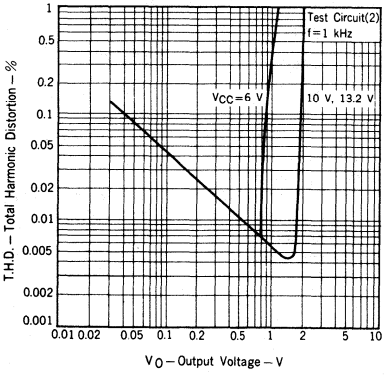
OUTPUT VOLTAGE vs. INPUT VOLTAGE



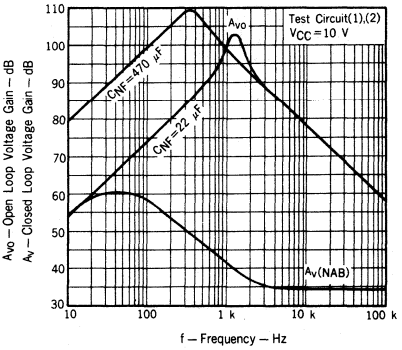
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



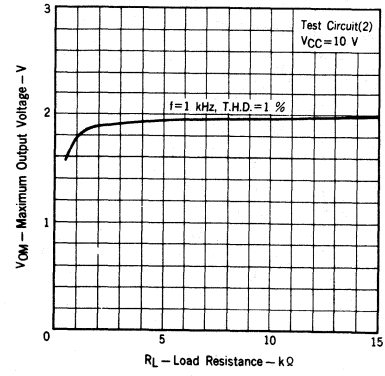
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



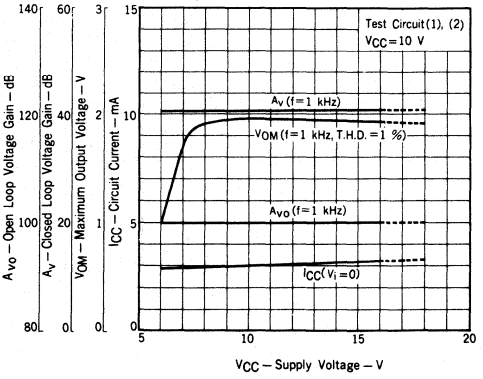
VOLTAGE GAIN vs. FREQUENCY



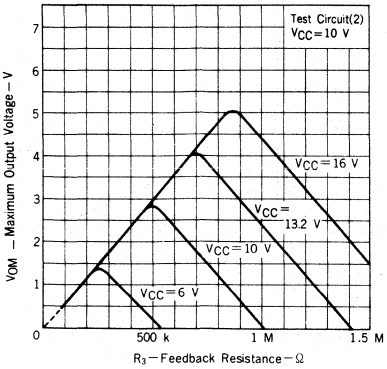
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE



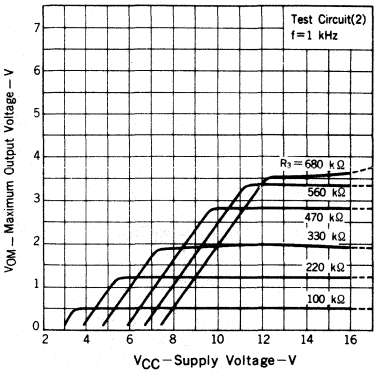
CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs. SUPPLY VOLTAGE



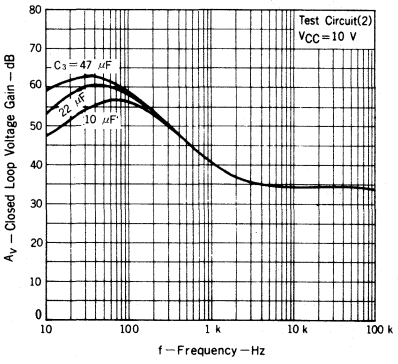
MAXIMUM OUTPUT VOLTAGE vs. FEEDBACK RESISTANCE



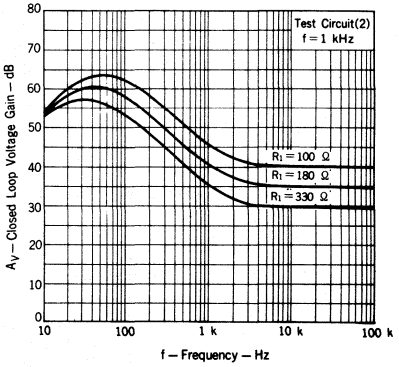
MAXIMUM OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



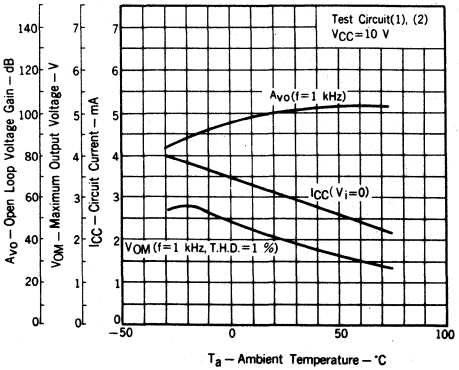
VOLTAGE GAIN vs. FREQUENCY



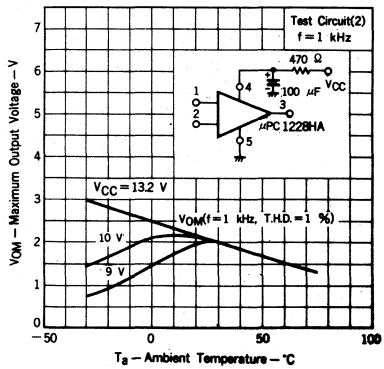
VOLTAGE GAIN vs. FREQUENCY



QUIESCENT CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs. AMBIENT TEMPERATURE

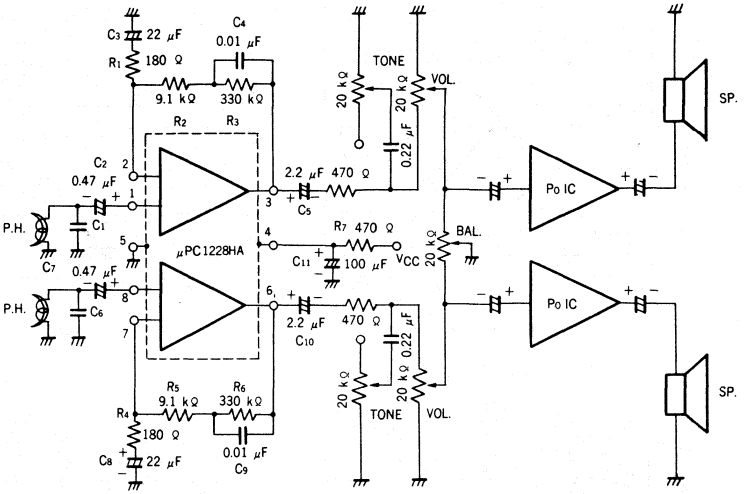


MAXIMUM OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE

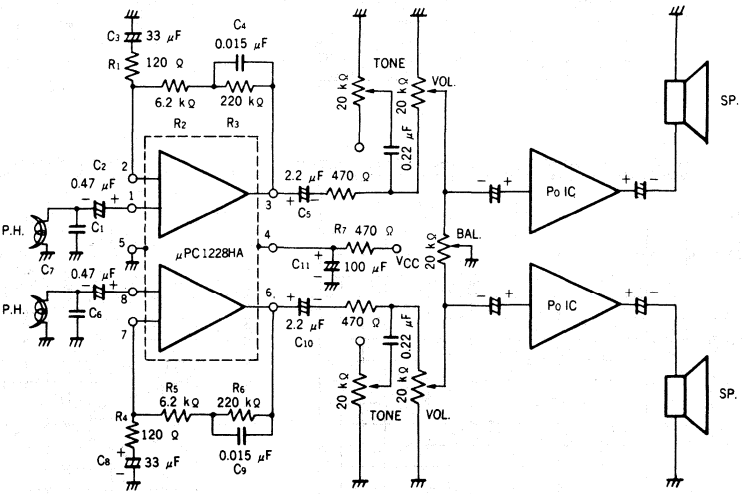


8

APPLICATION 1 (NAB EQ, V_{CC} = 8 to 17 V, V_{OM} = 2 V)

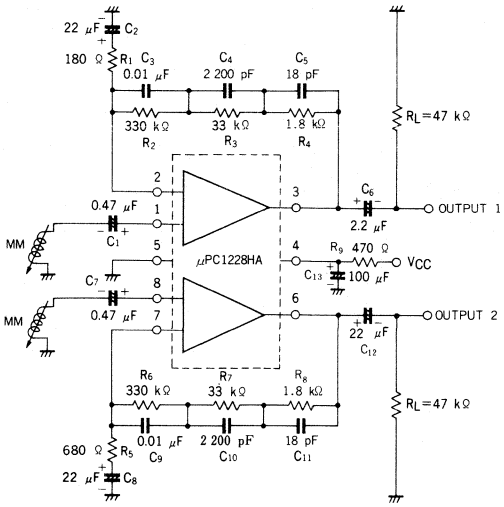


APPLICATION 2 (NAB EQ, V_{CC} = 6 to 17 V, V_{OM} = 1.2 V)



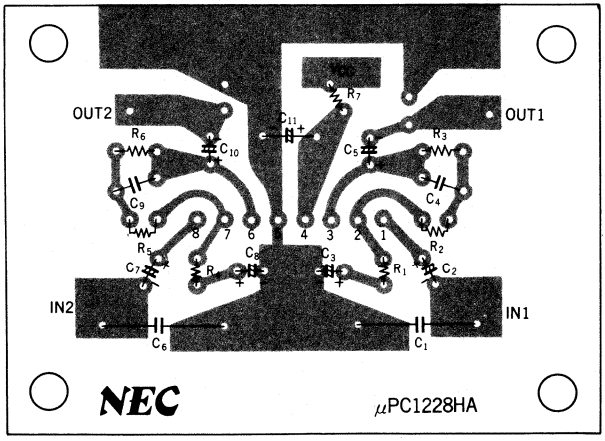
* When supply voltage of pin ④ is down to 6 V, please use TYPICAL APPLICATION 2.

APPLICATION 3 (NAB EQ, V_{CC} = 8 to 18 V, V_{OM} = 2 V)



TYPICAL PRINTED CIRCUIT BOARD PATTERN

Copper foil side



PROTECTOR IC FOR STEREO POWER AMPLIFIER

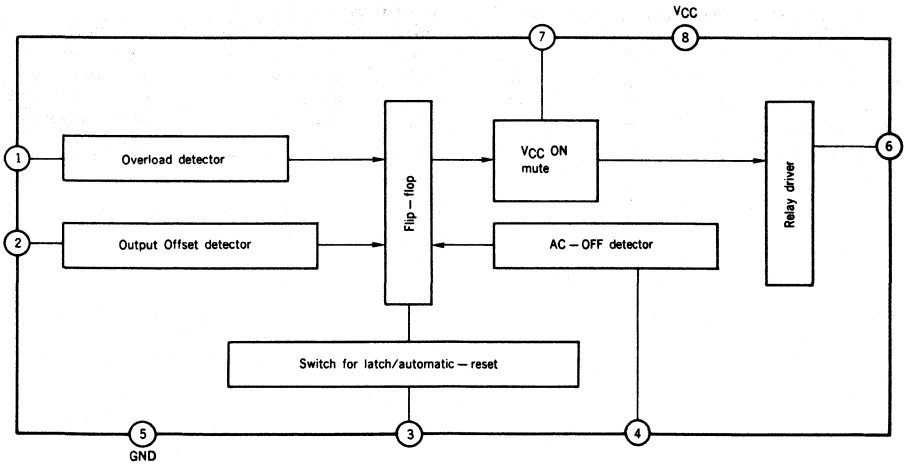
DESCRIPTION

μPC1237HA is a monolithic integrated circuit designed for protecting stereo power amplifiers and loudspeakers, and is in an 8 pin single in-line package.

FEATURES

- Work stably within a wide power supply voltage range. (V_{CC} = 25 to 60 V)
- Contain a relay driver. (Max. I_6 = 80 mA)
- Work as either latching function or automatic resetting function by using pin 3. (In both overload detection and output offset detection, either function can be selected.)
- Need only single power supply.
- Both positive and negative output offset can be detected through the same pin. (Output offset detection through pin 2)
- AC voltage can be detected. (For AC-power-OFF mute through pin 4)
- The time delay from amplifier power ON to relay ON can be freely set by selecting external components. (For AC-power-ON mute through pin 7)
- The moment that amplifier-power is turned off, it can make relay broken OFF and then loudspeaker disconnected from amplifier to prevent a shock off noise.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power Supply Voltage	V_{CC}	60	V
Allowable Power Dissipation	P_D	320*	mW
Operational Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Pin 6 Maximum Current	I_6 max	80	mA
Pin 4 Maximum Voltage	V_4 max	10	V
Pin 8 Maximum Voltage	V_8 max	8	V
Pin 1 Maximum Current	I_1 max	3	mA
Pin 2 Maximum Current	I_2 max	±3	mA
Pin 7 Maximum Voltage	V_7 max	8	V

*T_a = 75 °C

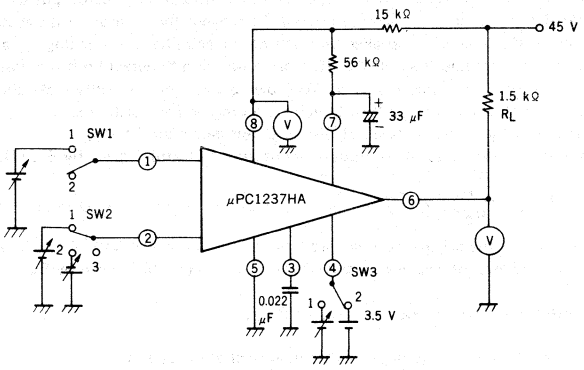
RECOMMENDED OPERATING CONDITION

Supply Voltage V_{CC} = 25 to 45 to 60 V

ELECTRICAL CHARACTERISTICS (V_{CC} = 45 V, T_a = 25 °C, State using latching function)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX.	UNIT	CONDITION
Pin 1 Threshold Voltage	Vth 1	0.58	0.67	0.76	V	level to invert at pin 6
Pin 2 Positive Threshold Voltage	Vth^+2	0.54	0.62	0.70	V	level to invert at pin 6
Pin 2 Negative Threshold Voltage	Vth^-2	−0.12	−0.17	−0.23	V	level to invert at pin 6
Pin 4 Threshold Voltage	Vth 4	0.60	0.74	0.90	V	level to invert at pin 6
Pin 8 Reference Voltage	V8	3.0	3.4	3.8	V	R_L = 1.5 kΩ

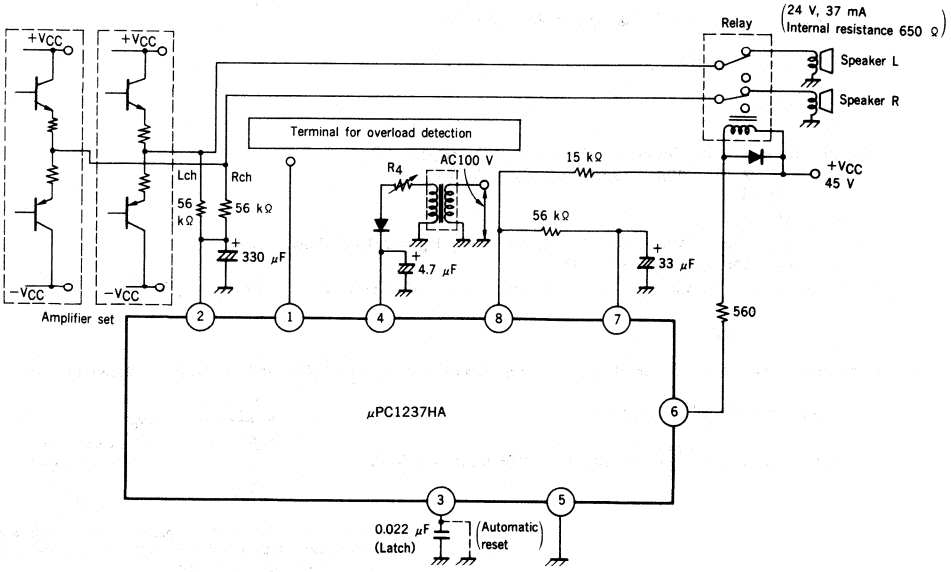
TEST CIRCUIT (State using latchung function)



Switch positions

Item	SW 1	SW 2	SW 3
Vth 1	1	3	2
Vth+2	2	1	2
Vth−2	2	2	2
Vth 4	2	3	1
V8	2	3	2

TYPICAL APPLICATION CIRCUIT



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NOTE FOR USING μPC1237HA

1. FUNCTION FOR OUTPUT OFFSET DETECTION (pin 2)

1) If too much DC current flows through a speaker voice coil due to large output offset DC level, the voice coil might be overheated and the speaker might be broken. To prevent the damage, it is necessary to detect the Output Offset DC level and to disconnect the speaker from the power amplifier by breaking off a relay if the detected DC level is shifted beyond a threshold level. μPC1237HA has a function to detect both the positive and the negative Output Offset DC level with its single power supply. As shown below, you can easily make the positive and the negative threshold level equivalent and also set up their level by choosing proper resistances.

2) How to determine the threshold levels of Output Offset detection. (±Vth)

[1] The threshold level of positive output offset detection (+Vth) is given by Eq. (1).

$$+Vth = (2 + \frac{R_A}{R_C}) \cdot Vth^{+}2, \quad \cdots\cdots (1)$$

where $Vth^{+}2$ is the original positive threshold level of pin 2, and $Vth^{+}2 = 0.62$ V TYP.

[2] The threshold level of negative Output Offset detection (−Vth) is given by Eq. (2).

$$-Vth = -\left\{ -Vth^{-}2 \cdot (2 + \frac{R_A}{R_C}) + I_{c2} \cdot R_A \right\}, \quad \cdots\cdots (2)$$

where $Vth^{-}2$ is the original negative threshold level of pin 2, and
$Vth^{-}2 = -0.17$ V TYP.
and I_{c2} is the current from μPC1237HA and,
$I_{c2} = 12.5$ μA TYP.
at nearly −Vth.

3) You can easily find how to make ±Vth level equivalent as shown below

$$(2 + \frac{R_A}{R_C}) \cdot Vth^{+}2 = -\left\{ -Vth^{-}2 \cdot (2 + \frac{R_A}{R_C}) + I_{c2} \cdot RA \right\}, \quad \cdots\cdots (3)$$

therefore determine R_A, R_B and R_C from Eq. (3)

Attention; The original positive and negative threshold level at pin 2 without any resistances are unbalanced; +Vth = 0.62 V TYP. and −Vth = −0.17 V TYP.

Example of design

If you need the output offset threshold level ±Vth to be ±2.0 V, determine R_A, R_B and R_C as shown below.

[1] Substitute 2.0 to +Vth in Eq. (1) and obtain R_A / R_C.

$$2.0 = (2 + \frac{R_A}{R_C}) \times 0.62$$

$$\frac{R_A}{R_C} \fallingdotseq 1.226$$

[2] Substitute −2.0 to −Vth in Eq. (2) and obtain R_A (R_B) and R_C.

$-2.0 = -0.17\ (2 + 1.226) - 12.5\ (\mu A) \times R_A\ (k\Omega)$ (V)

$R_A = 116.1\ k\Omega$

$R_C = 94.7\ k\Omega$

Therefore, if you need ±Vth to be 2.0 volts, choose R_A, R_B and R_C as shown below.

$R_A = R_B = 120\ k\Omega$ and $R_C = 91\ k\Omega$

The lower limits of R_A and R_B are given by the maximum rating (±3 mA) of pin 2 and

$$\frac{\pm V_{CC}}{R_A(B)} < \pm 3\ (mA)$$

In case of recommended condition, that is $R_A = R_B = 56\ k\Omega$ and $R_C = \infty$, ±Vth can be obtained as shown below.

[1] $+Vth = (2 + \frac{56\ (k\Omega)}{\infty})\ \ 0.62 = 1.24$ (V)

[2] $-Vth = -0.17\ (2 + \frac{56\ (k\Omega)}{\infty}) - 12.5\ (\mu A) \times 56\ (k\Omega) = -1.04$ (V)

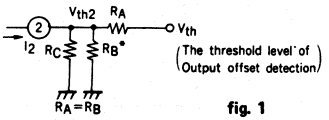


fig. 1

* Rch power amplifier output terminal is usually an imaginally GND as seen from Lch power amplifier, so that the equivalent circuit can be obtained as shown above.

2. FUNCTION OF AC LEVEL DETECTION

When you turn off the power switch, it sometimes causes a shock-off noise, therefore it is necessary to break off the relay and then to keep the power amplifier apart from loud speaker at the moment that power switch is turned off. In other words, the protection circuit is required to have a function to detect that power-off time. However, in fact, it is difficult to detect that power-off time from actual DC supply voltage line. Because it cannot be turned 0 V instantaneously due to a large capacitance inserted between the power supply line and GND. In case of μPC1237HA, it can detect this power-off time from AC power supply directly, that is, this is a function to detect AC level.

The AC power supply level (usually 50 Hz or 60 Hz) can be transmitted to pin 4 through a half-wave rectification circuit as shown below.

And it works within a wide range of AC level by choosing a proper resistance as R4 (Refer to the characteristic curve shown as fig.5 for the choice of R4). If power switch is turned off while the relay is being made ON and the speaker is being connected to the power amplifier output, the relay will be broken OFF to disconnect the speaker after a time delay (AC OFF mute) according to the discharge time constant determined by the voltage on pin 4, the external capacitance C4, and the internal resistance of the IC.

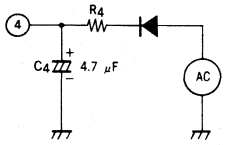


fig. 2

3. FUNCTION OF OVERLOAD DETECTION (pin 1)

The original threshold level of pin 1 is 0.67 V TYP. In case of using a constant-current drive, as the means of detection, the threshold current level is 110 μA TYP. When current which is larger than 110 μA flows to the IC, the relay will be broken OFF.

Note ; The overload detecting circuit is not included in the IC because of patent problems. Use the external circuit as an overload detection.

4. FUNCTION OF LATCHING AND AUTOMATIC RESETTING (pin 3)

If the IC detects the abnormal condition such as the larger output offset level or the overload, the IC can make the relay broken OFF. And then, two functions can be selected after the condition returns to the normal state. One is that the relay is made ON automatically and the other is that it keeps the relay broken off until once the power switch is turned off and then is turned on again.

The former is a function of automatic resetting and the latter is a function of latching. μPC1237HA has both functions and can be selected either function by using pin 3. In case of latching, connect pin 3 to the ground through the capacitor, which is for preventing misoperation. For automatic resetting, connect it to the ground directly. This function is valid for both overload detection and output offset detection.

5. TIME DELAY FROM POWER AMPLIFIER POWER SWITCH ON TO RELAY ON (power-on mute at pin 7)

To suppress shock-on noise generated by power ON, a time delay is provided by connecting a circuit with a time constant. This time delay is set to make relay ON to connect speakers after enough time for the power amplifier and the preamplifier to reach a stable operating condition. The ON mute time is determined as follows,

$$T\ (\text{ON mute}) = -C_7 \cdot R_7 \cdot \ell n \frac{V_8 - V_7}{V_8},$$

where V_8 is reference voltage at pin 8, 3.40 volts, TYP. and V_7 is threshold level at pin 7, 2.06 volts, TYP.

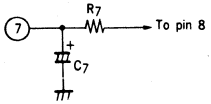


fig. 3

6. HOW TO MAKE IT WORK WITHIN A WIDE RANGE OF POWER SUPPLY VOLTAGE (pin 8)

By choosing a proper resistance R_8 connected to pin 8, the IC can work within a wide range of power supply voltage V_{CC} from 25 to 60 volts.

In case that pin 8 is directly driven by a regulated power supply, set V_8 to 3.40 volts, TYP. As for the choice of R_8 value, refer to the characteristic curve shown as fig.6.

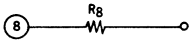
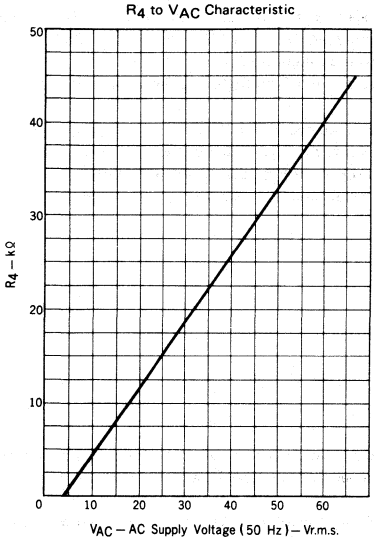
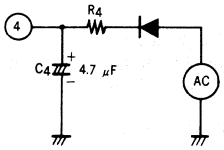


fig. 4

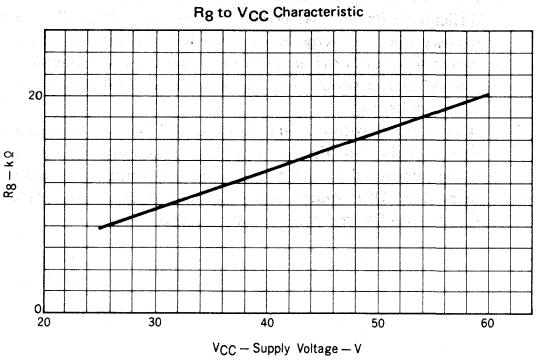
fig. 5 OPTIMUM VALUE OF EXTERNAL RESISTANCE R_4

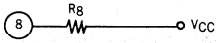




Example) Use of E-24 series.
Select 24 kΩ R_4 for 40 volts r.m.s. V_{AC}.
If no resistance of specified value is available, choose a resistance which is as close as possible to and lower than the value specified by the diagram.

fig. 6 OPTIMUM VALUE OF EXTERNAL RESISTANCE R_8

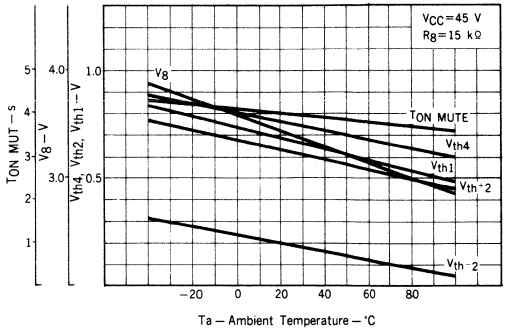




Example) Use of E-24 series.
Select 15 kΩ R_8 for 45 volts Vcc.
If no resistance of specified value is available, choose a resistance which is as close as possible to and lower than the value specified by the diagram.

TEMPERATURE CHARACTERISTIC

V_8, T_{ON} mut, Vth4, Vth+2, and Vth1 to Ta Characteristics



50 to 80 W POWER AMPLIFIER DRIVER

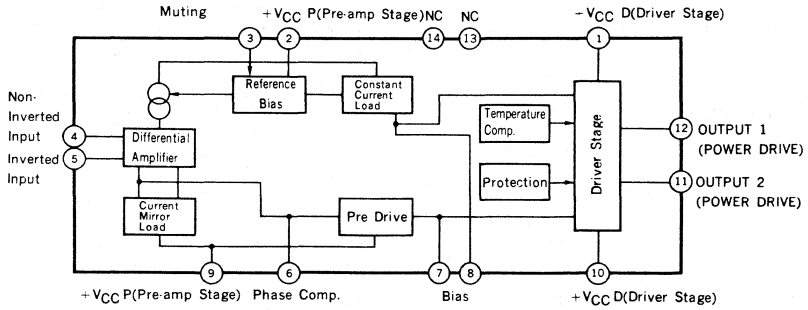
DESCRIPTION

μPC1298V is a integrated monolithic circuit designed for 50 W to 80 W class HiFi audio power amplifier and consists of a input differential amplifier, a predriver circuit, a driver circuit and a over current protection circuit.

FEATURES

- Low Distortion.
  0.002 % TYP. (V_{CC} = ±46 V, f = 1 kHz, A_v = 30 dB, P_O = 50 W, R_L = 8 Ω with Power Transistor)
  0.006 % TYP. (V_{CC} = ±46 V, f = 20 kHz, A_v = 30 dB, P_O = 50 W, R_L = 8 Ω with Power Transistor)
- Wide Frequency Band.
  900 kHz TYP. (–3 dB)
- Wide Power Band Width.
  90 kHz TYP. (P_O = 40 W, THD = 0.1 %)

BLOCK DIAGRAM



NOTE: The built-in over current circuit protects μPC1298V and cannot protect external power transistors.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Quiescent)	V_{CC1}	±65	V
Supply Voltage (Operational)	V_{CC2}	±60	V
Circuit Current	$I_{CC(peak)}$	250	mA
Allowable Package Dissipation	P_D	7.5*	W
Operational Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C

* 100 x 100 x 2 mm Al heat sink

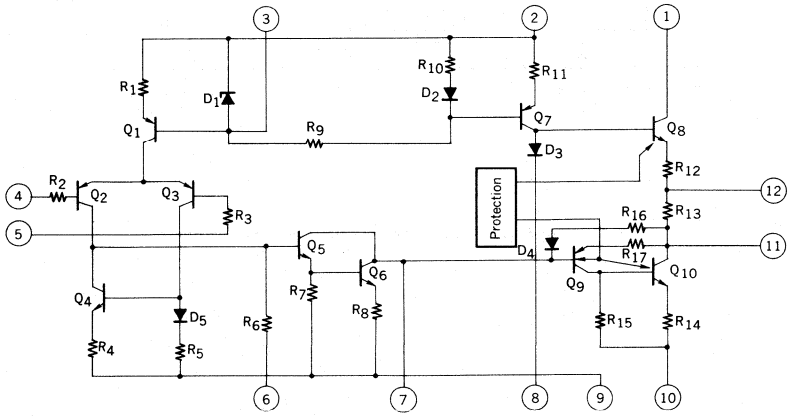
RECOMMENDED OPERATING CONDITION

Supply Voltage (Operational)	V_{CC} = ±20 to ±46 V
Input Bias Resistance	R_{IN} = 1 to 50 to 100 kΩ
Power Transistor h_{FE}	$h_{FE} \geqq 50$ at P_O = 80 W, R_L = 8 Ω, $T_j < 125$ °C
Closed Loop Voltage Gain	A_v = 26 to 30 dB
Junction Temperature	T_j = −20 to 125 °C

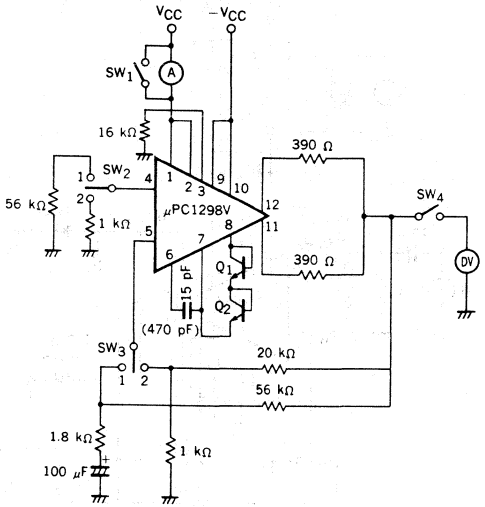
ELECTRICAL CHARACTERISTICS (V_{CC} = ±46 V, A_v = 30 dB, Use Standard Test Circuit, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Output Offset Voltage	V_{offset}		±5	±50	mV	V_{IN} = 0
Quiescent Circuit Current	I_{CC}		20	40	mA	V_{IN} = 0
Maximum Output Voltage	V_{OM}	25	28		V	THD = 0.05%, f = 20 Hz to 20 kHz
Open Loop Voltage Gain	A_{vo}	80	95		dB	V_o = 1.5 V, f = 1 kHz
Output Noise Voltage	V_n		0.07	0.14	mV	R_G = 10 kΩ
Rolloff Frequency	f_H		900		kHz	V_o = 1.5 V, −3 dB
Supply Voltage Rejection Ratio	SVR	55	70		dB	R_G = 2.2 kΩ, f_{ripple} = 100 Hz, v_{ripple} = 1 $V_{r.m.s.}$

EQUIVALENT CIRCUIT



TEST CIRCUIT 1 (I_{CC}, V_{OFF})



Q_1, Q_2 } 2SC1844F

SWITCH POSITION

	SW_1	SW_2	SW_3	SW_4
I_{CC}	OFF	2	2	OFF
V_{OFF}	ON	1	1	ON

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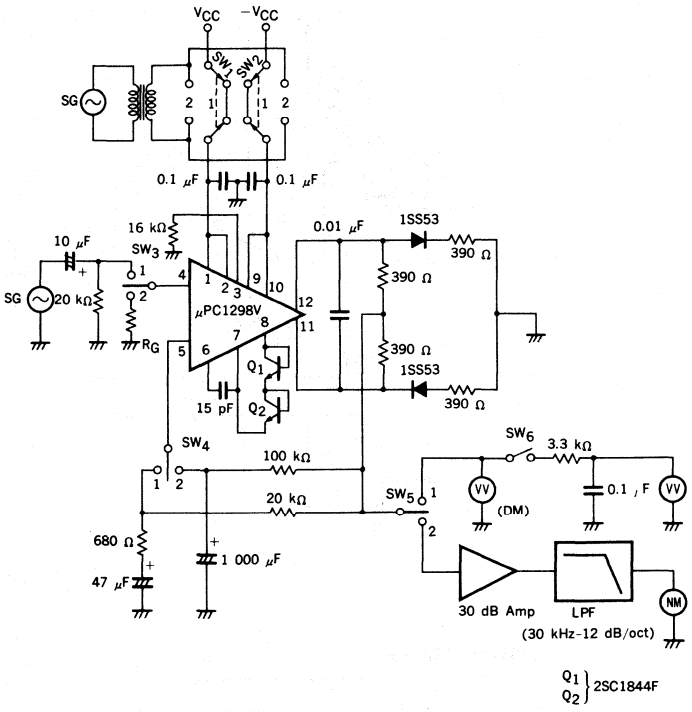
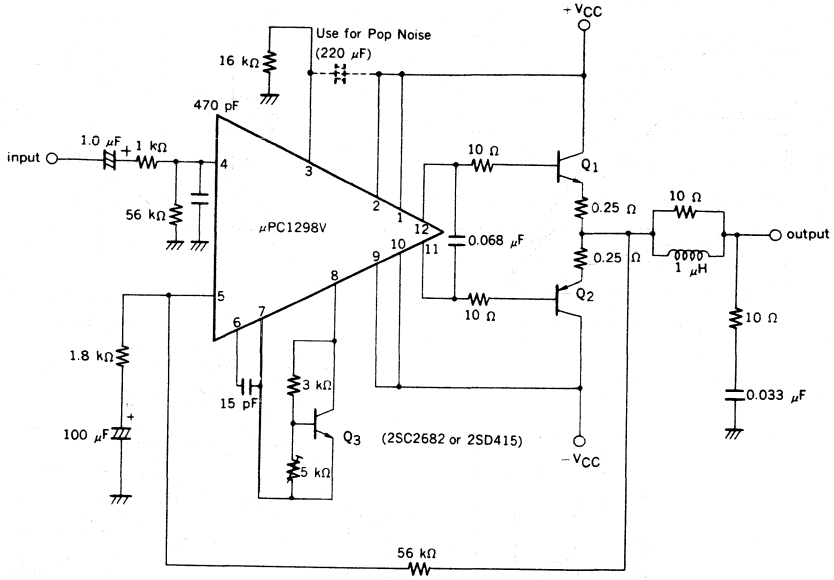
TEST CIRCUIT 2 (V_{OM}, A_v, A_{vO}, V_{NO}, SVR, PBW)



SWITCH POSITION

	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6
V_{OM}	1	1	1	1	1	OFF
A_v	1	1	1	1	1	OFF
A_{vO}	1	1	1	2	1	OFF
V_{NO}	1	1	2	1	2	OFF
SVR	2/1	1/2	2	1	1	ON
PBW	1	1	1	1	1	OFF

APPLICATION CIRCUIT



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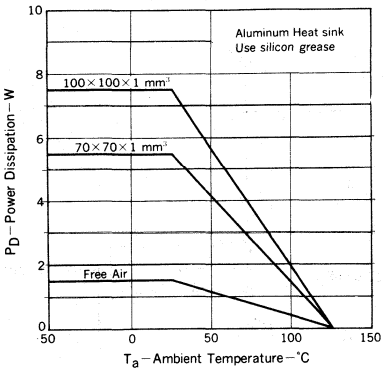
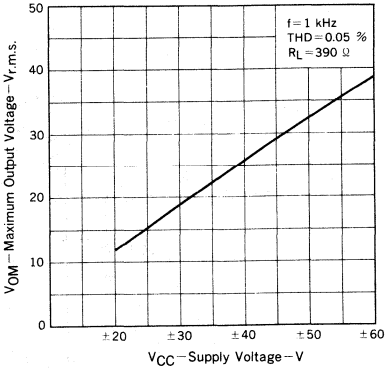
RECOMMENDED POWER TRANSISTOR

P_O	25 to 40 W	45 to 55 W	50 to 70 W	70 to 80 W
Q_1	2SD1288 2SD2013	2SD1289 2SD1977	2SC3012 2SC4267	2SC2987 2SC2987A 2SC4268
Q_2	2SB965 2SB1336	2SB966 2SB1315	2SA1232 2SA1631	2SA1227 2SA1227A 2SA1632

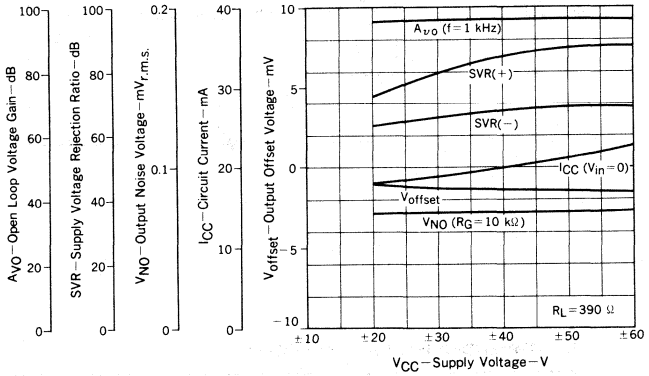
POWER DISSIPATION vs.
AMBIENT TEMPERATURE



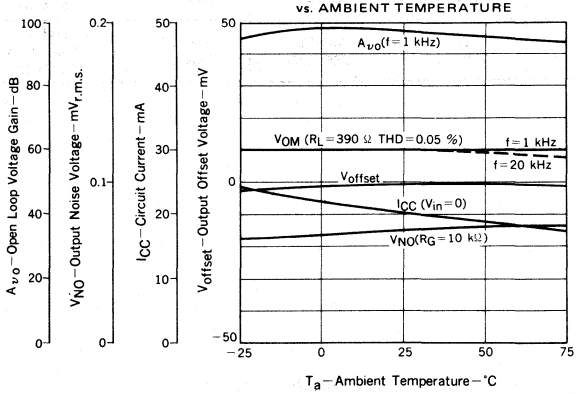
MAXIMUM OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



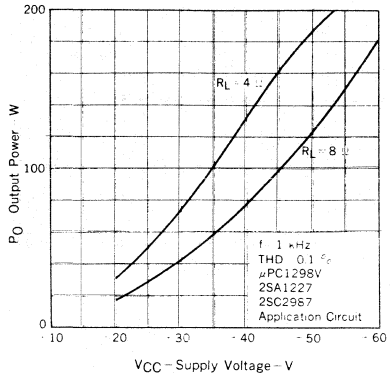
OPEN LOOP VOLTAGE GAIN,
SUPPLY VOLTAGE REJECTION RATIO,
OUTPUT NOISE VOLTAGE,
CIRCUIT CURRENT,
OUTPUT OFFSET VOLTAGE
vs. SUPPLY VOLTAGE



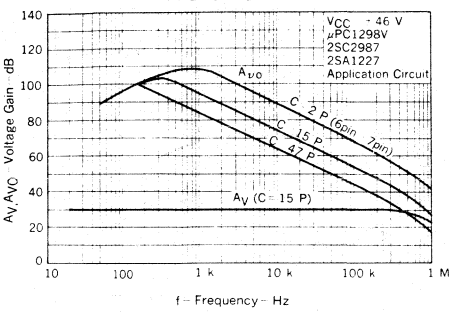
OPEN LOOP VOLTAGE GAIN,
OUTPUT NOISE VOLTAGE,
CIRCUIT CURRENT,
OUTPUT OFFSET VOLTAGE
vs. AMBIENT TEMPERATURE



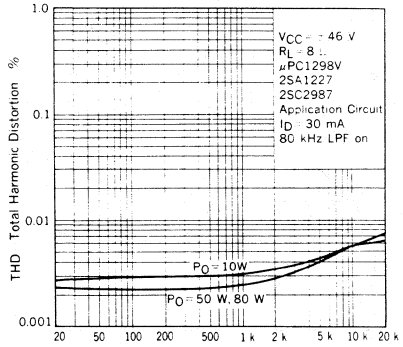
OUTPUT POWER vs. SUPPLY VOLTAGE



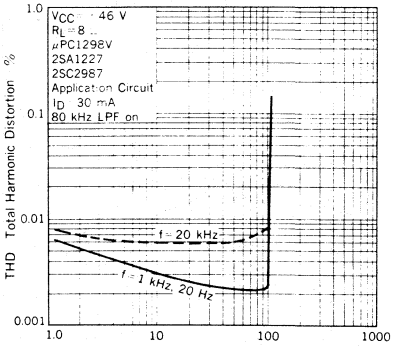
VOLTAGE GAIN vs. FREQUENCY



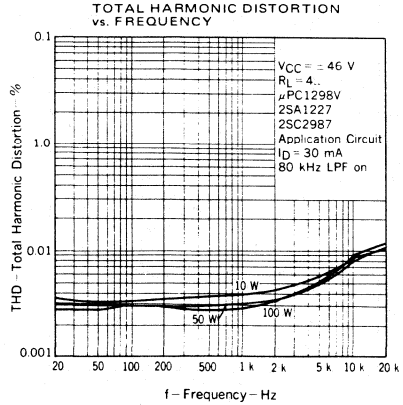
TOTAL POWER DISTORTION vs. FREQUENCY



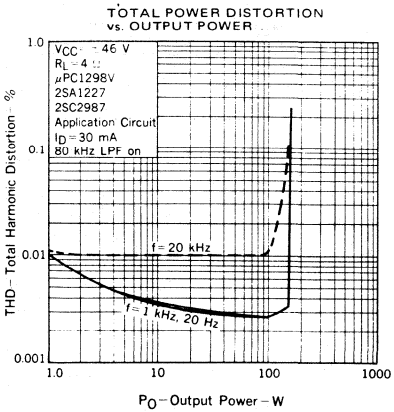
TOTAL POWER DISTORTION vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL POWER DISTORTION vs. OUTPUT POWER



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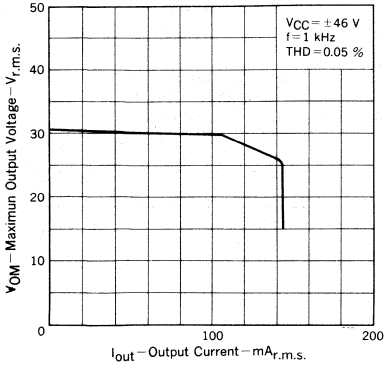
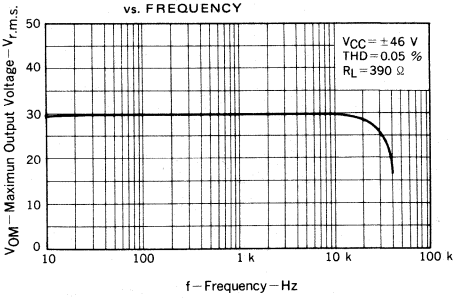
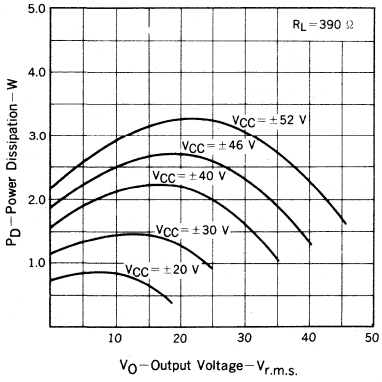
MAXIMUM OUTPUT VOLTAGE
vs. OUTPUT CURRENT



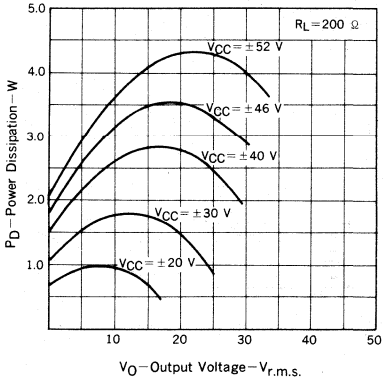
MAXIMUM OUTPUT VOLTAGE
vs. FREQUENCY



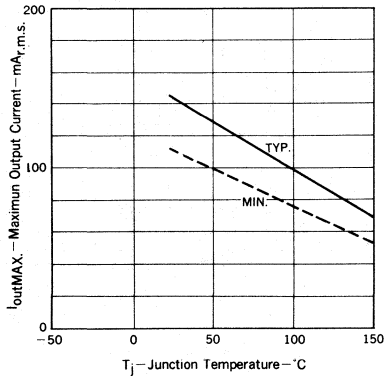
POWER DISSIPATION vs.
OUTPUT VOLTAGE



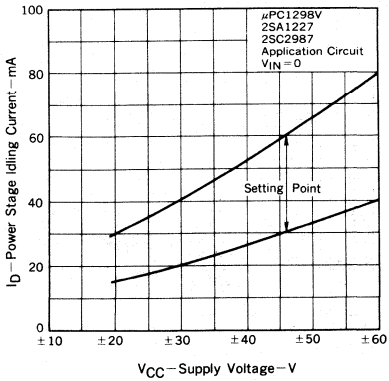
POWER DISSIPATION
vs. OUTPUT VOLTAGE



MAXIMUM OUTPUT CURRENT
vs. JUNCTION TEMPERATURE



POWER STAGE IDLING CURRENT
vs. SUPPLY VOLTAGE



50 to 110 W POWER AMPLIFIER DRIVER

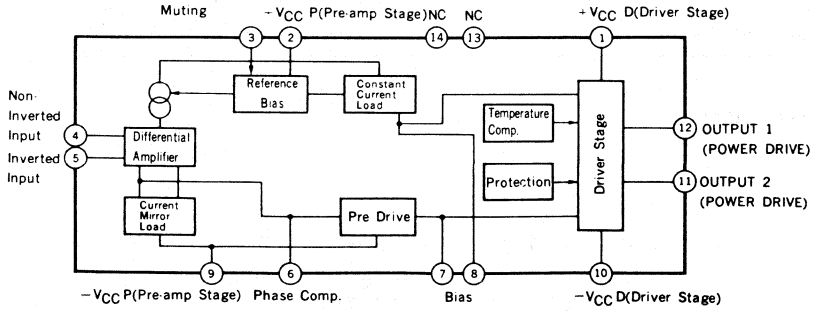
DESCRIPTION

μPC1342V is a integrated monolithic circuit designed for 50 W to 110 W class HiFi audio power amplifier and consists of a input differential amplifier, a predriver circuit, a driver circuit and a over current protection circuit.

FEATURES

- Low Distortion.
  0.002 % TYP. (V_{CC} = ±46 V, f = 1 kHz, A_v = 30 dB, P_O = 80 W, R_L = 8 Ω with Power Transistor)
  0.006 % TYP. (V_{CC} = ±46 V, f = 20 kHz, A_v = 30 dB, P_O = 80 W, R_L = 8 Ω with Power Transistor)
- Wide Frequency Band.
  900 kHz TYP. (–3 dB)
- Wide Power Band Width.
  90 kHz TYP. (P_O = 40 W, THD = 0.1 %)

BLOCK DIAGRAM



NOTE: The built-in over current circuit protects μPC1342V and cannot protect external power transistors.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Quiescent)	V_{CC1}	±75	V
Supply Voltage (Operational)	V_{CC2}	±70	V
Circuit Current	$I_{CC\,(peak)}$	250	mA
Allowable Package Dissipation	P_D	7.5*	W
Operational Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C

* 100 x 100 x 2 mm Al heat sink

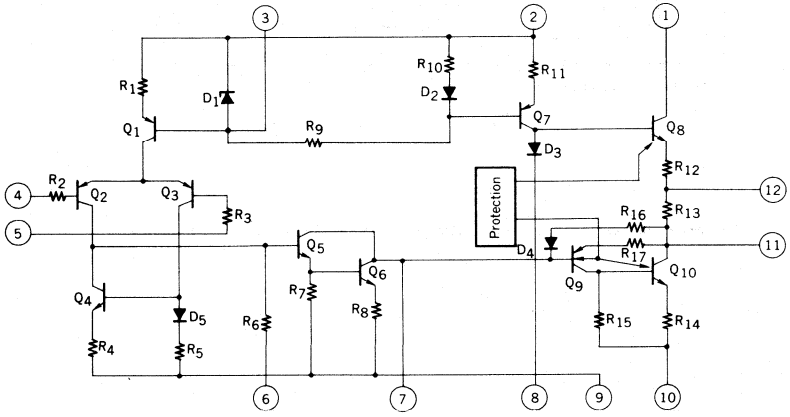
RECOMMENDED OPERATING CONDITIONS

Supply Voltage (Operational)	V_{CC} = ±20 to ±52 V
Input Bias Resistance	R_{IN} = 1 to 50 to 100 kΩ
Power Transistor h_{FE}	$h_{FE} \geq 50$ at P_O = 80 W, R_L = 8 Ω, $T_j < 125$ °C
Closed Loop Voltage Gain	A_v = 26 to 30 dB
Junction Temperature	T_j = −20 to 125 °C

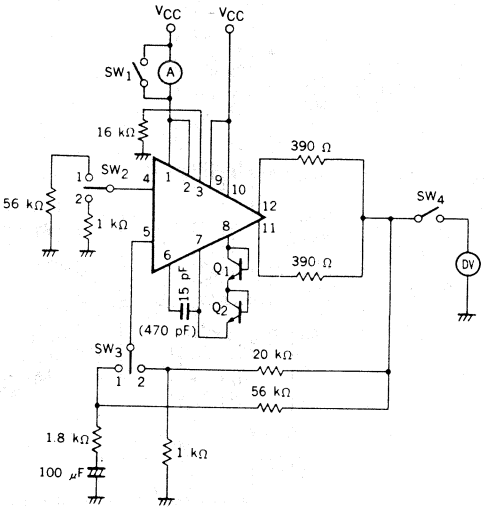
ELECTRICAL CHARACTERISTICS (V_{CC} = ±46 V, A_v = 30 dB, Use Standard Test Circuit, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Output Offset Voltage	V_{offset}		±5	±50	mV	V_{IN} = 0
Quiescent Circuit Current	I_{CC}		20	40	mA	V_{IN} = 0
Maximum Output Voltage	V_{OM}	25	28		V	THD = 0.05%, f = 20 Hz to 20 kHz
Open Loop Voltage Gain	A_{vo}	80	95		dB	V_o = 1.5 V, f = 1 kHz
Output Noise Voltage	V_n		0.07	0.14	mV	R_G = 10 kΩ
Rolloff Frequency	f_H		900		kHz	V_o = 1.5 V, −3 dB
Supply Voltage Rejection Ratio	SVR	55	70		dB	R_G = 2.2 kΩ, f_{ripple} = 100 Hz, v_{ripple} = 1 $V_{r.m.s.}$

EQUIVALENT CIRCUIT



TEST CIRCUIT 1 (I_{CC}, V_{OFF})



Q_1, Q_2 } 2SC1844F

SWITCH POSITION

	SW_1	SW_2	SW_3	SW_4
I_{CC}	OFF	2	2	OFF
V_{OFF}	ON	1	1	ON

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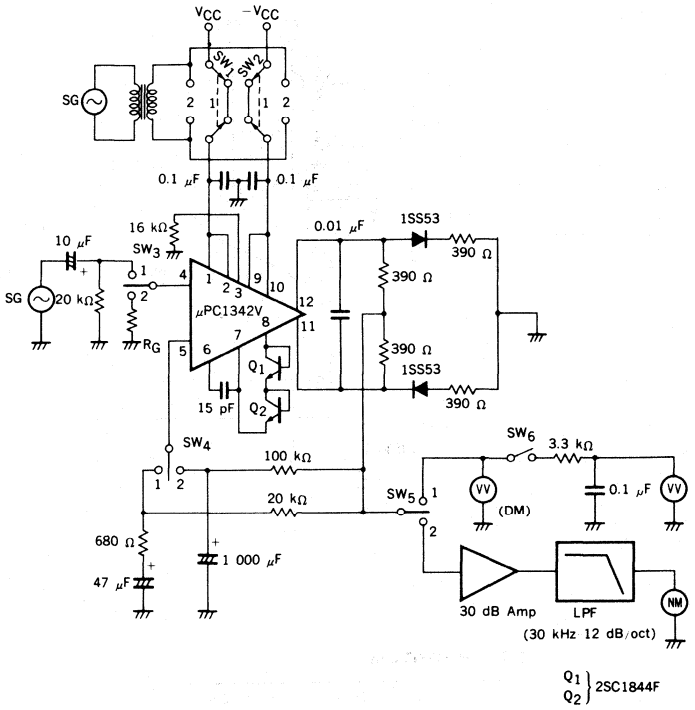
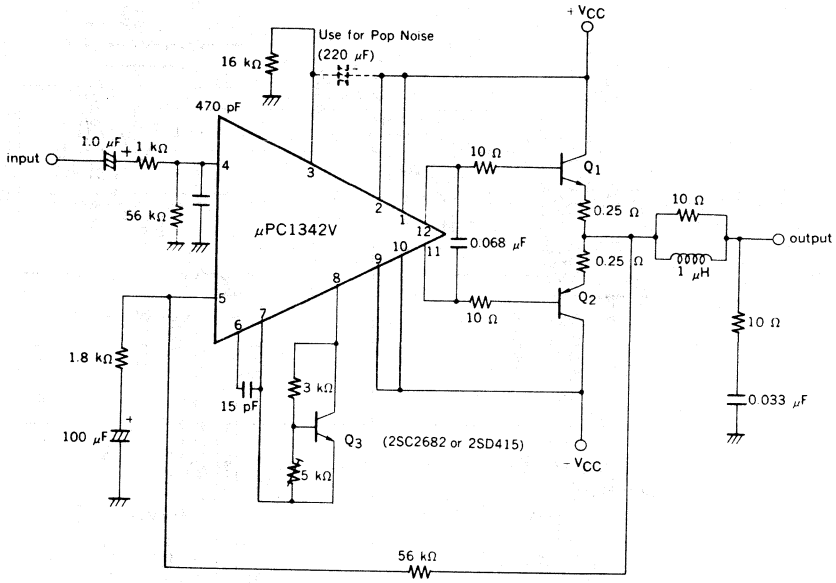
TEST CIRCUIT 2 (V_{OM}, A_v, A_{vO}, V_{NO}, SVR, PBW)



SWITCH POSITION

	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6
V_{OM}	1	1	1	1	1	OFF
A_v	1	1	1	1	1	OFF
A_{vO}	1	1	1	2	1	OFF
V_{NO}	1	1	2	1	2	OFF
SVR	2/1	1/2	2	1	1	ON
PBW	1	1	1	1	1	OFF

APPLICATION CIRCUIT



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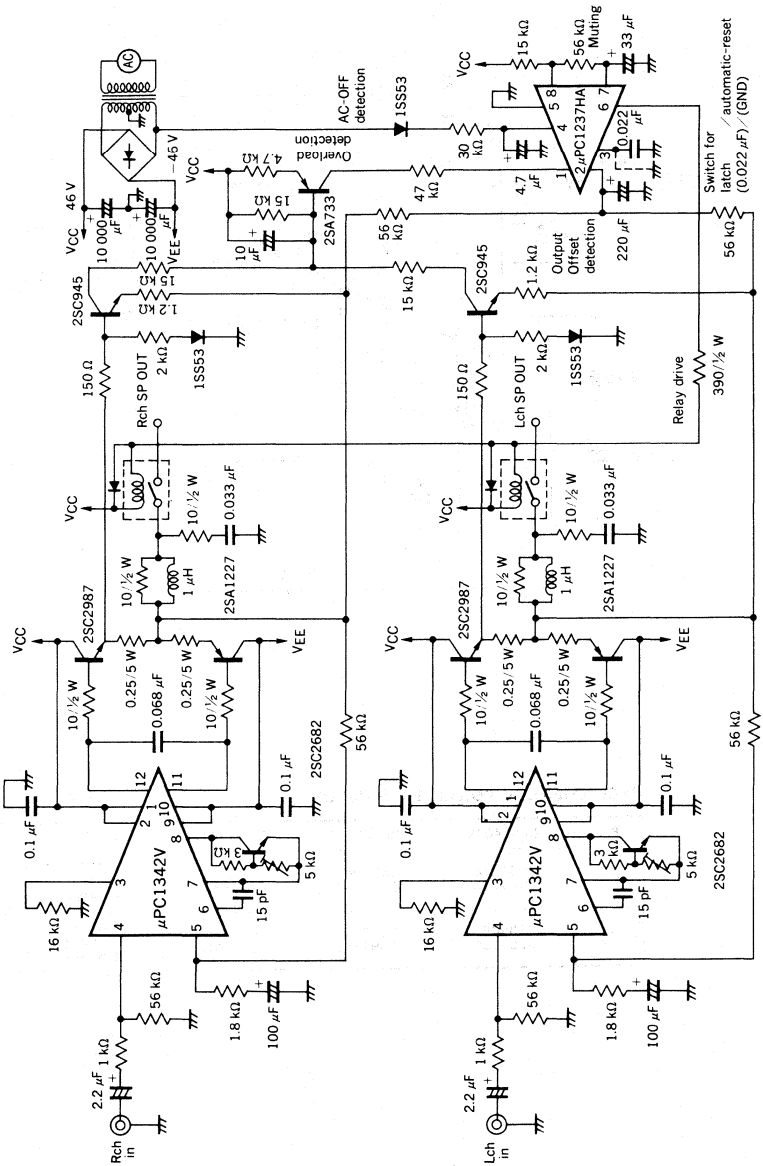
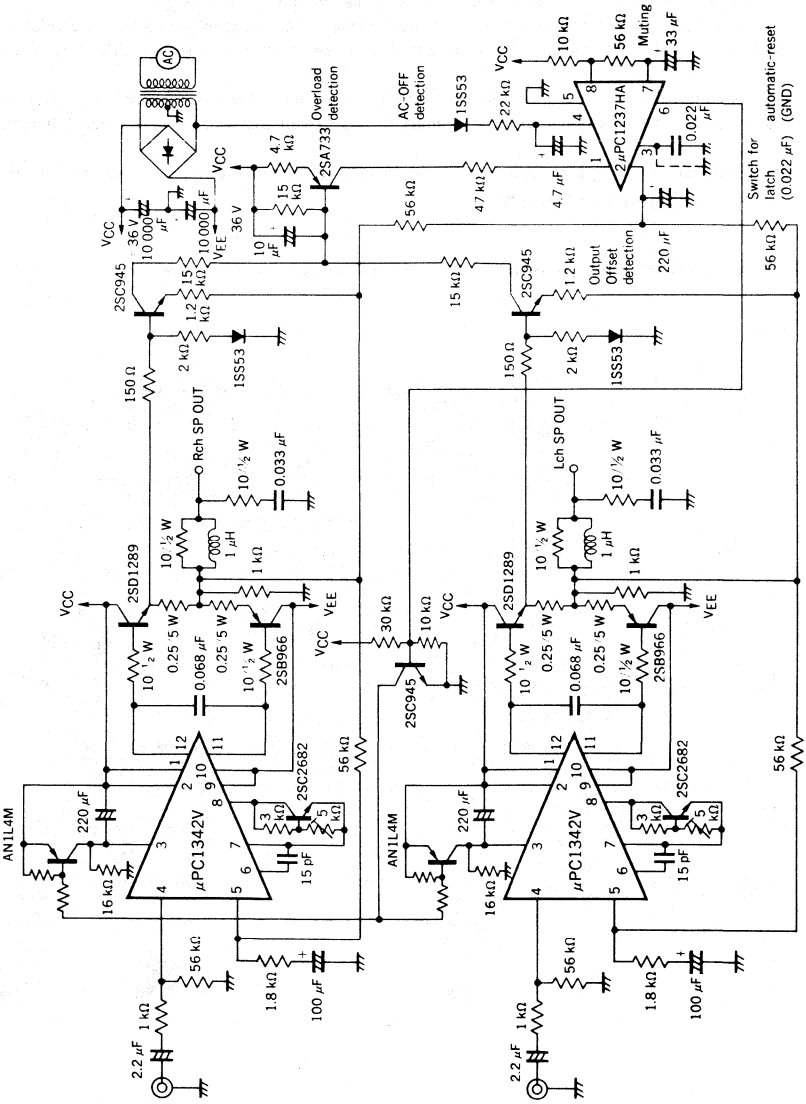
RECOMMENDED POWER TRANSISTOR

P_O	25 to 40 W	45 to 55 W	50 to 70 W	70 to 80 W	80 to 110 W
Q_1	2SD1288 2SD2013	2SD1289 2SD1977	2SC3012 2SC4267	2SC2987 2SC2987A 2SC4268	2SC2987A 2SC4268 × 2
Q_2	2SB965 2SB1336	2SB966 2SB1315	2SA1232 2SA1631	2SA1227 2SA1227A 2SA1632	2SA1227A 2SA1632 × 2

EXAMPLE 1 OF APPLICATION CIRCUIT WITH PROTECTION CIRCUIT (by use of relay)



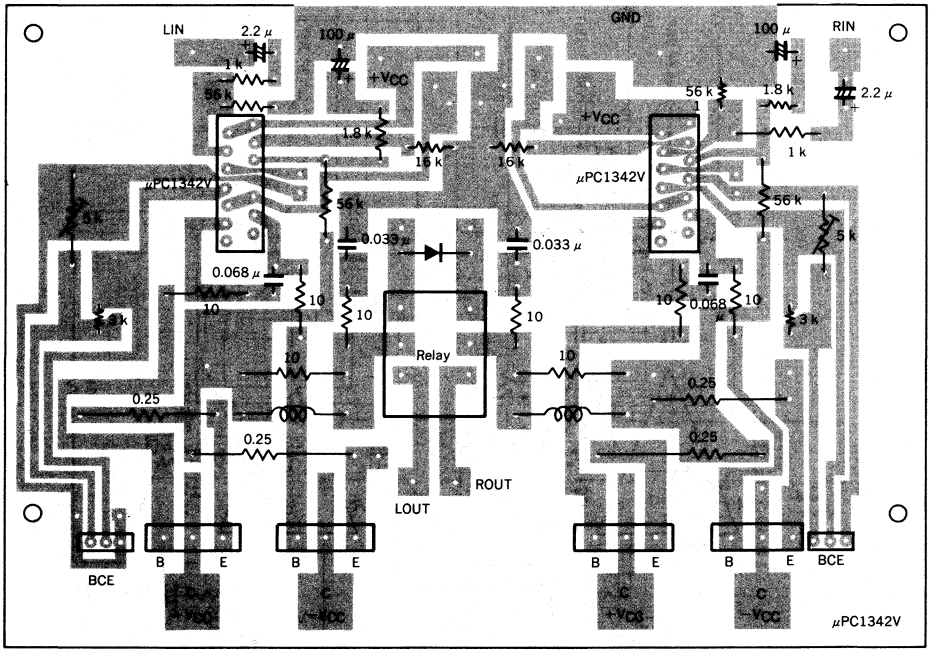
EXAMPLE 2 OF APPLICATION CIRCUIT WITH PROTECTION CIRCUIT



NOTES FOR USE

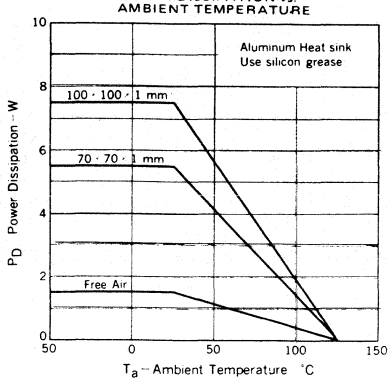
- If external heat sink is connected to other circuit electrically, the radiation fin of IC must be insulated from external heat sink electrically. Because the voltage of IC's radiation fin is equal to $-V_{CC}$.
- Pay attention to pattern layout of power source line and GND line, or some problem, as oscillation, may happen.
- Mylar capacitor is suitable for bypass capacitors between power source line and GND line, and 0.1 [μF] is suitable for these capacitances.
- The transistor in bias circuit between #7 and #8 can be replaced by varistor. Either transistor or varistor, which also do the part of temperature compensation, must be attached to the same heat sink that last stage power transistors are attached to.
- If the way of muting is to short-circuit between #2 and #3, add a resistor of which the value is about 1 [kΩ] between output and GND. (Refer to page 7)

EXAMPLE OF PRINT-CIRCUIT BOARD AND COMPONENTS LAYOUT (Copper side)

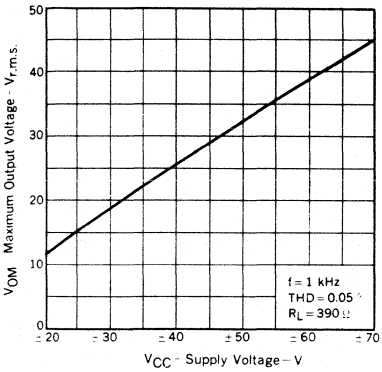


Unit : resistor-Ω, capacitor-F

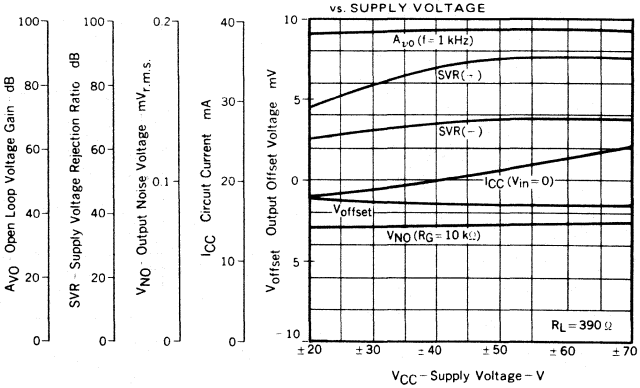
POWER DISSIPATION vs.
AMBIENT TEMPERATURE



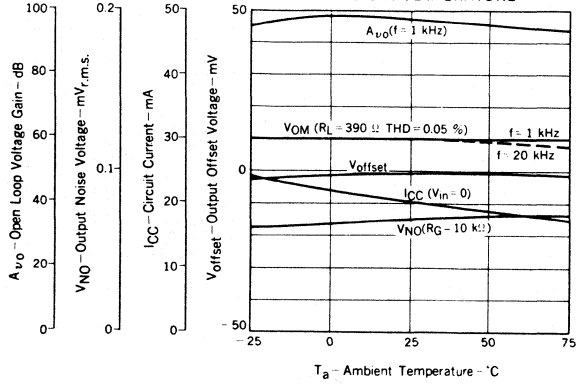
MAXIMUM OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



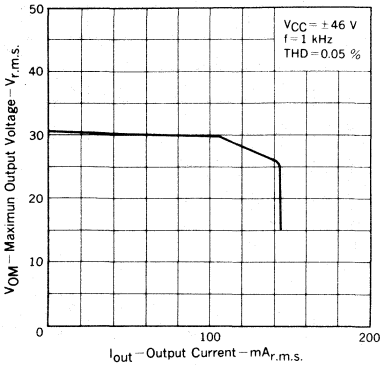
OPEN LOOP VOLTAGE GAIN,
SUPPLY VOLTAGE REJECTION RATIO,
OUTPUT NOISE VOLTAGE,
CIRCUIT CURRENT,
OUTPUT OFFSET VOLTAGE
vs. SUPPLY VOLTAGE



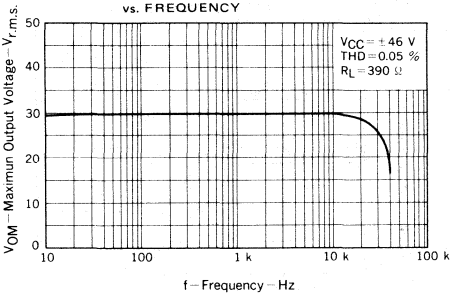
OPEN LOOP VOLTAGE GAIN,
OUTPUT NOISE VOLTAGE,
CIRCUIT CURRENT,
OUTPUT OFFSET VOLTAGE
vs. AMBIENT TEMPERATURE



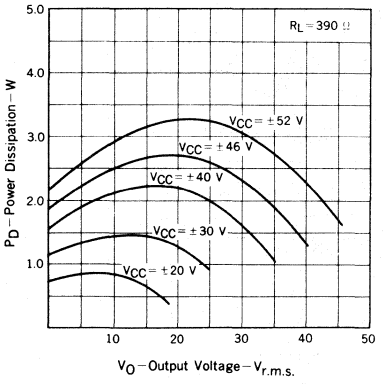
MAXIMUM OUTPUT VOLTAGE
vs. OUTPUT CURRENT



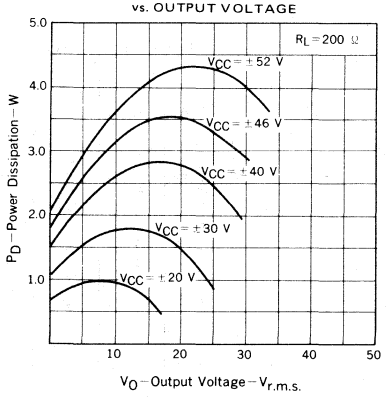
MAXIMUM OUTPUT VOLTAGE
vs. FREQUENCY



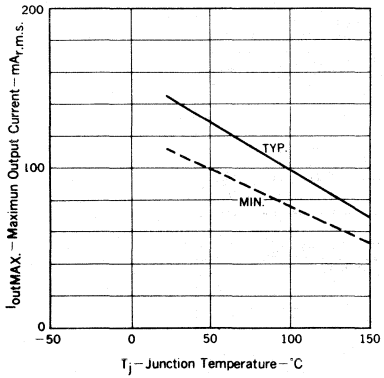
POWER DISSIPATION vs.
OUTPUT VOLTAGE



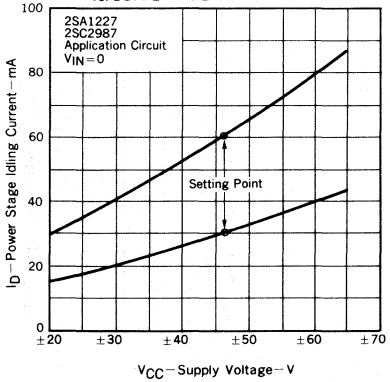
POWER DISSIPATION
vs. OUTPUT VOLTAGE



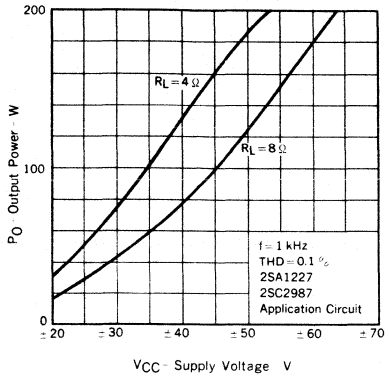
MAXIMUM OUTPUT CURRENT
vs. JUNCTION TEMPERATURE



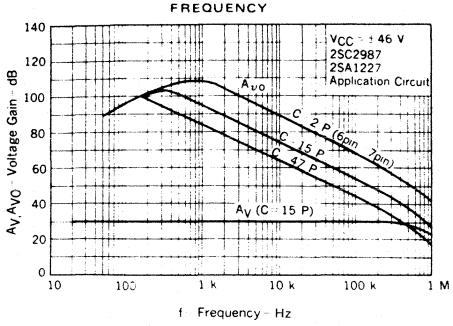
POWER STAGE IDLING CURRENT
vs. SUPPLY VOLTAGE



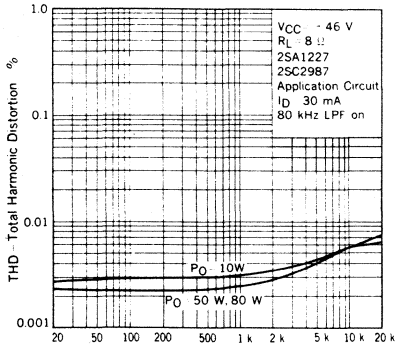
OUTPUT POWER vs. SUPPLY VOLTAGE



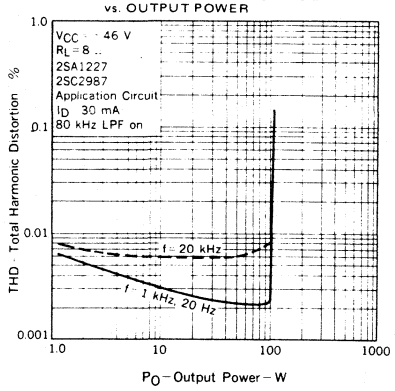
VOLTAGE GAIN vs. FREQUENCY



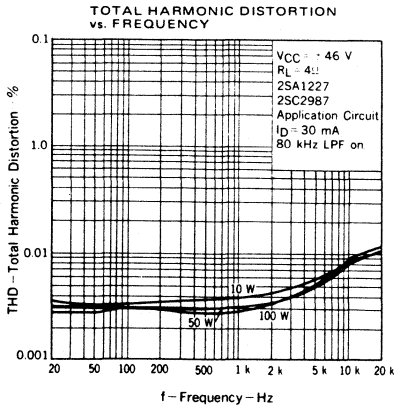
TOTAL POWER DISTORTION vs. FREQUENCY



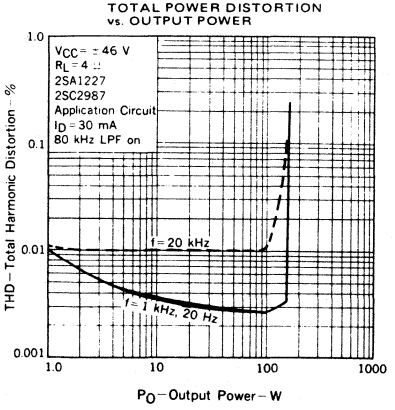
TOTAL POWER DISTORTION vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL POWER DISTORTION vs. OUTPUT POWER



8

45 W AF POWER AMPLIFIER

DESCRIPTION

The μPC2500H is an audio power amplifier in a 12-lead single in-line package, specifically designed for car stereo applications.

Typically it provides output power of 45 W at 14.4 V or 40 W at 13.2 V to a 2 Ω load.

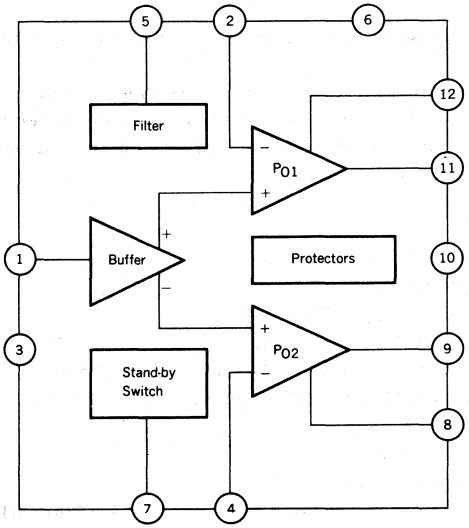
This IC can be used without output capacitors, because its two output terminals have the same potential and it includes original short circuit protection function which protects internal output power transistors and a speaker at the same time when one output terminal is shorted to ground or V_{CC}.

FEATURES

- Internal stand-by switch circuit; CMOS drive possible.
- Can be used as OCL connection.
- Very low output offset voltage : V_{offset} = 150 mV (MAX.)
- High output power : P_O = 45 W (TYP.) @ R_L = 2 Ω, V_{CC} = 14.4 V, THD = 10 %
  P_O = 40 W (TYP.) @ R_L = 2 Ω, V_{CC} = 13.2 V, THD = 10 %
- Very low distortion : THD = 0.03 % (TYP.) @ R_L = 2 Ω, V_{CC} = 13.2 V, P_O = 8 W, f = 1 kHz
- Following protection circuits are included.
  (1) Load dump voltage surge protection circuit.
  (2) Thermal shut down protection circuit.
  (3) Output terminal short circuit protection circuit. (V_{CC} to OUT, OUT to GND, OUT to OUT)
  (4) Loudspeaker protection circuit.

8

BLOCK DIAGRAM



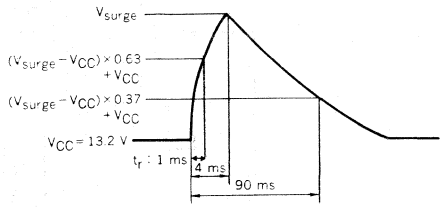
CONNECTION DIAGRAM

PIN NO.	CONNECTION	PIN NO.	CONNECTION
1	Input	7	Stand-by Switch
2	NFB1	8	Bootstrap 2
3	GND for Input	9	Output 2
4	NFB2	10	GND for Output
5	Filter	11	Output 1
6	V_{CC}	12	Bootstrap 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Note)	$V_{CC\ surge}$	60*	V
Supply Voltage (Operational)	V_{CC}	18	V
Output Current (Instantaneous)	I_o	8	A
Power Dissipation	P_D	50	W
Operating Temperature	T_{opt}	−30 to +85	°C
Storage Temperature	T_{stg}	−40 to +150	°C

*



Surge Pulse Waveform

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

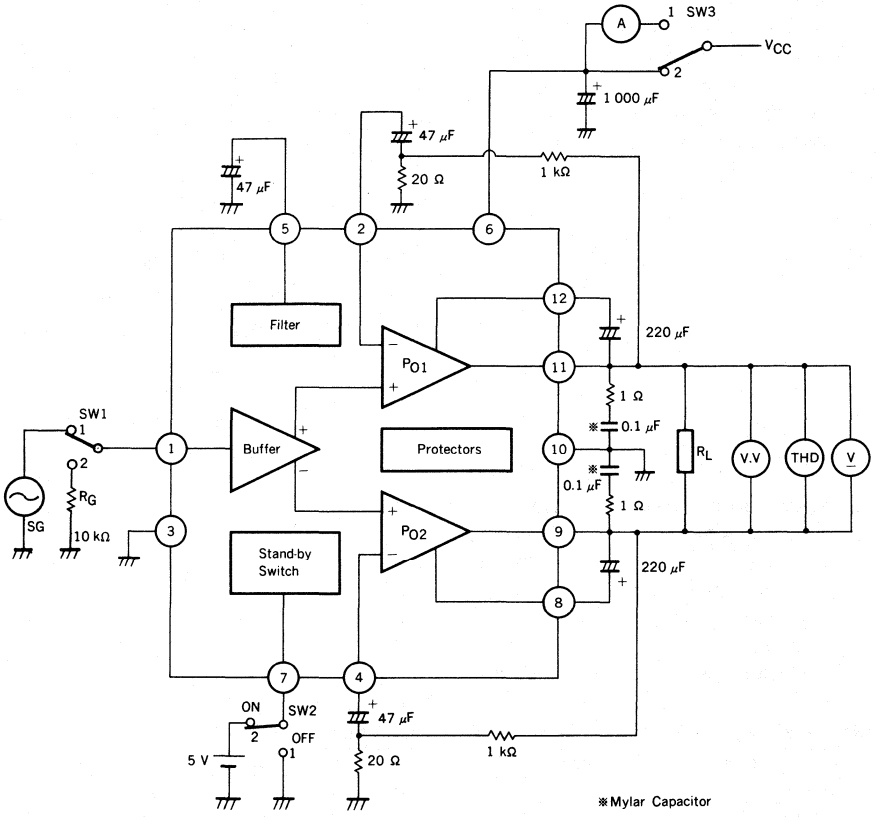
Supply Voltage Range	9 to 16	V
Load Impedance	2 to 8	Ω
Pin 7 Voltage (Operating)	3.5 to V_{CC}	V
Pin 7 Voltage (Stand-by)	0 to 1.5	V
Voltage Gain	34 MIN.	dB
Input Voltage Level	1 MAX.	$V_{r.m.s.}$

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Quiescent Current	I_{CC}		150	250	mA	V_i = 0
Output Offset Voltage	V_{offset}	−150	0	+150	mV	V_i = 0
Output Power	P_{O1}	32	40		W	R_L = 2 Ω, THD = 10 %
	P_{O2}		45		W	R_L = 2 Ω, THD = 10 %, V_{CC} = 14.4 V
	P_{O3}	20	24		W	R_L = 4 Ω, THD = 10 %
	P_{O4}	25	33		W	R_L = 2 Ω, THD = 1 %
	P_{O5}	15	19		W	R_L = 4 Ω, THD = 1 %
Voltage Gain	A_V		40		dB	P_O = 2 W
Total Harmonic Distortion	THD_1		0.03	0.12	%	R_L = 2 Ω, P_O = 8 W
	THD_2		0.03	0.12	%	R_L = 4 Ω, P_O = 4 W
Output Noise Level	V_n		0.35	0.7	mV	R_G = 10 kΩ, BW = 20 Hz to 20 kHz
Supply Voltage Rejection Ratio	SVR	50	60		dB	R_G = 0, f_{rip} = 100 Hz, V_{rip} = 1.0 V
Input Resistance	R_i	20	30		kΩ	
Roll-off Frequency	f_H	100	250	400	kHz	A_V = −3 dB from 1 kHz Ref High
	f_L		5	10	Hz	A_V = −3 dB from 1 kHz Ref Low
Stand-by Current	$I_{CC(SB)}$		0.05	10	μA	0 ≦ V_7 ≦ 1.5 V

8

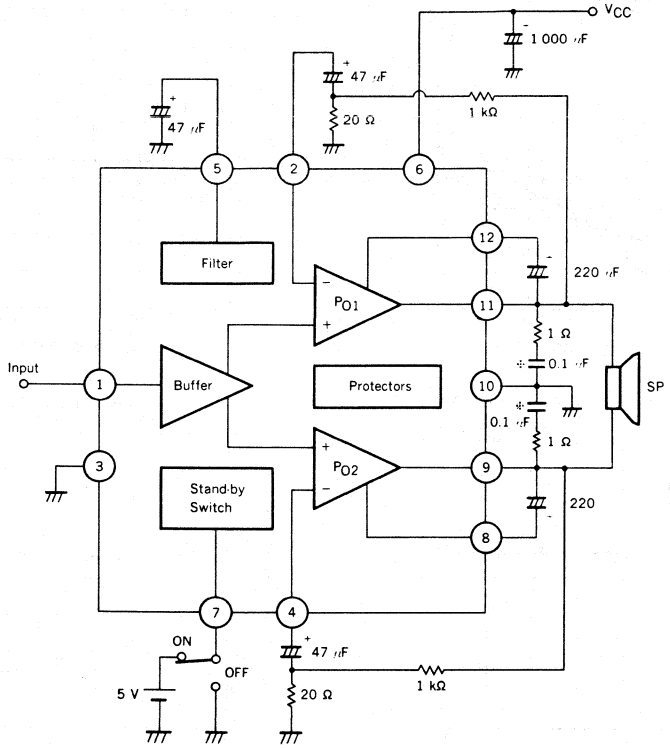
TEST CIRCUIT



SWITCH POSITION

CHARACTERISTIC	SYMBOL	SW 1	SW 2	SW 3
Quiescent Current	I_{CC}	2	2	1
Output Offset Voltage	V_{offset}	2	2	2
Voltage Gain	A_V	1	2	2
Output Power	P_O	1	2	2
Total Harmonic Distortion	THD	1	2	2
Output Noise Level	V_n	2	2	2
Stand-by Current	$I_{CC(SB)}$	2	1	1

TYPICAL APPLICATION



*Mylar Capacitor

INSTRUCTION FOR USE

(1) How to attach the heatsink.

- Surely use the silicon grease.
- Please keep the fastening torque for the screw in the range of 5 to 8 kg-cm.
- Flatness of attached area of heatsink should be kept within 0.1 mm.

(2) When this IC is unstable due to the high impedance of signal source, connect a capacitor (about 1 000 pF) between Pin 1 and Pin 3.

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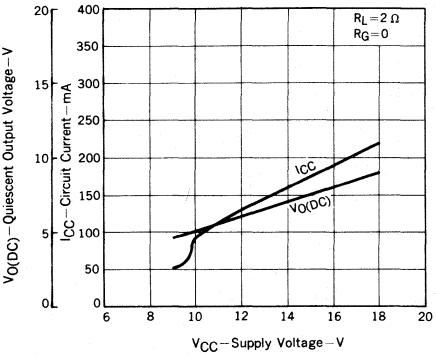
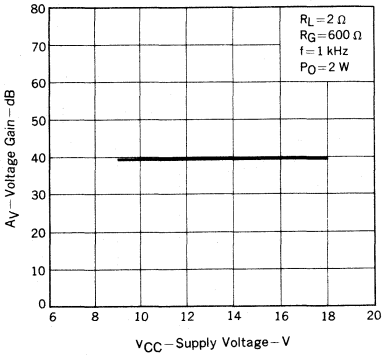
TYPICAL CHARACTERISTICS (T_a = 25 °C)

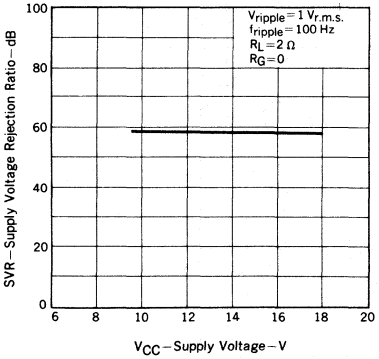
CIRCUIT CURRENT, QUIESCENT OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



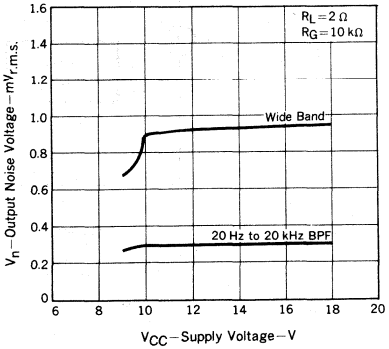
VOLTAGE GAIN vs. SUPPLY VOLTAGE



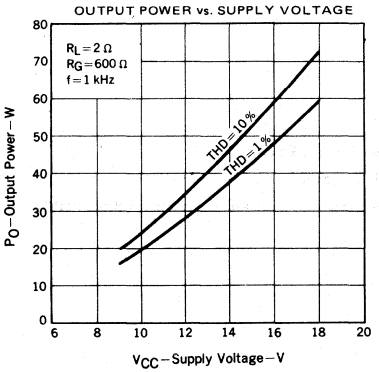
SUPPLY VOLTAGE REJECTION RATIO vs. SUPPLY VOLTAGE



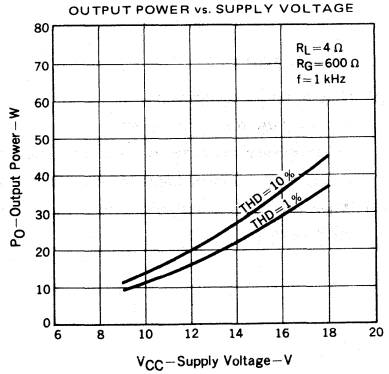
OUTPUT NOISE VOLTAGE vs. SUPPLY VOLTAGE



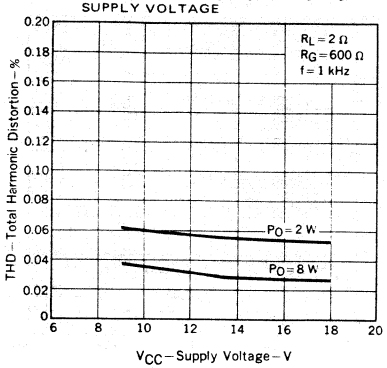
OUTPUT POWER vs. SUPPLY VOLTAGE



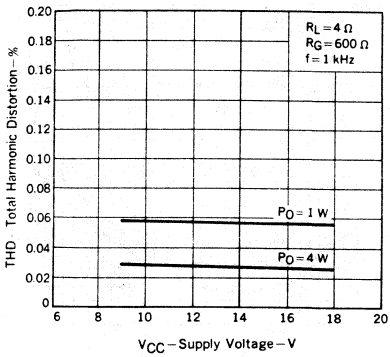
OUTPUT POWER vs. SUPPLY VOLTAGE



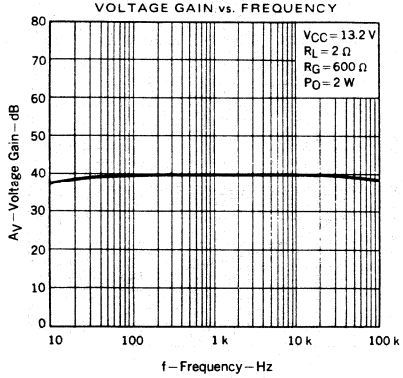
TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



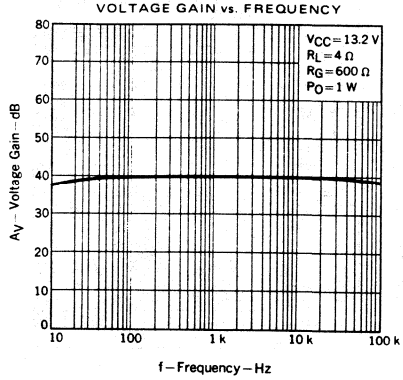
TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



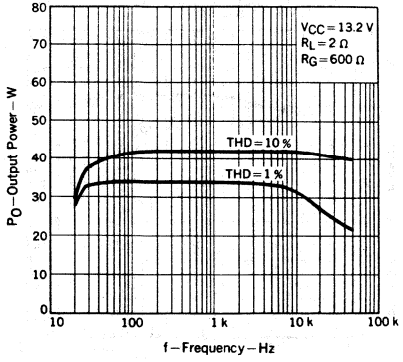
VOLTAGE GAIN vs. FREQUENCY



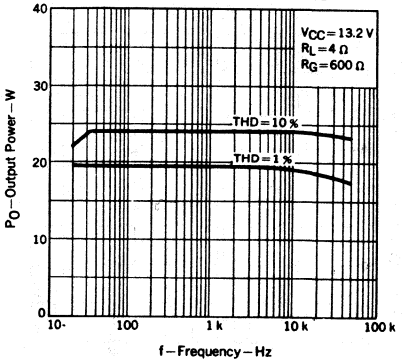
VOLTAGE GAIN vs. FREQUENCY



OUTPUT POWER vs. FREQUENCY



OUTPUT POWER vs. FREQUENCY



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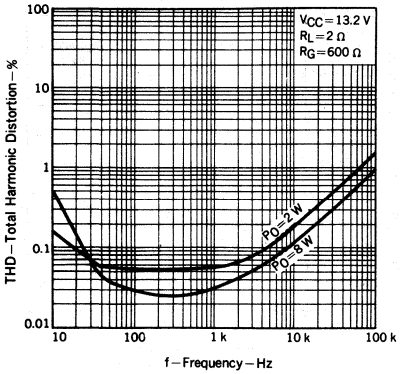
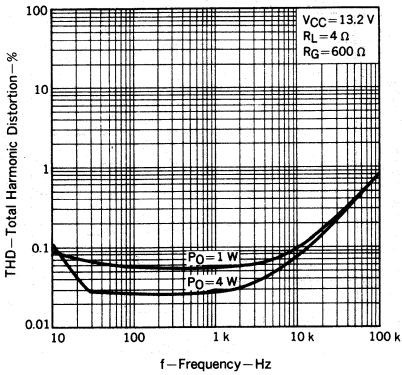
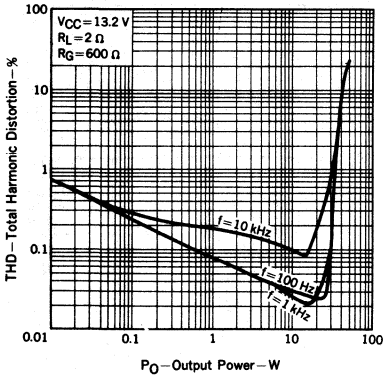
TOTAL HARMONIC DISTORTION vs. FREQUENCY



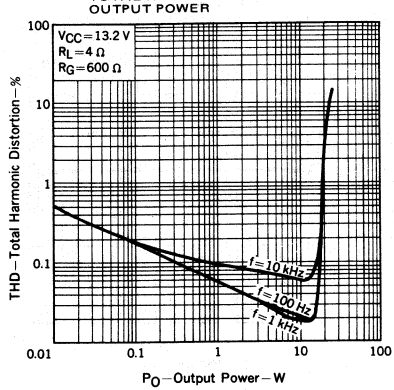
TOTAL HARMONIC DISTORTION vs. FREQUENCY



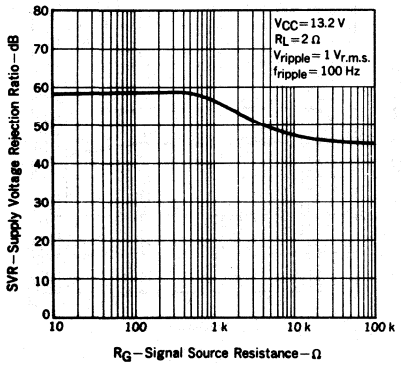
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



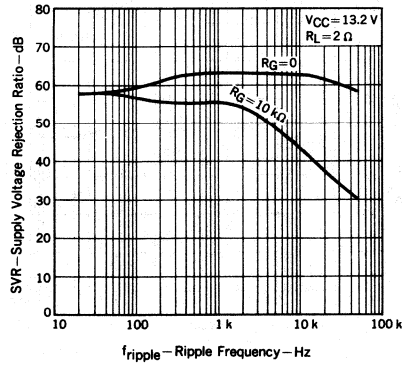
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



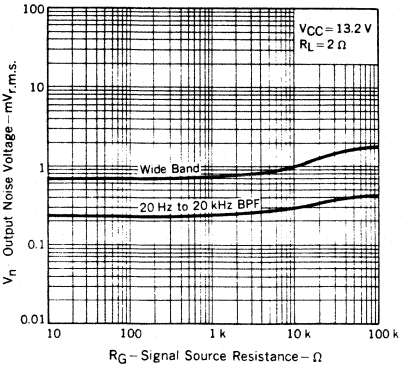
SUPPLY VOLTAGE REJECTION RATIO vs. SIGNAL SOURCE RESISTANCE



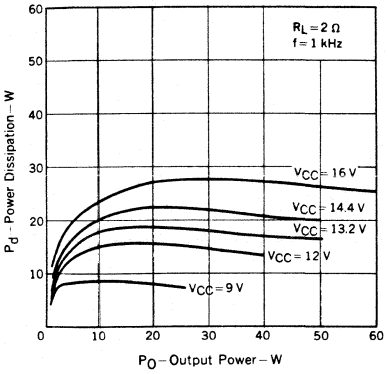
SUPPLY VOLTAGE REJECTION RATIO vs. RIPPLE FREQUENCY



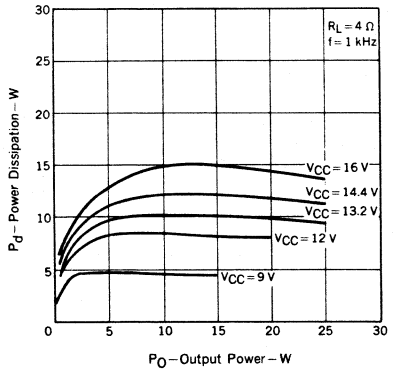
OUTPUT NOISE VOLTAGE vs.
SIGNAL SOURCE RESISTANCE



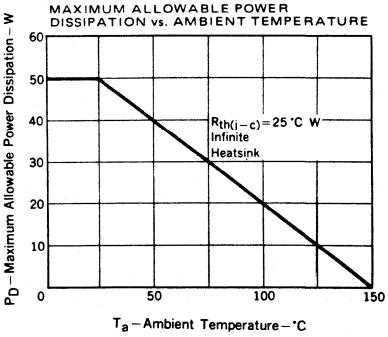
POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



MAXIMUM ALLOWABLE POWER
DISSIPATION vs. AMBIENT TEMPERATURE



18 W AF POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1308V is an audio power amplifier in a 14-lead vertical dual in-line package, specifically designed for car stereo applications.

Typically it provides output power of 18 W at 14.4 V or 15 W at 13.2 V to a 4 Ω load.

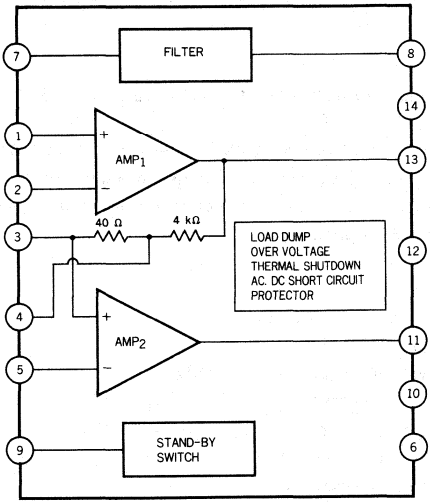
This IC can be used without output capacitors, because its two output terminals have the same potential and it includes an original short circuit protection function which protects internal output power transistors and a speaker at the same time when one output terminal is shorted to ground.

FEATURES

- Internal stand-by switch circuit; CMOS drive possible.
- Can be used as OCL connection.
- Very low output offset voltage : V_{offset} = 150 mV (MAX.)
- High output power : P_O = 18 W (TYP.) @ R_L = 4 Ω, V_{CC} = 14.4 V, THD = 10 %
  P_O = 15 W (TYP.) @ R_L = 4 Ω, V_{CC} = 13.2 V, THD = 10 %
- Very low distortion : THD = 0.1 % (TYP.)
- Following protection circuits are included.
  (1) Load dump voltage surge protection circuit.
  (2) Thermal shut down protection circuit.
  (3) Output terminal short circuit protection circuit. (V_{CC} to OUT, OUT to GND, OUT to OUT)
  (4) Loudspeaker protection circuit.

8

BLOCK DIAGRAM

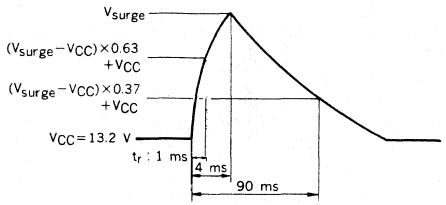


CONNECTION DIAGRAM

PIN No.	CONNECTION	PIN No.	CONNECTION
1	Input $_1$	8	V_{CC}
2	NFB $_1$	9	Stand-by switch
3	GND (Input)	10	NC
4	Output $_1$ Devided	11	Output $_2$
5	NFB $_2$	12	GND (Output)
6	GND (Output)	13	Output $_1$
7	Filter	14	NC

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Note)	$V_{CC\ surge}$	60	V
Supply Voltage (Operational)	V_{CC}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Power Dissipation	P_D	20	W
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C



RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

Supply Voltage Range	9 to 16	V
Load Impedance	3.2 to 16	Ω
Pin 9 Voltage (Operating)	3.5 to V_{CC}	V
Pin 9 Voltage (Stand-by)	0 to 1.5	V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz, Using 4 °C/W heat sink)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Quiescent Current	I_{CC}		90	150	mA	V_i = 0
Output Offset Voltage	V_{offset}		0	±150	mV	V_i = 0
Output Power	P_O		18		W	V_{CC} = 14.4 V, THD = 10 %**
		12	15		W	V_{CC} = 13.2 V, THD = 10 %**
Voltage Gain	A_V	44	46	48	dB	
Total Harmonic Distortion	THD		0.1	0.5	%	P_O = 1 W
Output Noise Level	V_n		0.45	1.5	$mV_{r.m.s.}$	R_G = 10 kΩ, BW = 20 Hz to 20 kHz
Supply Voltage Rejection Ratio	SVR	40	46		dB	R_G = 0, f_{rip} = 100 Hz, V_{rip} = 0.5 V
Input Resistance	R_i	45	65		kΩ	
Roll-off Frequency	f_H		80		kHz	A_V = −3 dB from 1 kHz Ref High
	f_L		10		Hz	A_V = −3 dB from 1 kHz Ref Low
Stand-by Current	$I_{CC(SB)}$		0.32	0.5	mA	0 ≤ V_9 ≤1.5 V

(**Using a Voltmeter: HP-400FL)

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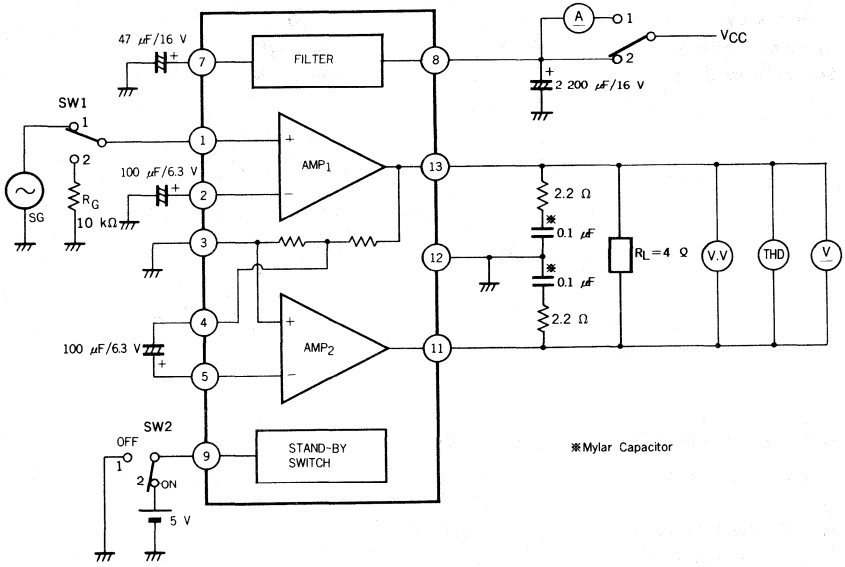
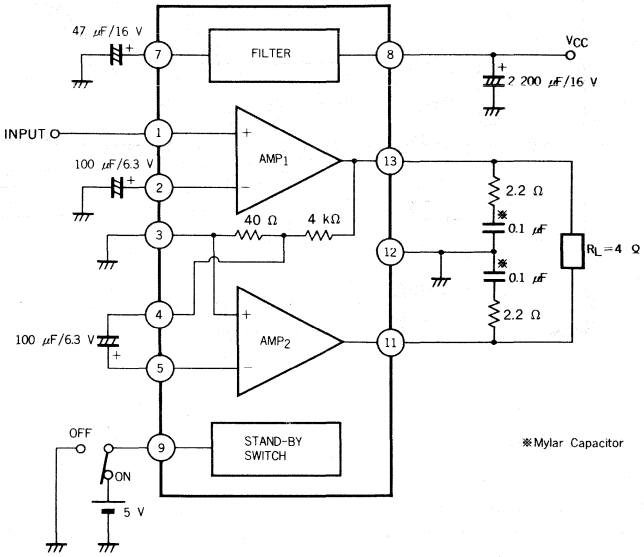
TEST CIRCUIT



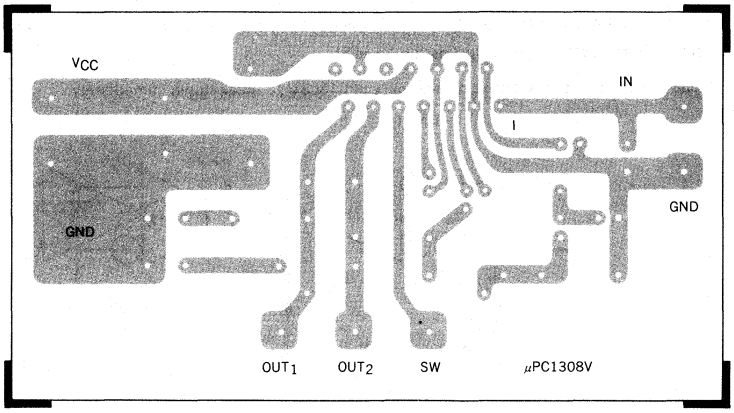
SWITCH POSITION

CHARACTERISTIC	SYMBOL	SW 1	SW 2	SW 3
Quiescent Current	I_{CC}	2	2	1
Output Offset Voltage	V_{offset}	2	2	2
Voltage Gain	A_V	1	2	2
Output Power	P_O	1	2	2
Total Harmonic Distortion	THD	1	2	2
Output Noise Level	V_n	2	2	2
Stand-by Current	$I_{CC(SB)}$	1	1	1

TYPICAL APPLICATION



EXAMPLE FOR PRINTED CIRCUIT BOARD (Copper foil side)



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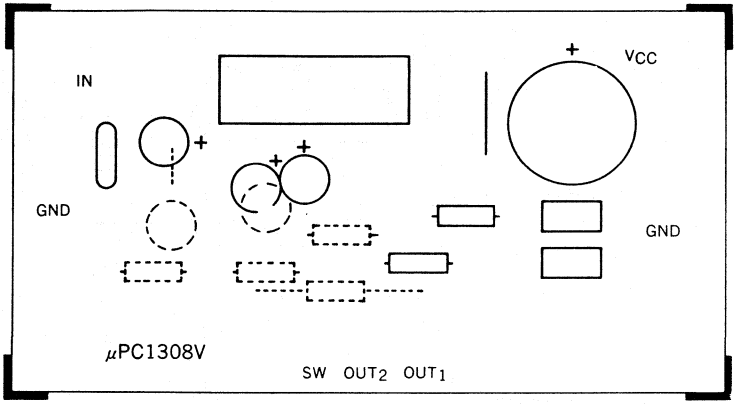
COMPONENT LAYOUT



INSTRUCTION FOR USE

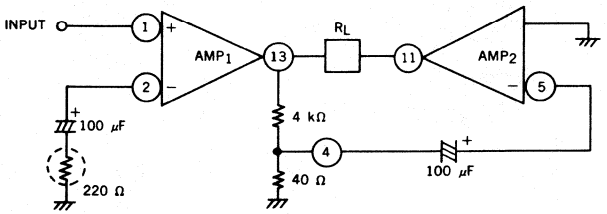
(1) How to attach the heat sink.

- Surely use the silicon grease.
- Please keep the fastening torque for the screw in the range of 5 to 8 kg-cm.
- Flatness of attached area of heat sink should be kept within 0.1 mm.

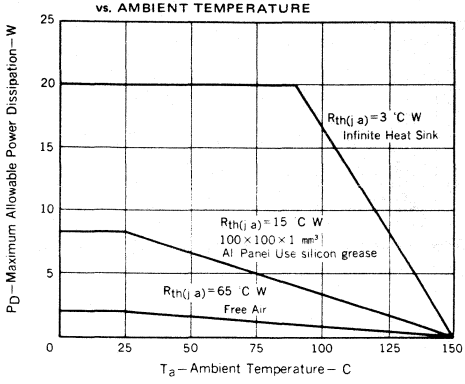
(2) When this IC is unstable due to the high impedance of signal source, connect a capacitor (about 1 000 pF) between Pin 1 and Pin 3.

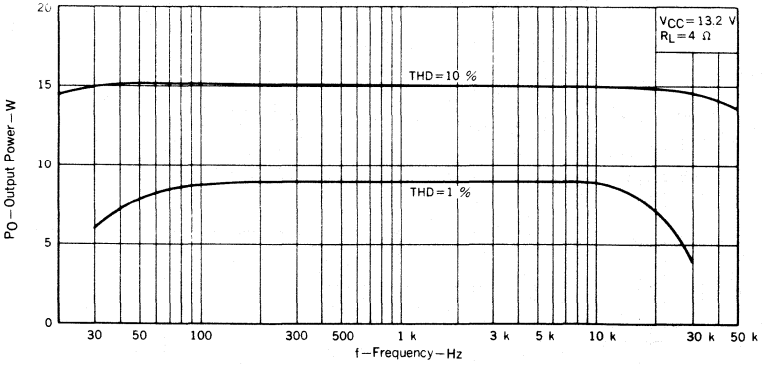
(3) How to decrease voltage gain A_V.
This IC is designed to use A_V of 46 dB but A_V can be set down to 40 dB by modifying the application circuit. The modified point are shown by dotted areas which include additional components. Other external components are as same as in the case of typical application (page 5).

(4) Polarity inversion of the power supply cause μPC1308V to break down immediately.

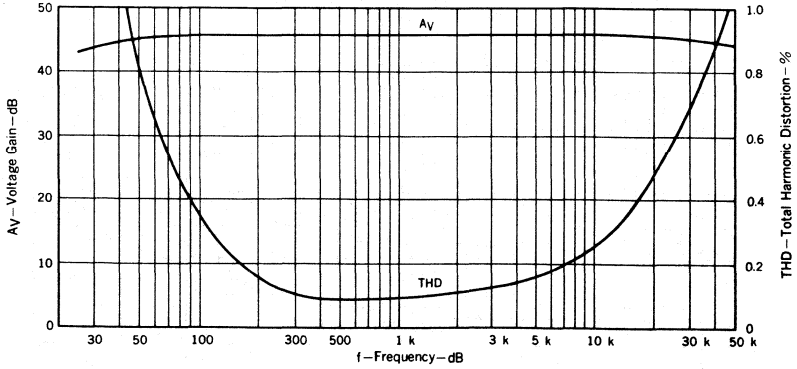


MAXIMUM ALLOWABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE





VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



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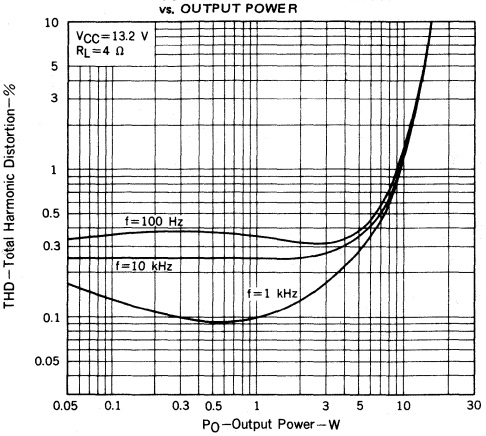
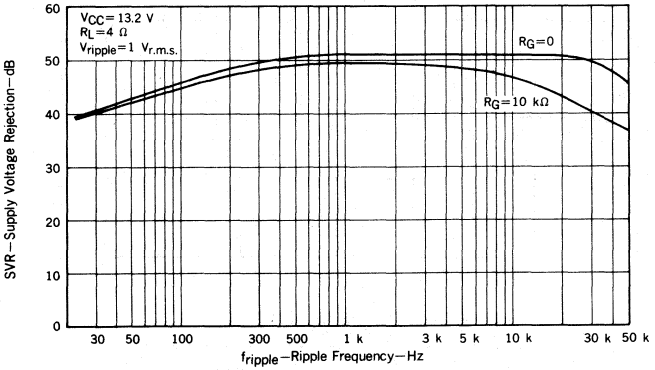
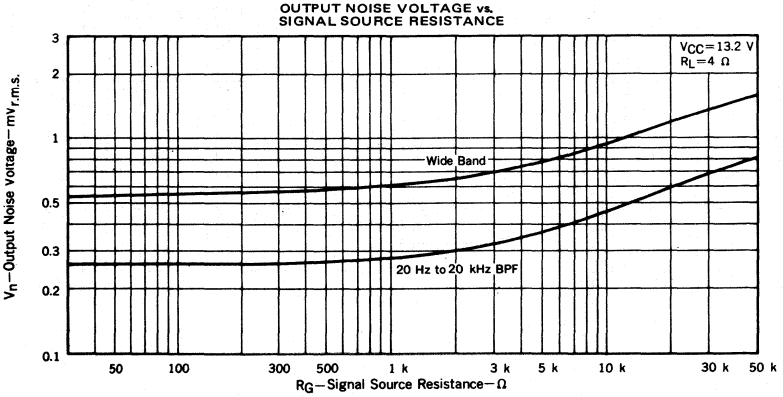
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



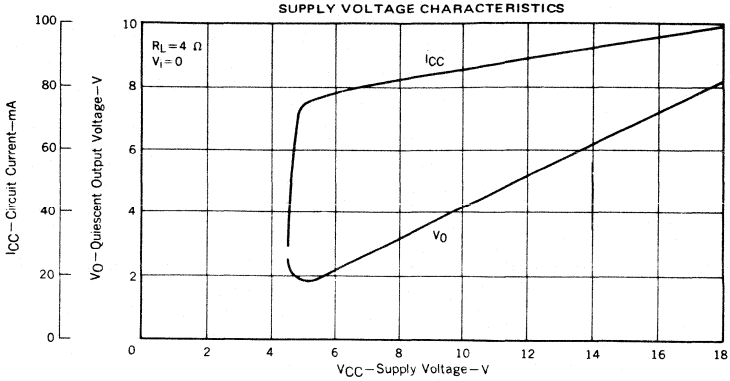
SUPPLY VOLTAGE REJECTION vs.
RIPPLE FREQUENCY



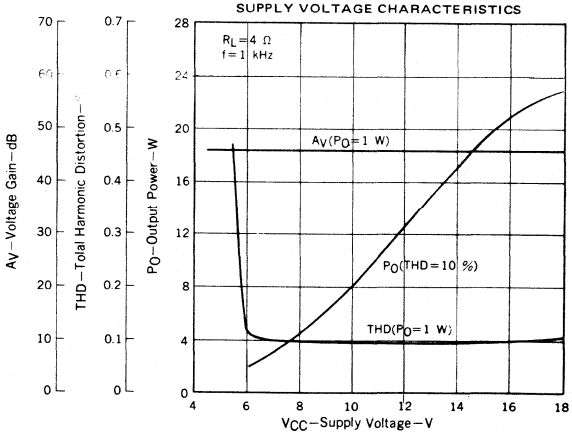
OUTPUT NOISE VOLTAGE vs.
SIGNAL SOURCE RESISTANCE



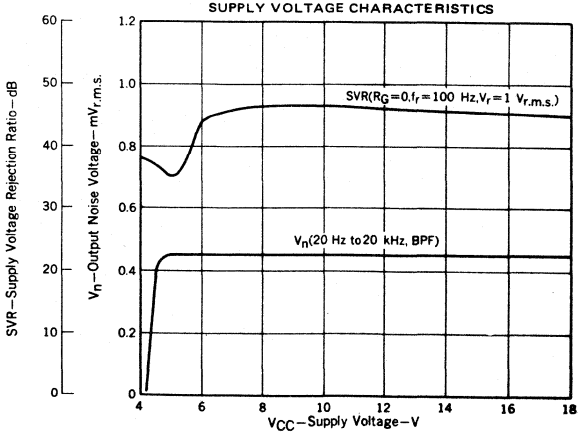
SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE CHARACTERISTICS



8

7 W DUAL AF POWER AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1310V is an audio power amplifier in a 14-lead vertical dual in-line package, specifically designed for car stereo applications.

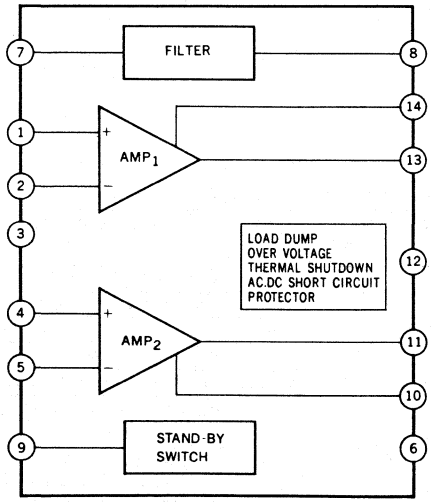
Typically it provides output power of 7 W/CH at 14.4 V or 5.8 W/CH at 13.2 V to a 4 Ω load.

The μPC1310V includes an original short circuit protection function which protects internal output power transistors when an output terminal is shorted to ground or V_{CC}.

FEATURES

- Internal stand-by switch circuit; CMOS drive possible.
- High output power: P_O = 7 W/CH (TYP.) @ R_L = 4 Ω, V_{CC} = 14.4 V, THD = 10 %
  P_O = 5.8 W/CH (TYP.) @ R_L = 4 Ω, V_{CC} = 13.2 V, THD = 10 %
- Very low distortion: THD = 0.1 % (TYP.)
- Following protection circuits are included.
  (1) Load dump voltage surge protection circuit.
  (2) Thermal shut down protection circuit.
  (3) Output terminal short circuit protection circuit. (V_{CC} to OUT, OUT to GND)

BLOCK DIAGRAM



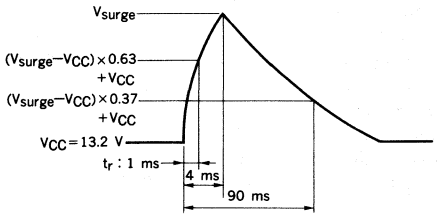
CONNECTION DIAGRAM

PIN No.	CONNECTION
1	Input 1
2	NFB_1
3	GND (Input)
4	Input 2
5	NFB_2
6	GND (Fin)
7	Filter
8	V_{CC}
9	Stand-by switch
10	Bootstrap 2
11	Output 2
12	GND (Output)
13	Output 1
14	Bootstrap 1

8

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Note)	$V_{CC\ surge}$	60*	V
Supply Voltage (Operational)	V_{CC}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Power Dissipation	P_D	20	W
Operating Temperature	T_{opt}	−30 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C



* Surge Pulse Waveform

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

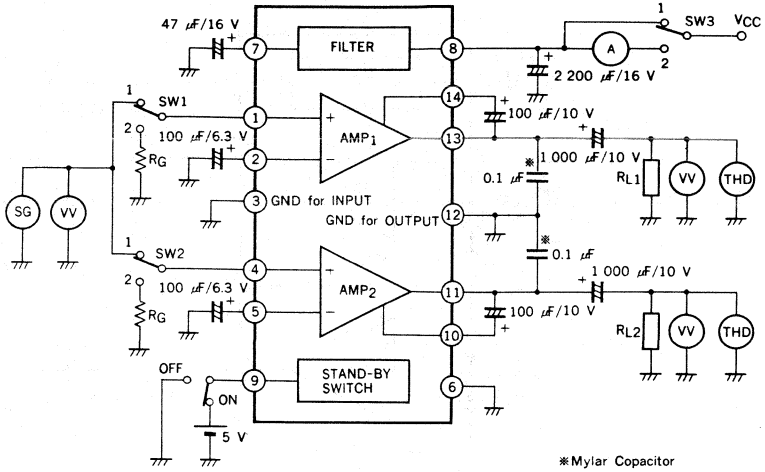
Supply Voltage Range	9 to 16	V
Load Impedance	2 to 8	Ω

ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz, Using 4°C/W heat sink)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Quiescent Current	I_{CC}		100	160	mA	V_{in} = 0
Output Power	P_O		7		W	V_{CC} = 14.4 V, THD = 10 %**
		5	5.8		W	V_{CC} = 13.2 V, THD = 10 %**
Voltage Gain	A_V	50	52	54	dB	
Total Harmonic Distortion	THD		0.1	0.5	%	P_O = 1 W, R_G = 600 Ω
Output Noise Level	V_n		0.8	2.0	$mV_{r.m.s.}$	R_G = 10 kΩ, BW = 20 Hz to 20 kHz
Supply Voltage Rejection Ratio	SVR	35	45		dB	R_G=0, f_{rip}=100 Hz, V_{rip}=1.0 $V_{r.m.s.}$
Input Resistance	R_{in}	45	60		kΩ	
Cross Talk	CT	50	60		dB	P_O = 1 W, R_G (other CH) = 0
Roll-off Frequency	f_H		40		kHz	A_V = −3 dB from 1 kHz Ref High
	f_L		60		Hz	A_V = −3 dB from 1 kHz Ref Low
Pin 9 Voltage	V_9	0		1.5	V	Stand-by
Pin 9 Voltage	V_9	3.5		V_{CC}	V	Operating
Stand-by Current	$I_{CC(SB)}$		0.3	0.5	mA	0 ≤ V9 ≤ 1.5 V

(**Using a Voltmeter: HP-400FL)

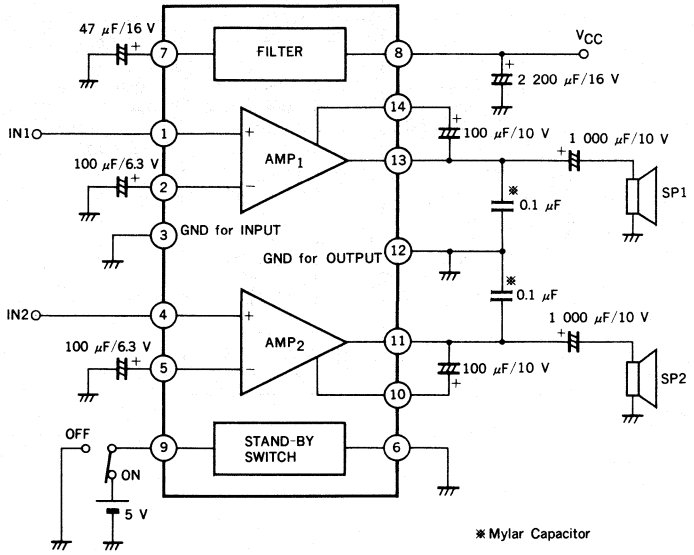
TEST CIRCUIT



SWITCH POSITION

ITEM	SYMBOL	SW1	SW2	SW3
Circuit Current	I_{CC}	2	2	2
Voltage Gain	A_V	1	1	1
Output Power	P_O	1	1	1
Total Harmonic Distortion	THD	1	1	1
Cross Talk	CT	1/2	2/1	1
Output Noise Level	V_n	2	2	1
Supply Voltage Rejection Ratio	SVR	2	2	1

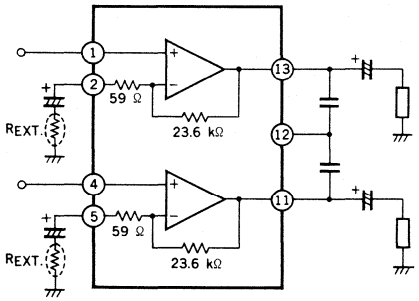
TYPICAL APPLICATION



INSTRUMENT FOR USE

1. How to attach to the heat sink.
   - Surely use the silicon grease.
   - Keep fastening torque for the screw in the range of 5 to 8 kg-cm.
2. When this IC is unstable due to the high impedance of signal source, connect the capacitances (around 1 000 pF) between input terminals (pin #1 and pin #4) and GND for input (pin #3).
3. In pattern layout, connect pin #6 to pin #3 (GND for input), and separate its earth point from that of GND for output (pin #12).
4. The μPC1310V is not recommended for bridge and power booster amplifiers without capacitors because it doesn't include speaker protection circuit. The μPC1318AV is suitable for bridge and power booster amplifiers.
5. How to decrease voltage gain A_V.
   This IC is designed to use A_V of 52 dB so that the external components are most reduced. But A_V can be set down to 40 dB according to the following application. The modified points are shown by dotted circule and they are additional components.

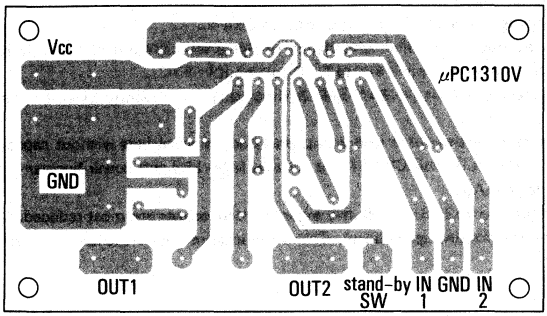
How to decrease voltage gain.



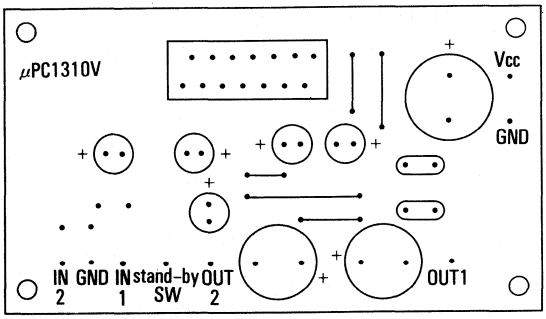
$A_V \fallingdotseq 20 \text{ Log } [23.6 \times 10^3/(59 + R_{EXT.})]$

8

EXAMPLE FOR PRINTED CIRCUIT BOARD (Copper foil side)

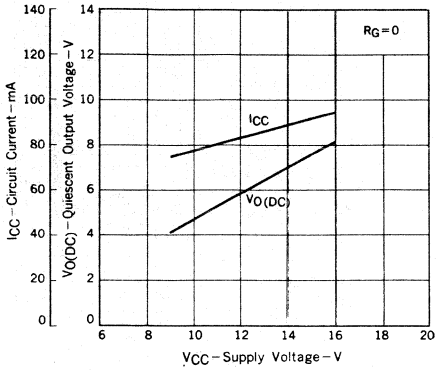


COMPONENT LAYOUT

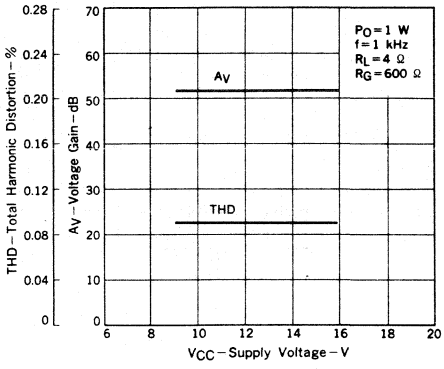


TYPICAL CHARACTERISTICS (T_a = 25 °C)

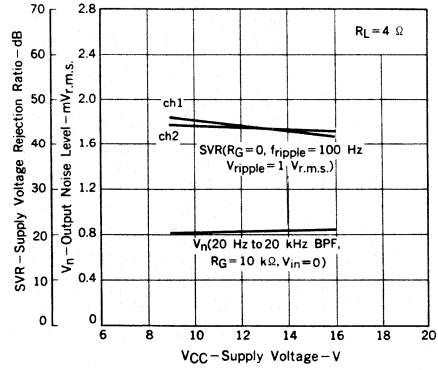
QUIESCENT OUTPUT VOLTAGE, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



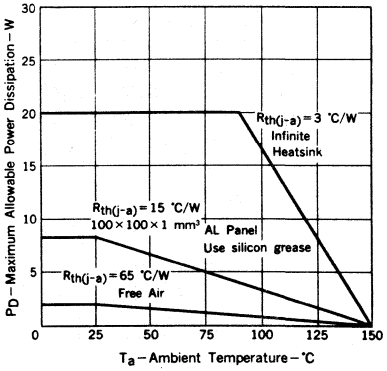
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



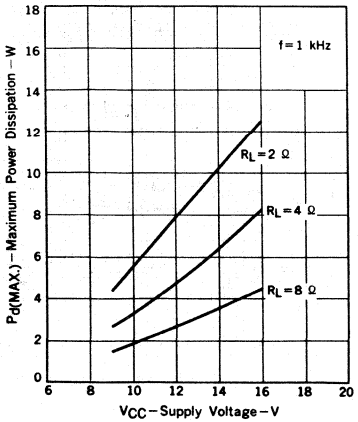
OUTPUT NOISE LEVEL, SUPPLY VOLTAGE REJECTION RATIO vs. SUPPLY VOLTAGE



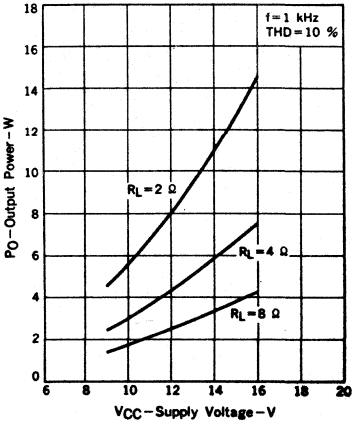
MAXIMUM ALLOWABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE



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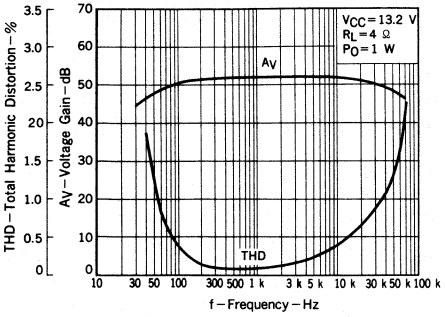
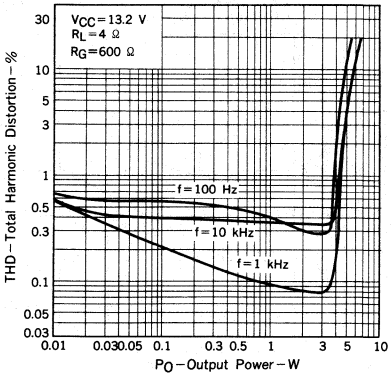
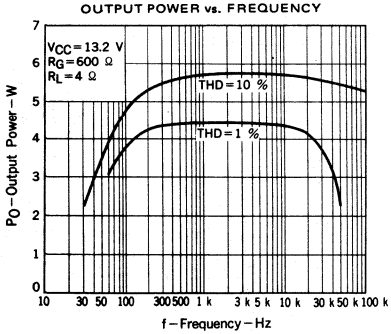
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



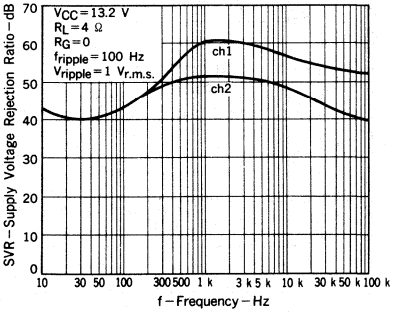
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



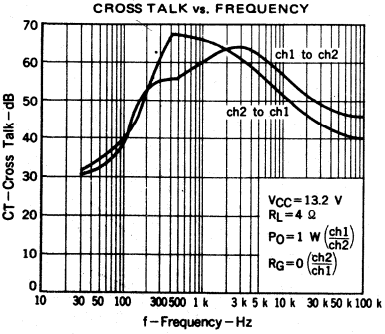
OUTPUT POWER vs. FREQUENCY



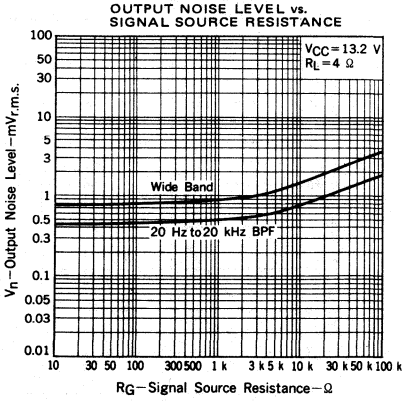
SUPPLY VOLTAGE REJECTION RATIO vs. FREQUENCY



CROSS TALK vs. FREQUENCY



OUTPUT NOISE LEVEL vs. SIGNAL SOURCE RESISTANCE



LOW NOISE DUAL PREAMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

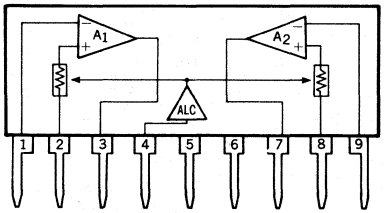
The μPC1313HA is a silicon monolithic integrated circuit and a low noise dual preamplifier with ALC (Automatic Level Control) circuit designed for record and play-back amplifier of stereo portable cassette tape-recorder. Its major features are low noise, low distortion, high gain, large dynamic range and wide supply range.

Outline is a 9-lead single in-line plastic package, for small mounting space on P.C. Board.

FEATURES

- Very low seated height : 5.72 mm MAX.
- High open loop gain : A_{VO} = 90 dB TYP. (f = 1 kHz)
- Low noise : V_{nin} = 1.3 μV TYP. (R_G = 2.2 kΩ NAB)
- Low distortion : THD = 0.05 % TYP. (V_O = 0.3 V)
- Large dynamic range : V_{OM} = 1.8 V TYP. (THD = 1 %)

BLOCK DIAGRAM



CONNECTION DIAGRAM

PIN No.	ELECTRICAL CONNECTION
1	Negative feed back 1
2	Input 1
3	Output 1
4	ALC Input
5	Ground
6	Power Supply
7	Output 2
8	Input 2
9	Negative feed back 2

8

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{CC}	15	V
Package Dissipation	P_D	300*	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

* T_a = 75 °C

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

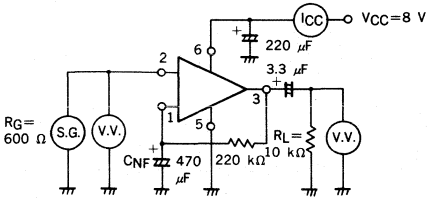
Supply Voltage Range	V_{CC}	4 to 15	V	(PLAY)
	V_{CC}	7.5 to 15	V	(REC. at Application Circuit 1)
	V_{CC}	6.5 to 15	V	(REC. at Application Circuit 2)
	V_{CC}	5.0 to 15	V	(REC. at Application Circuit 3)
Voltage Gain	A_V	46 MIN.	dB	(NAB)
	A_V	40 MIN.	dB	(FLAT)

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 9 V, f = 1 kHz, R_L = 10 kΩ NAB)

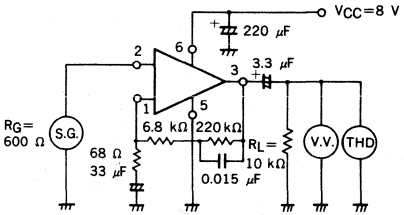
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Quiescent Current	I_{CC}	2.5	4	6	mA	(1)	V_{in} = 0
Open Loop Voltage Gain	A_{VO}	80	90		dB	(1)	V_O = 0.3 V
Voltage Gain	A_V		46		dB	(2)	V_O = 0.3 V
Maximum Output Voltage	V_{OM}	1.2	1.8		V	(2)	THD = 1 %
Total Harmonic Distortion	THD		0.05	0.3	%	(2)	V_O = 0.3 V with 400 pF and 30 kHz 4 pF
Input Impedance	R_i	25	45		kΩ	(2)	
Equivalent Input Noise Voltage	V_{nin}		1.3	4	μV	(3)	R_G = 2.2 kΩ
Cross Talk	CT	−50	−65		dB	(4)	V_O = 1 V, (The other channel V_{in} = 0, R_G = 2.2 kΩ)
ALC Balance	ΔV_{ALC}		0	2.5	dB	(6)	V_{in} = −50 dBV
ALC THD	THD_{ALC}		0.2	1	%	(5)	V_{in} = −50 dBV
ALC	ALC	40	46		dB	(5)	from V_{in} = −70 dBV to become THD = 10 %

TEST CIRCUITS

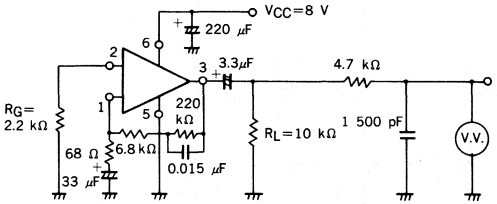
(1) I_{CC}, A_{VO} test circuit



(2) A_V, V_{OM}, THD, Z_{in} test circuit (for CH1)

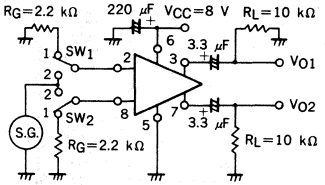


(3) V_{nin} test circuit (for CH1)



AV f=1 kHz

(4) Cross talk, Channel balance test circuit



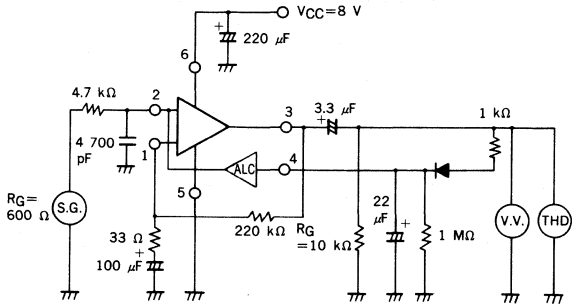
NOTE 1: External components of the IC are the same as the test circuit (2).

2: Cross talk procedure
Switch position SW.1 → 2, SW.2 → 1, 20 log V_{o2}/V_{o1}
Switch position SW.1 → 1, SW.2 → 2, 20 log V_{o1}/V_{o2}

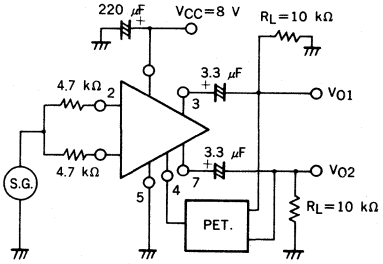
3: Channel balance
Switch position SW.1 → 2, SW.2 → 2, 20 log V_{o1}/V_{o2}

8

(5) THD_{ALC}, ALC test circuit (for CH1)



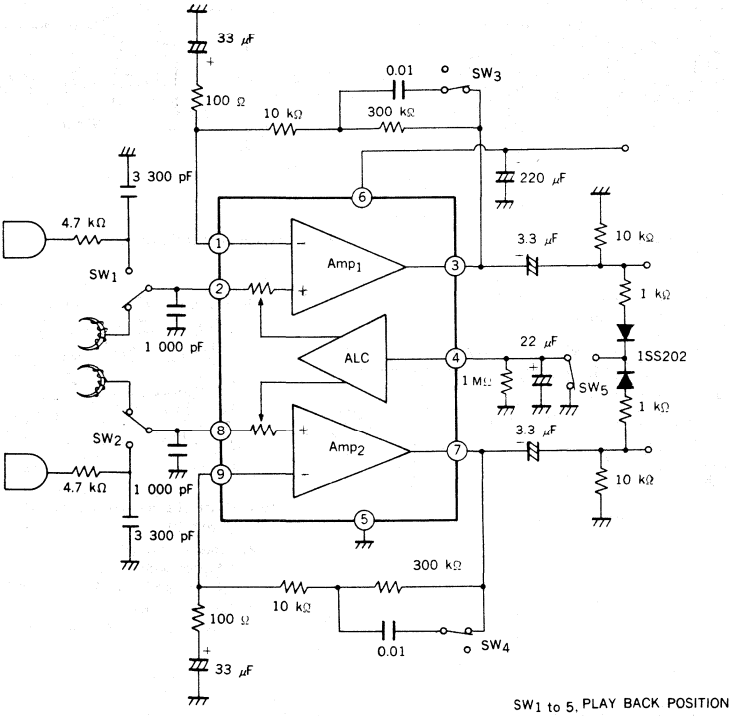
(6) ALC balance test circuit



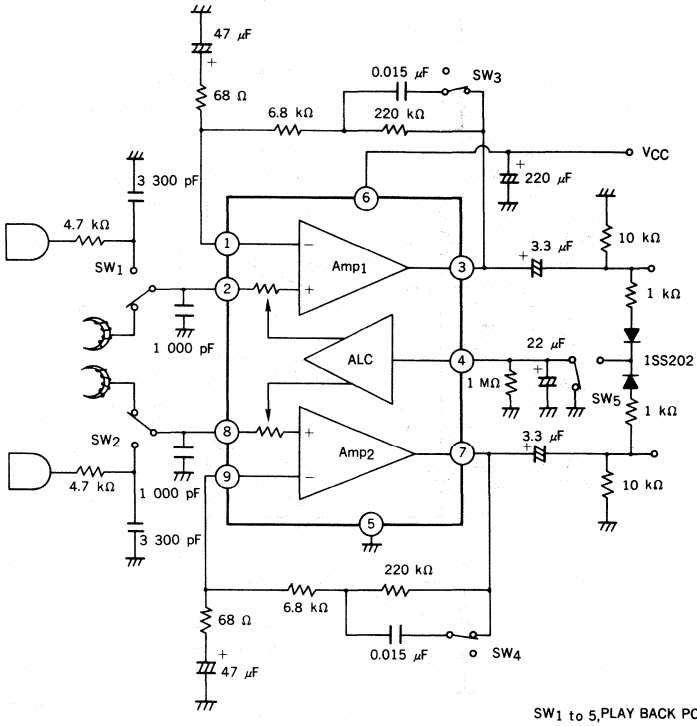
NOTE 1: External components of the IC are the same as test circuit (5).

2: ALC balance: 20 log V_{o1}/V_{o2}

APPLICATION CIRCUIT 1 (V_{CC} = 7.5 to 15 V)



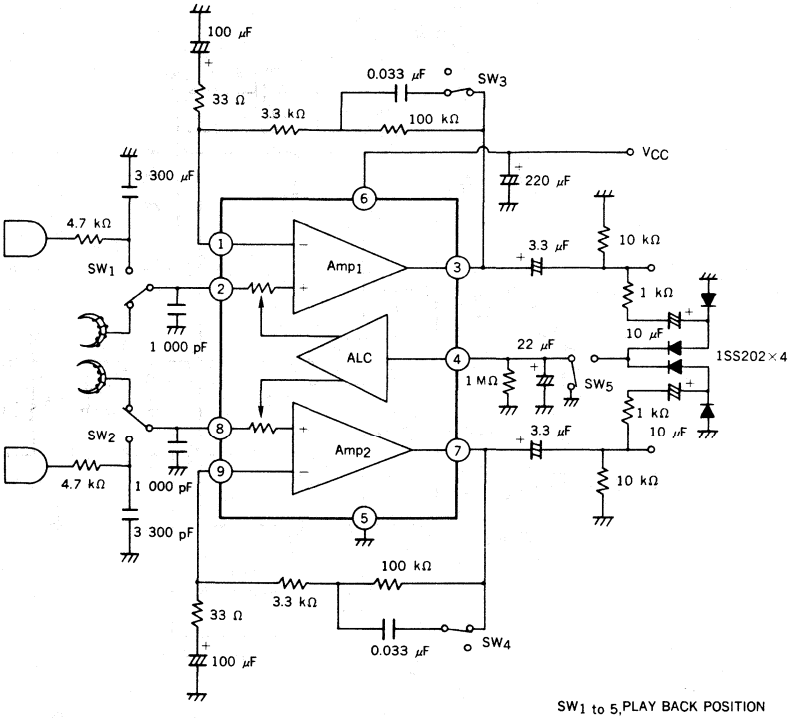
APPLICATION CIRCUIT 2 (V_{CC} = 6.5 to 15 V)



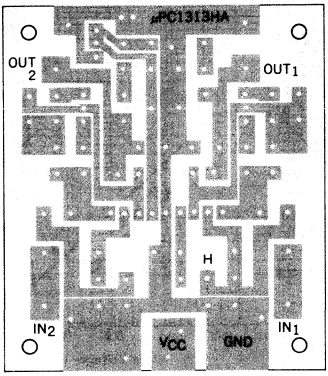
SW_1 to 5,PLAY BACK POSITION

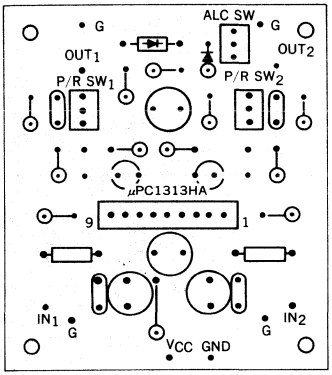
8

APPLICATION CIRCUIT 3 (5.0 V to 15 V)



TYPICAL PCB

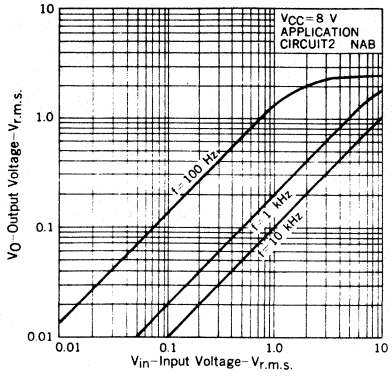




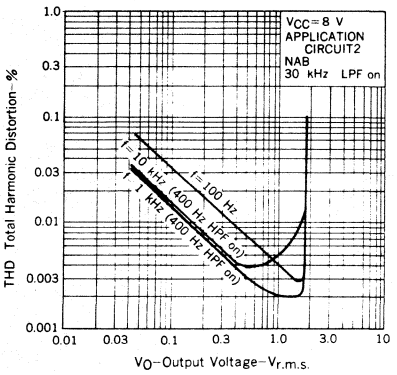
(COPPER SIDE)

TYPICAL CHARACTERISTICS (T_a = 25 °C)

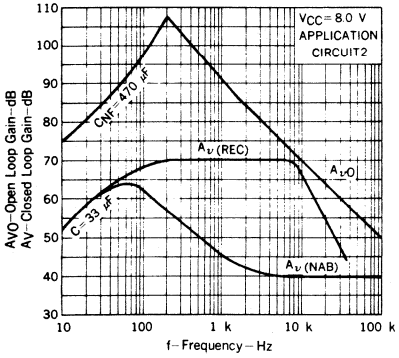
OUTPUT VOLTAGE vs. INPUT VOLTAGE



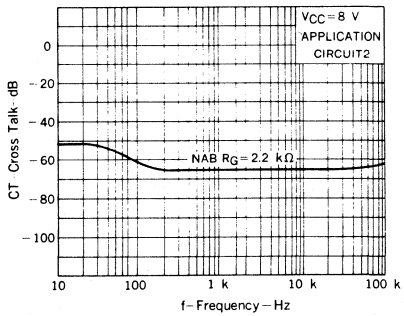
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE



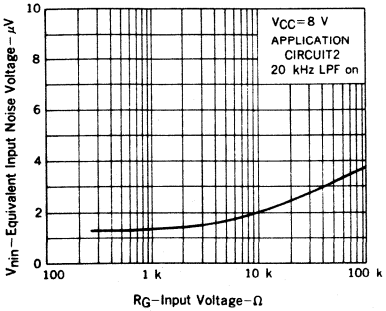
OPEN AND CLOSED LOOP GAIN vs. FREQUENCY



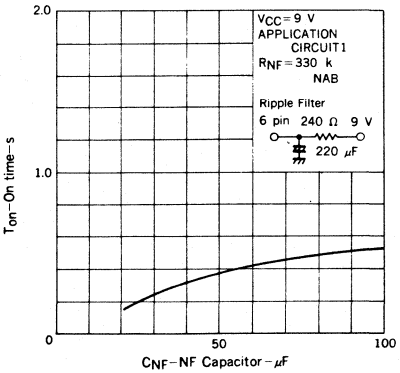
CROSS TALK vs. FREQUENCY



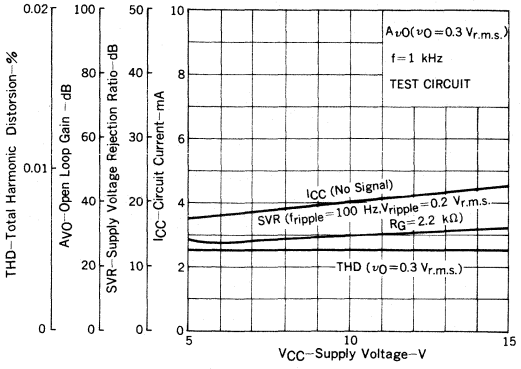
EQUIVARENT INPUT VOLTAGE vs. INPUT RESISTANCE



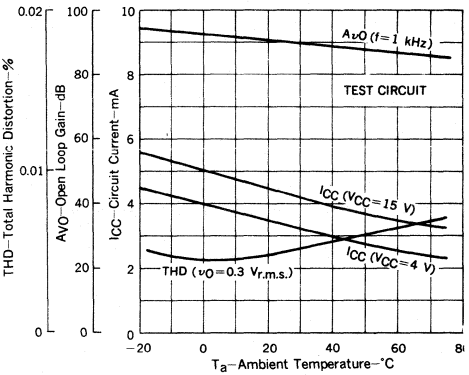
ON TIME vs. NF CAPACITOR



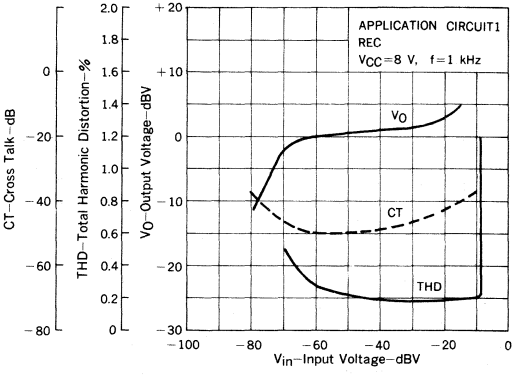
TOTAL HARMONIC DISTORTION, OPEN LOOP GAIN, SUPPLY VOLTAGE REJECTION RATIO, CIRCUIT CURRENT vs. SUPPLY VOLTAGE



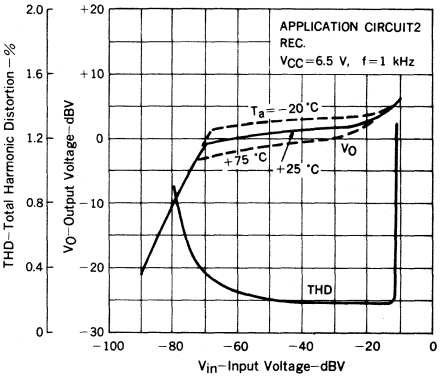
TOTAL HARMONIC DISTORTION, OPEN LOOP GAIN, CIRCUIT CURRENT vs. AMBIENT TEMPERATURE



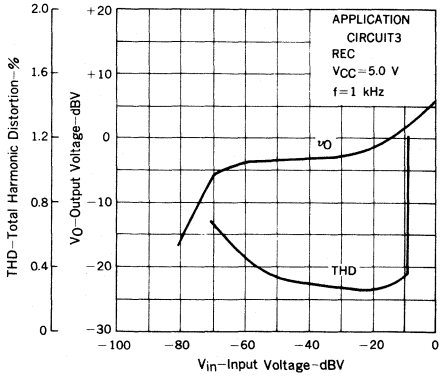
CROSS TALK, TOTAL HARMONIC DISTORTION, OUTPUT VOLTAGE vs. INPUT VOLTAGE



TOTAL HARMONIC DISTORTION, OUTPUT VOLTAGE vs. INPUT VOLTAGE



TOTAL HARMONIC DISTORTION, OUTPUT VOLTAGE vs. INPUT VOLTAGE



8

DUAL AUDIO POWER AMPLIFIER

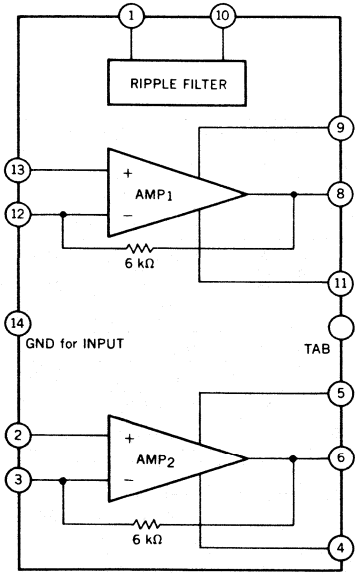
DESCRIPTION

The μPC1316C is a dual audio power amplifier in a 14-lead dual in line plastic package, and designed for portable audio sets.

FEATURES

- Wide operating voltage range. V_{CC} = 3 to 16 V
- High output power. P_O = 2 W TYP. @ 12 V / 8 Ω / 10 %
  P_O = 1.6 W TYP. @ 9 V / 4 Ω / 10 %
  P_O = 1.2 W TYP. @ 9 V / 8 Ω / 10 %
  P_O = 0.7 W TYP. @ 6 V / 4 Ω / 10 %
  P_O = 0.5 W TYP. @ 6 V / 8 Ω / 10 %
  P_O = 80 mW @ 4.5 V / 32 Ω / 10 %
  (V_{CC} / R_L / THD)
- High supply voltage rejection. SVR = 45 dB
- Low quiescent current. I_{CC} = 12 mA
- Easy assembly so that two power amplifiers are built in a package.
- Low pop noise at power switch on and off.

BLOCK DIAGRAM



CONNECTION DIAGRAM

PIN NO	CONNECTION
1	Filter
2	Input 2
3	NFB 2
4	Compensation 2
5	Bootstrap 2
6	Output 2
7	NC
TAB	GND
8	Output 1
9	Bootstrap 1
10	V_{CC}
11	Compensation 1
12	NFB 1
13	Input 1
14	GND

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (No Signal)	V_{CC1}	18	V
Supply Voltage (Operating)	V_{CC2}	16	V
Power Dissipation	P_D	2.4 *	W
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +150	°C

* 50 x 50 x 0.035 mm Copper heat sink on PCB

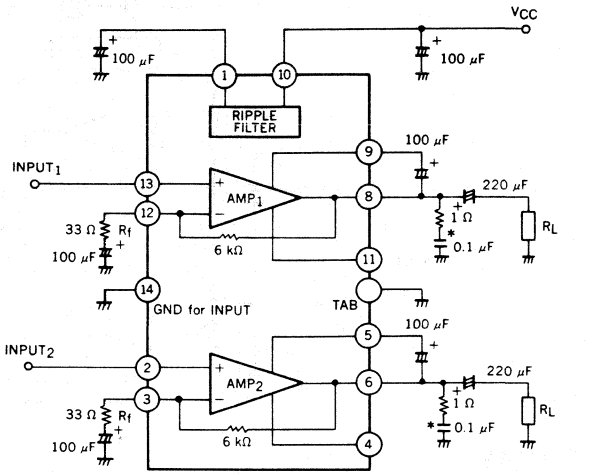
RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage (R_L=16 Ω)	V_{CC} (16)	3		16	V
Supply Voltage (R_L=8 Ω)	V_{CC} (8)	3		13	V
Supply Voltage (R_L=4 Ω)	V_{CC} (4)	3		9	V
Load Impedance	R_L	4	8		Ω
Voltage Gain	A_v	34	44		dB

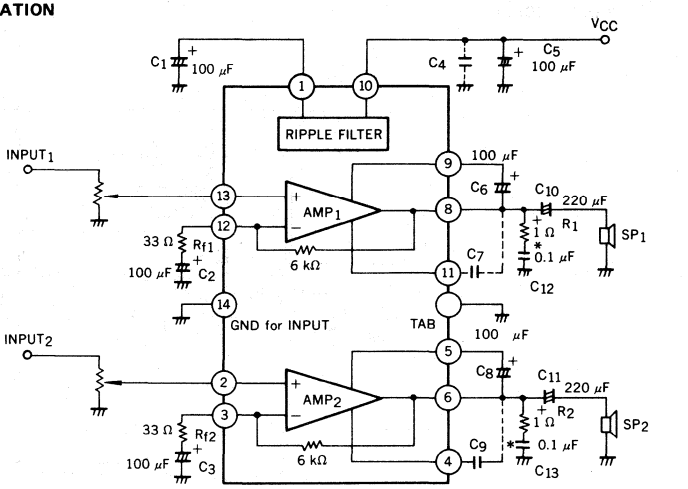
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)
(V_{CC}=9 V, R_f=33 Ω, f=1 kHz, R_L=8 Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Circuit Current	I_{CC}		12	25	mA	No Signal
Voltage Gain	A_{v1}	41	44	47	dB	P_O=0.25 W, R_f=33 Ω
	A_{v2}		34		dB	P_O=0.25 W, R_f=120 Ω
Output Power	P_{O1}		2		W	V_{CC}=12 V, R_L=8 Ω, THD = 10 %
	P_{O2}		1.6		W	V_{CC}=9 V, R_L=4 Ω, THD = 10 %
	P_{O3}	0.9	1.2		W	V_{CC}=9 V, R_L=8 Ω, THD = 10 %
	P_{O4}		0.7		W	V_{CC}=6 V, R_L=4 Ω, THD = 10 %
	P_{O5}		0.5		W	V_{CC}=6 V, R_L=8 Ω, THD = 10 %
	P_{O6}		80		mW	V_{CC}=4.5 V, R_L=32 Ω, THD = 10 %
Total Harmonic Distortion	THD1		0.4	1.6	%	P_O=0.5 W, R_f=33 Ω
	THD2		0.3		%	P_O=0.5 W, R_f=120 Ω
Output Noise Voltage	NL		0.9	1.5	$mV_{r.m.s.}$	R_G=10 kΩ
Supply Voltage Rejection	SVR	36	45		dB	R_G=0, f(ripple)=100 Hz, V(ripple)=0.3 $V_{r.m.s.}$
Cross Talk	CT	40	55		dB	R_G=0, P_O=0.25 W
Channel Balance	ChB	−2	0	2	dB	P_O=0.25 W
Input Impedance	Z_{in}		5		MΩ	

TEST CIRCUIT



TYPICAL APPLICATION

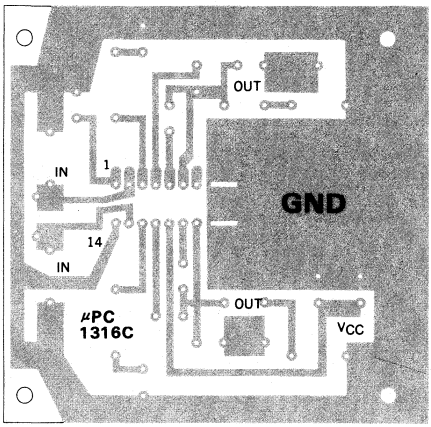


* Mylar Capacitor

NOTE FOR USE

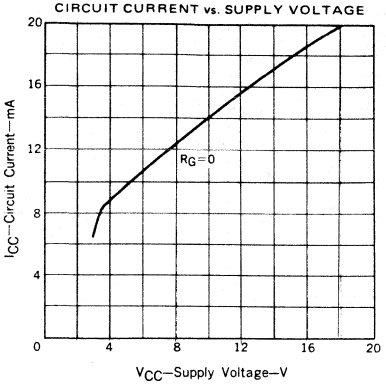
(1) Mylar capacitor is recommended as C_{12}, C_{13}.
(2) Add C_7, C_9, in the case of reducing voltage gain at high frequency.
(3) Add C_4 or increase capacitance of C_{12}, C_{13} when a oscillation may occur due to the pattern layout on PCB.
(4) Voltage gain can be changed by value of R_{f1}, R_{f2}, The voltage gain should be set more than 34 dB.
(5) When a input capacitor is connected the input terminal, a bias resistor should be connected between its terminal and GND.

EXAMPLE FOR PRINTED CIRCUIT BOARD (Copper foil side)

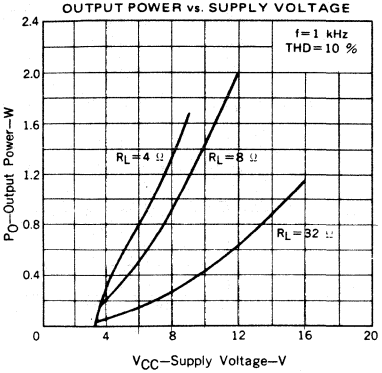


TYPICAL CHARACTERISTICS (T_a = 25 °C)

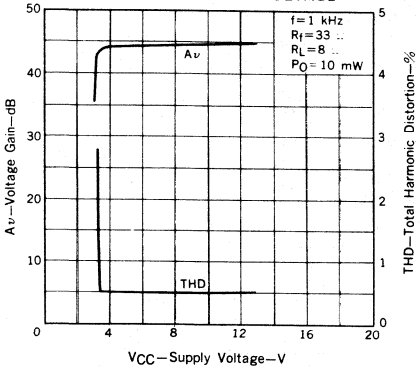
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



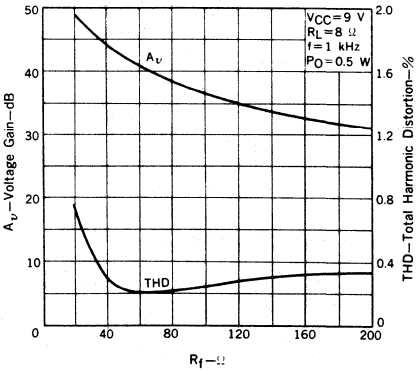
OUTPUT POWER vs. SUPPLY VOLTAGE



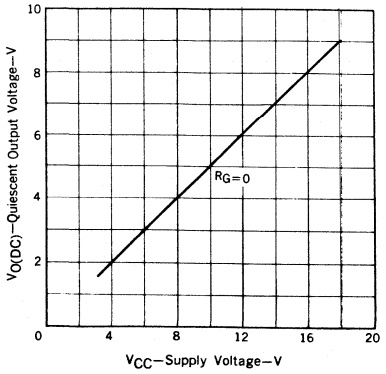
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



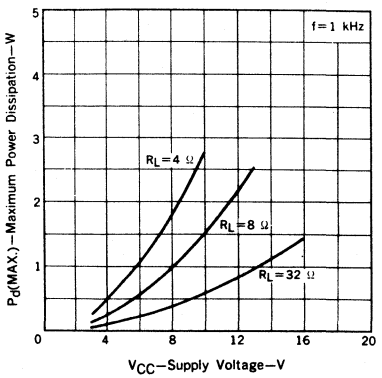
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. R_f



QUIESCENT OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE



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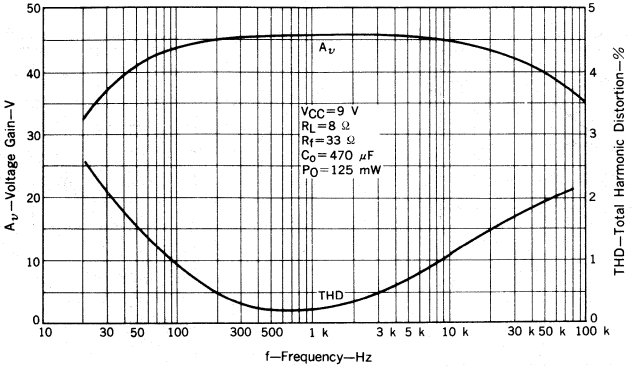
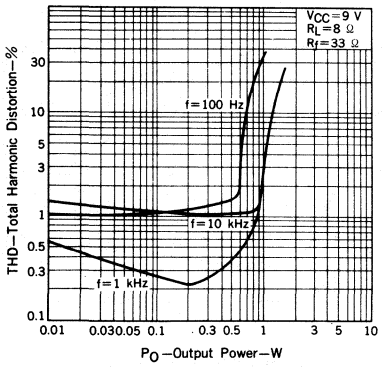
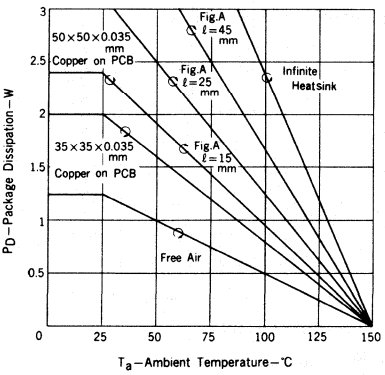
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY

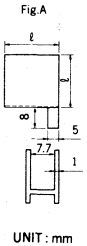


TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



PACKAGE DISSIPATION vs. AMBIENT TEMPERATURE





23 W AF POWER AMPLIFIER

DESCRIPTION

The μPC1318AV is an audio power amplifier in a 14-lead vertical dual in-line package, specifically designed for car stereo applications.

Typically it provides output power of 23 W at 14.4 V or 20 W at 13.2 V to a 4 Ω load.

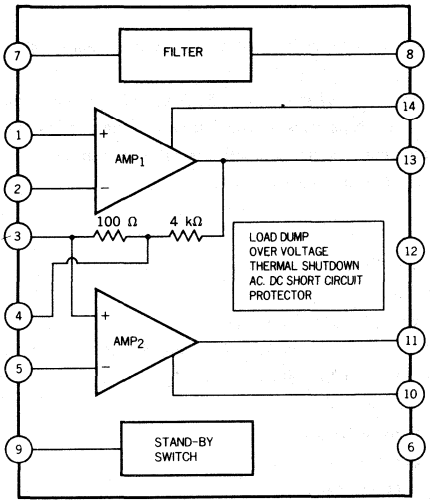
This IC can be used without output capacitors, because its two output terminals have the same potential and it includes original short circuit protection function which protects internal output power transistors and a speaker at the same time when one output terminal is shorted to ground or V_{CC}.

FEATURES

- Internal stand-by switch circuit; CMOS drive possible.
- Can be used as OCL connection.
- Very low output offset voltage : V_{offset} = 150 mV (MAX.)
- High output power : P_O = 23 W (TYP.) @ R_L = 4 Ω, V_{CC} = 14.4 V, THD = 10 %
  P_O = 20 W (TYP.) @ R_L = 4 Ω, V_{CC} = 13.2 V, THD = 10 %
- Very low distortion : THD = 0.06 % (TYP.)
- Following protection circuits are included.
  (1) Load dump voltage surge protection circuit.
  (2) Thermal shut down protection circuit.
  (3) Output terminal short circuit protection circuit. (V_{CC} to OUT, OUT to GND, OUT to OUT)
  (4) Loudspeaker protection circuit.

8

BLOCK DIAGRAM



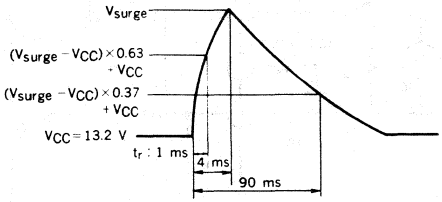
CONNECTION DIAGRAM

PIN NO.	CONNECTION	PIN NO.	CONNECTION
1	Input $_1$	8	V_{CC}
2	NFB $_1$	9	Stand-by switch
3	GND (Input)	10	Bootstrap $_2$
4	Output $_1$ Devided	11	Output $_2$
5	NFB $_2$	12	GND (Output)
6	GND	13	Output $_1$
7	Filter	14	Bootstrap $_1$

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Note)	$V_{CC\ surge}$	60*	V
Supply Voltage (Operational)	V_{CC}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Power Dissipation	P_D	20	W
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*



Surge Pulse Waveform

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

Supply Voltage Range	9 to 16	V
Load Impedance	3.2 to 16	Ω
Pin 9 Voltage (Operating)	3.5 to V_{CC}	V
Pin 9 Voltage (Stand-by)	0 to 1.5	V
Voltage Gain	34 MIN.	dB

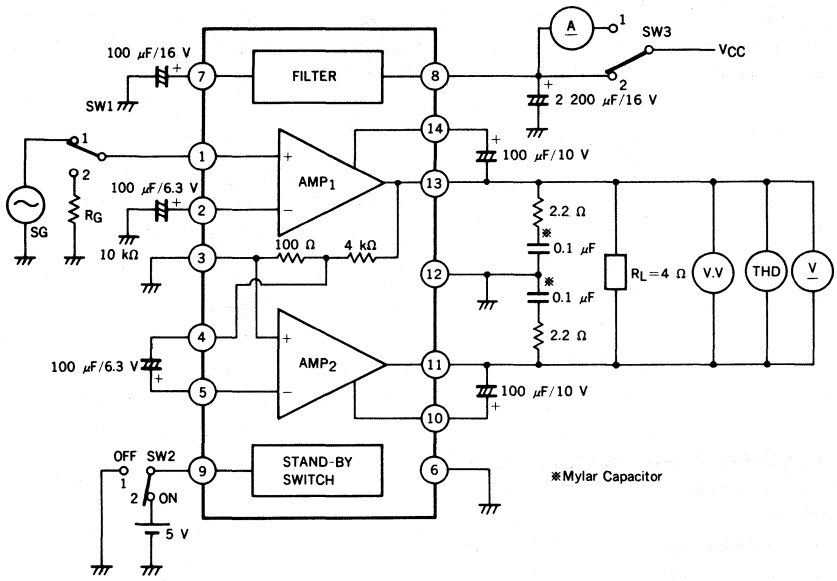
ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz, Using 4 °C/W heatsink)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Quiescent Current	I_{CC}		120	150	mA	V_i = 0
Output Offset Voltage	V_{offset}		0	±150	mV	V_i = 0
Output Power	P_O		23		W	V_{CC} = 14.4 V, THD = 10 %**
		16	20		W	V_{CC} = 13.2 V, THD = 10 %**
Voltage Gain	A_v	38	40	42	dB	P_O = 1 W
Total Harmonic Distortion	THD		0.06	0.3	%	P_O = 1 W
Output Noise Level	V_n		0.24	0.8	mV	R_G = 10 kΩ, BW = 20 Hz to 20 kHz
Supply Voltage Rejection Ratio	SVR	40	52		dB	R_G = 0, f_{rip} = 100 Hz, V_{rip} = 1.0 V
Input Resistance	R_i	45	60		kΩ	
Roll-off Frequency	f_H		160		kHz	A_v = −3 dB from 1 kHz Ref High
	f_L		10		Hz	A_v = −3 dB from 1 kHz Ref Low
Stand-by Current	$I_{CC(SB)}$		0.4	0.6	mA	$0 \leqq V_9 \leqq 1.5$ V

(**Using a Voltmeter: HP-400FL)

8

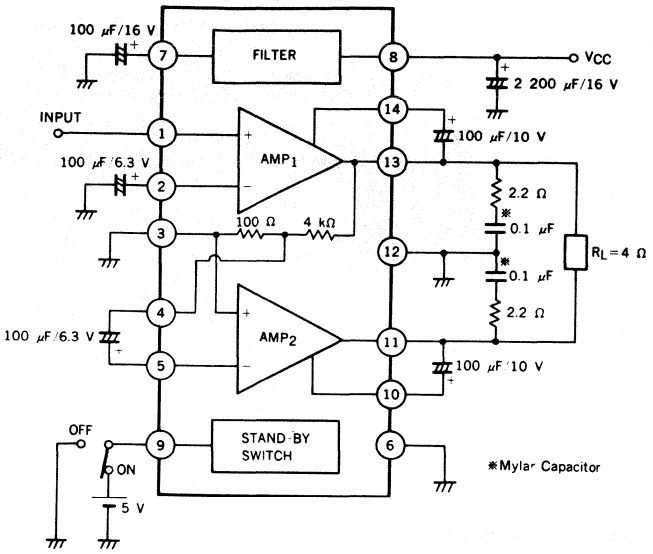
TEST CIRCUIT



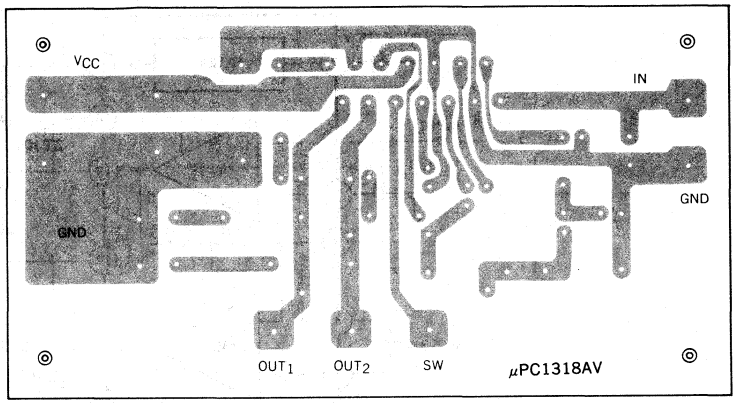
SWITCH POSITION

CHARACTERISTIC	SYMBOL	SW 1	SW 2	SW 3
Quiescent Current	I_{CC}	2	2	1
Output Offset Voltage	V_{offset}	2	2	2
Voltage Gain	A_V	1	2	2
Output Power	P_O	1	2	2
Total Harmonic Distortion	THD	1	2	2
Output Noise Level	V_n	2	2	2
Stand-by Current	$I_{CC(SB)}$	1	1	1

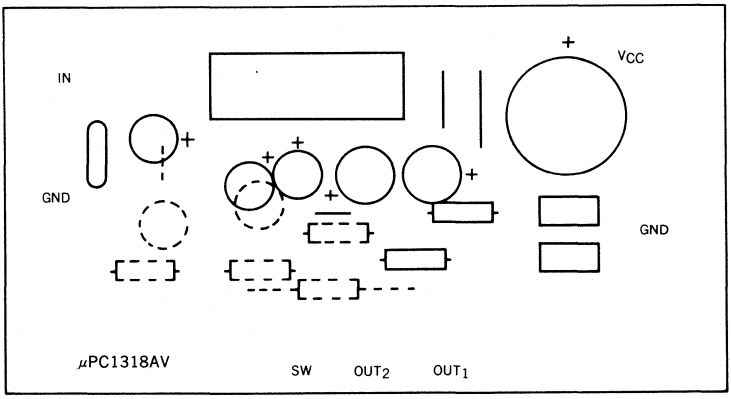
TYPICAL APPLICATION



EXAMPLE FOR PRINTED CIRCUIT BOARD (Copper foil side)



COMPONENT LAYOUT



INSTRUCTION FOR USE

(1) How to attach the heatsink.

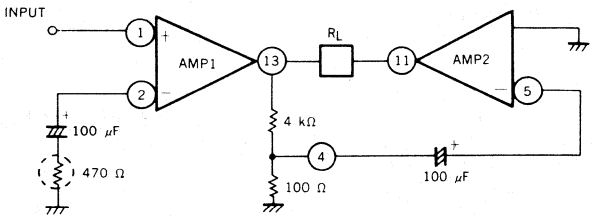
- Surely use the silicon grease.
- Please keep the fastening torque for the screw in the range of 5 to 8 kg-cm.
- Flatness of attached area of heatsink should be kept within 0.1 mm.

(2) When this IC is unstable due to the high impedance of signal source, connect a capacitor (about 1 000 pF) between Pin 1 and Pin 3.

(3) How to decrease voltage gain A_V.

This IC is designed to use A_V of 40 dB but A_V can be set down to 34 dB by modifying the application circuit. The modified point are shown by dotted areas which include additional component. Other external components are as same as in the case of typical application (page 5).

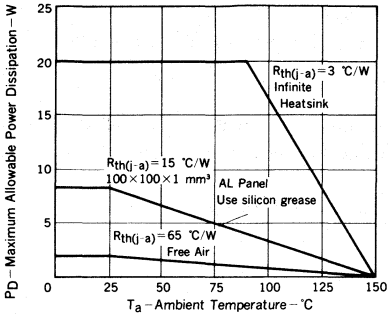
(4) Polarity inversion of the power supply cause μPC1318AV to break down immediately.



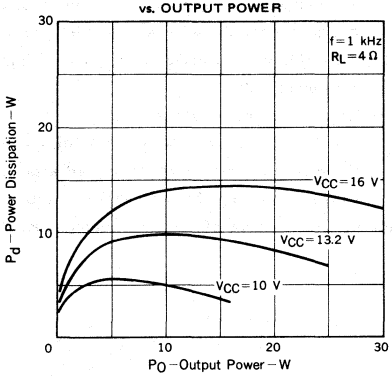
8

TYPICAL CHARACTERISTICS (T_a = 25 °C)

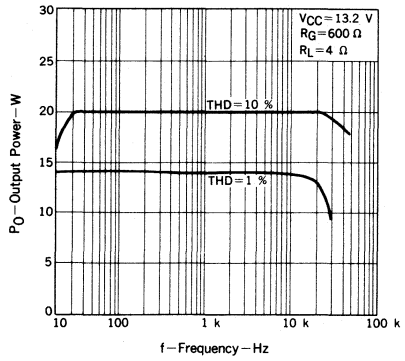
MAXIMUM ALLOWABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



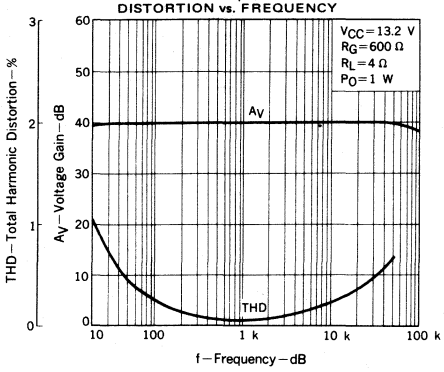
POWER DISSIPATION vs. OUTPUT POWER



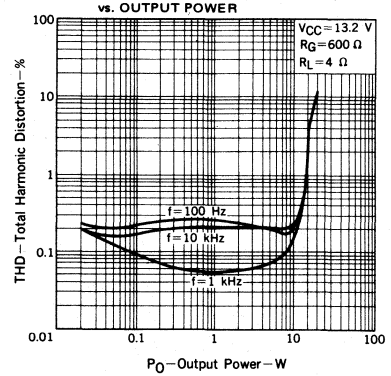
OUTPUT POWER vs. FREQUENCY



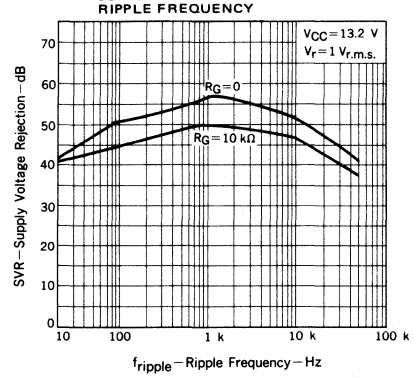
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



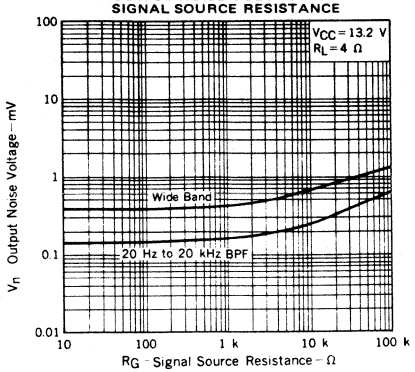
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



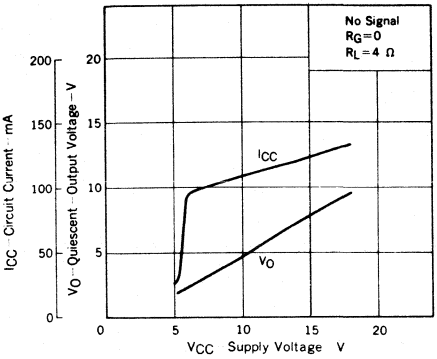
SUPPLY VOLTAGE REJECTION vs. RIPPLE FREQUENCY



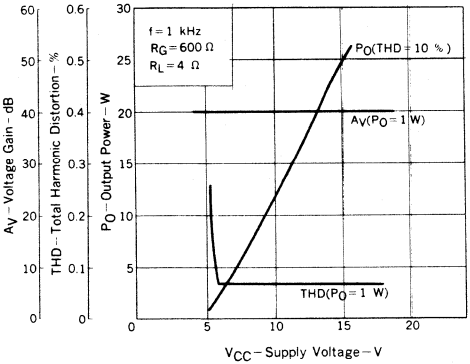
OUTPUT NOISE VOLTAGE vs. SIGNAL SOURCE RESISTANCE



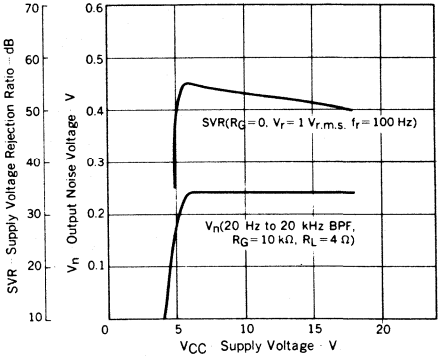
SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE CHARACTERISTICS



8

AUDIO POWER AMPLIFIER

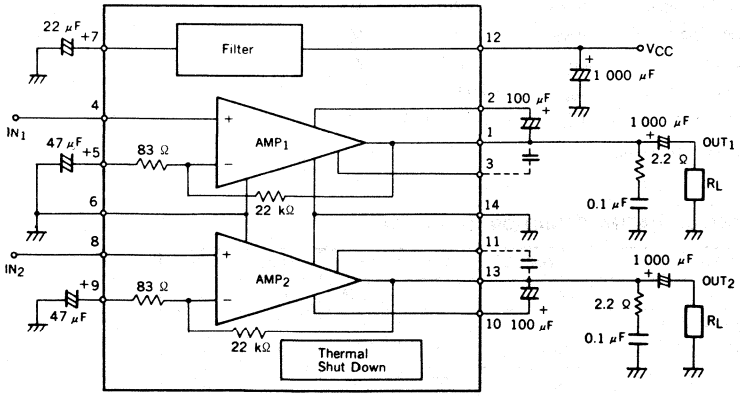
DESCRIPTION

The μPC1335V is a class B dual audio power amplifier designed for a music center and a radio cassette, and is encapsulated in a new 14 Pins vertical dual in line plastic package.

FEATURES

- High output power. 20 W (TYP.) @ V_{CC} = 18 V, R_L = 8 Ω (BTL)
  5.5 W/ch (TYP.) @ V_{CC} = 18 V, R_L = 8 Ω
  7 W/ch (TYP.) @ V_{CC} = 15 V, R_L = 4 Ω
  5.7 W/ch (TYP.) @ V_{CC} = 12 V, R_L = 3 Ω
  4.6 W/ch (TYP.) @ V_{CC} = 12 V, R_L = 4 Ω
- Wide operating voltage range. V_{CC} = 6 to 20 V
- Low quiescent current. I_{CC} = 23 mA (TYP.) @ V_{CC} = 15 V
- Low noise. N_L = 0.25 $mV_{r.m.s.}$ (TYP.)
- High supply voltage rejection. SVR = 55 dB (TYP.)
- No shock noise at power supply switch on and off.
- Soft clipping wave form.
- Thermal shut down circuit is built in.
- Low thermal resistance : $R_{th(j-c)}$ = 3 °C/W
- Very low number of external components, very simple mounting system with no electrical isolation between the package and the heat sink. (one screw only)

BLOCK DIAGRAM



CONNECTION DIAGRAM

PIN NO.	CONNECTION
1	Output $_1$
2	Boot Strap $_1$
3	Compensation $_1$
4	Input $_1$
5	NFB $_1$
6	GND (Input)
7	Filter
8	Input $_2$
9	NFB $_2$
10	Boot Strap $_2$
11	Compensation $_2$
12	V_{CC}
13	Output $_2$
14	GND (Output)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (No Signal)	V_{CC1}	28	V
Supply Voltage (Operating)	V_{CC2}	25	V
Power Dissipation	P_D	14*	W
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +150	°C

* 100 x 100 x 2 mm Al heat sink

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	6	12, 15	20	V
Load Impedance (DUAL)	R_L	3	4	8	Ω
Load Impedance (BTL)	R_L	4		8	Ω
Voltage Gain	A_V	36	48		dB

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_L = 4 Ω, f = 1 kHz, T_a = 25 °C, 100 x 100 x 2 mm Al Panel Heat Sink)

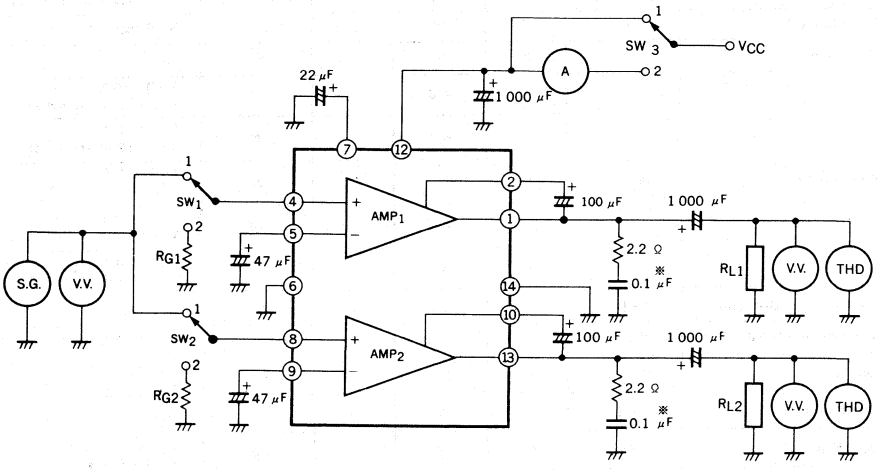
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Circuit Current	I_{CC}		23	36	mA	No Signal
Voltage Gain	A_V	46	48	50	dB	
Output Power	P_O		4.6		W	THD = 10 % V_{CC} = 12 V, R_L = 4 Ω
			5.7		W	THD = 10 % V_{CC} = 12 V, R_L = 3 Ω
		6	7		W	THD = 10 % V_{CC} = 15 V, R_L = 4 Ω
			5.5		W	THD = 10 % V_{CC} = 18 V, R_L = 8 Ω
			20		W	THD = 10 %, BTL V_{CC} = 18 V, R_L = 8 Ω
Total Harmonic Distortion	THD		0.2	1	%	P_O = 1 W
Output Noise Voltage	NL		0.25	0.6	$mV_{r.m.s.}$	DIN AUDIO R_G = 0
Cross Talk	C.T.	45	55		dB	P_O = 2 W other Ch. R_G = 0
Channel Balance	Ch. B.	−1	0	+1	dB	P_O = 4 W
Ripple Rejection	SVR	45	55		dB	R_G = 0, f = 100 Hz V = 0.3 $V_{r.m.s.}$
Input impedance	Z_{in}	20	30		kΩ	

SWITCH POSITION

ITEM	SYMBOL	SW_1	SW_2	SW_3
(DUAL OPERATION)				
Circuit Current	I_{CC}	2	2	2
Voltage Gain	A_V	1	1	1
Output Power	P_O	1	1	1
Total Harmonic Distortion	THD	1	1	1
Output Noise Voltage	NL	2	2	1
Cross Talk	C.T.	1/2	2/1	1
Channel Balance	Ch.B.	1	1	1
Supply Voltage Rejection	SVR	2	2	1
(BTL OPERATION)				
Output Power	P_O	–	–	–

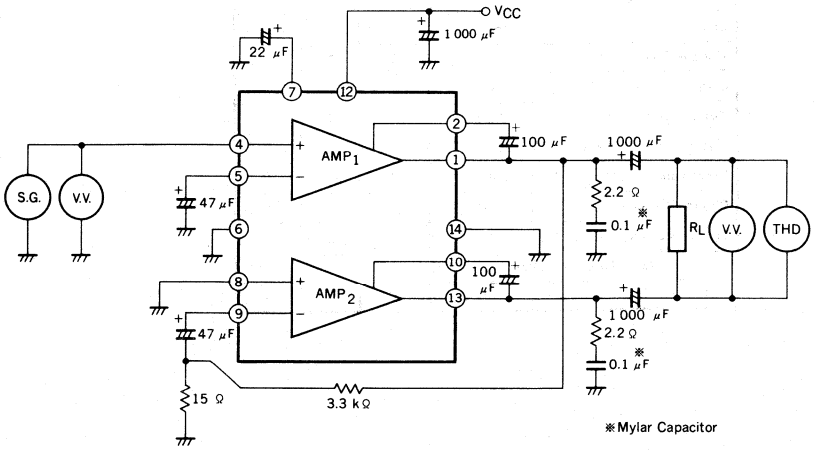
8

TEST CIRCUIT
(DUAL OPERATION)



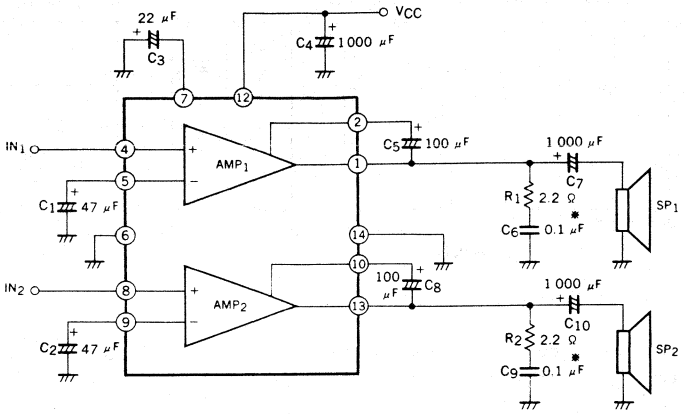
※Mylar Capacitor

(BTL OPERATION)



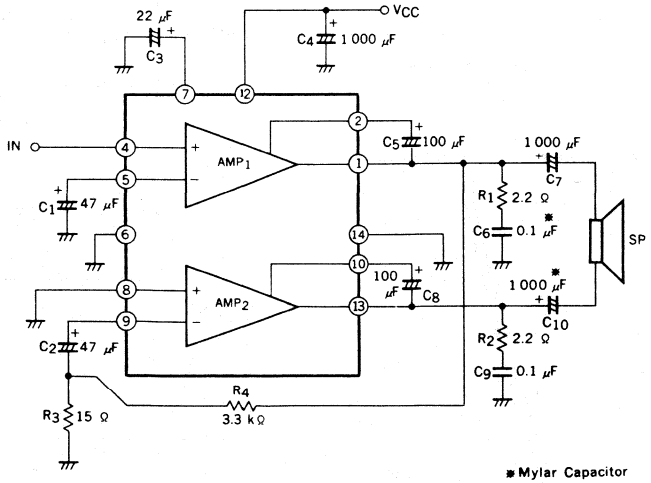
※Mylar Capacitor

TYPICAL APPLICATION
(DUAL OPERATION)



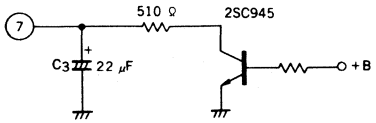
*Mylar Capacitor

(BTL OPERATION)



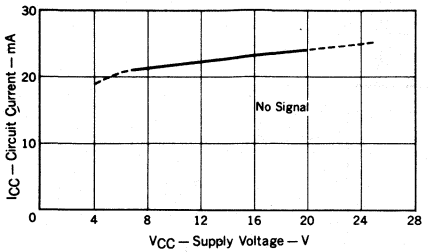
*Mylar Capacitor

(MUTING CIRCUIT)

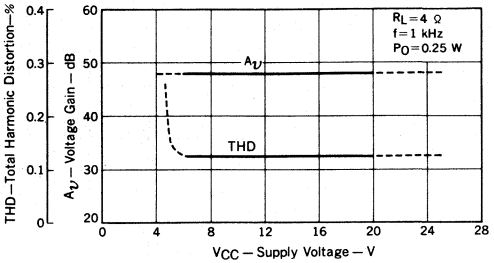


TYPICAL CHARACTERISTICS (T_a = 25 °C)

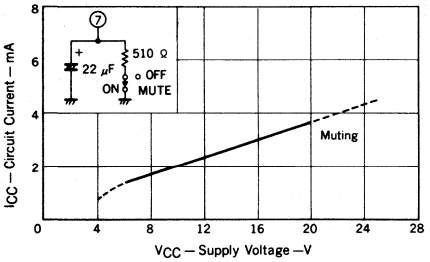
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



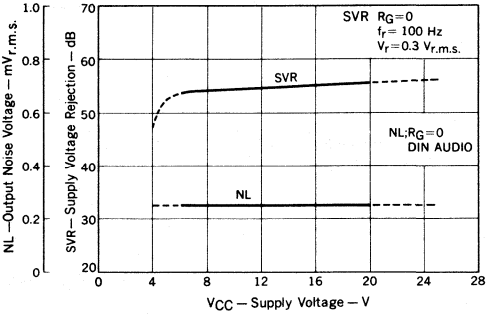
VOLTAGE GAIN vs. SUPPLY VOLTAGE, TOTAL HARMONIC DISTORTION



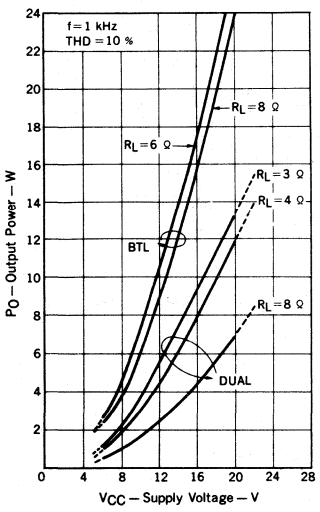
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



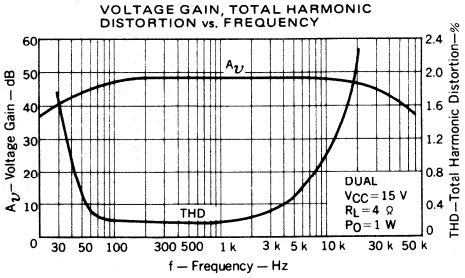
SUPPLY VOLTAGE REJECTION, OUTPUT NOISE VOLTAGE vs. SUPPLY VOLTAGE



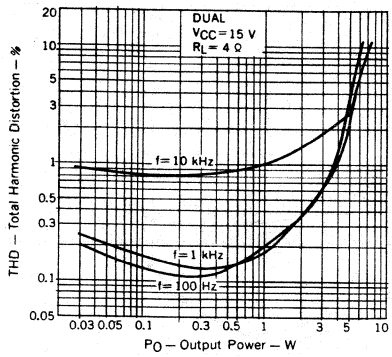
OUTPUT POWER vs. SUPPLY VOLTAGE



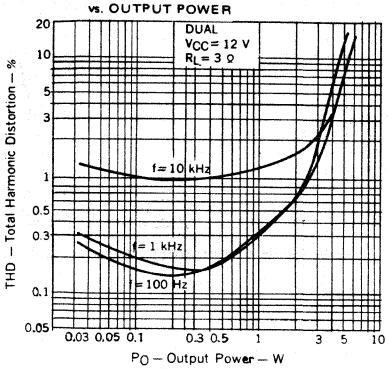
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



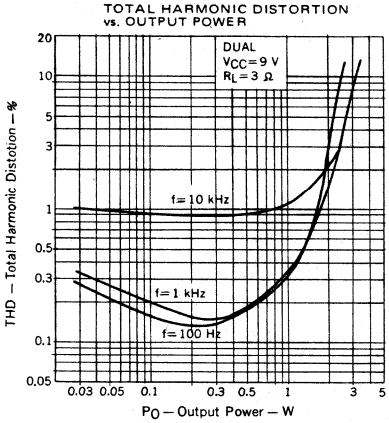
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



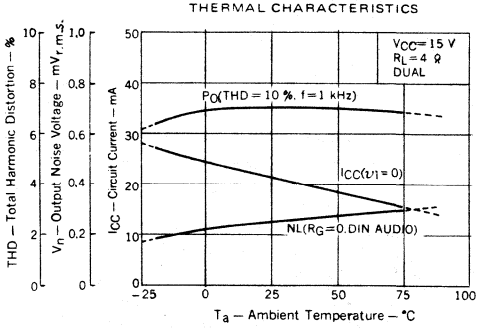
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



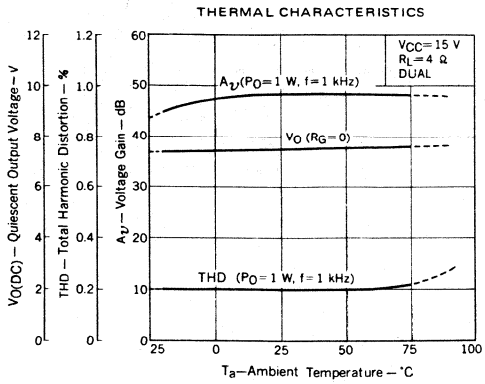
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



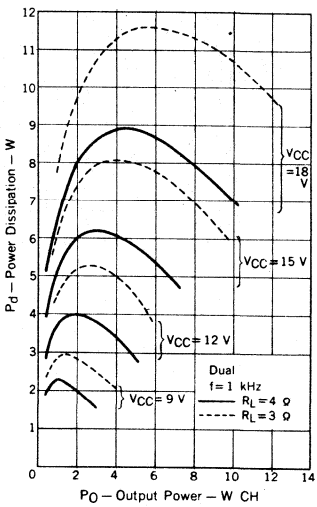
THERMAL CHARACTERISTICS



THERMAL CHARACTERISTICS

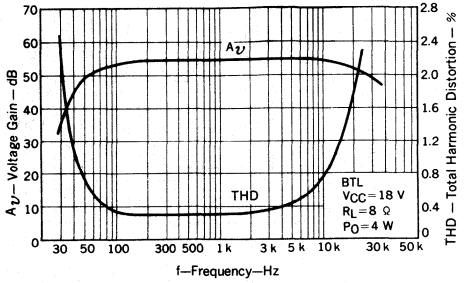


POWER DISSIPATION vs. OUTPUT POWER

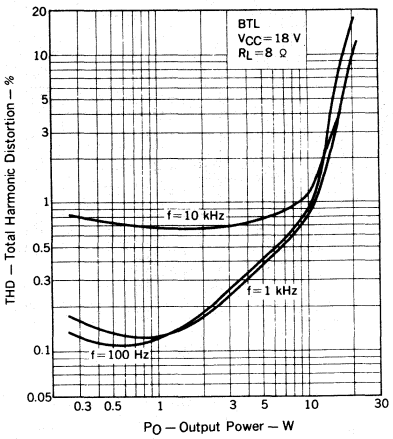


8

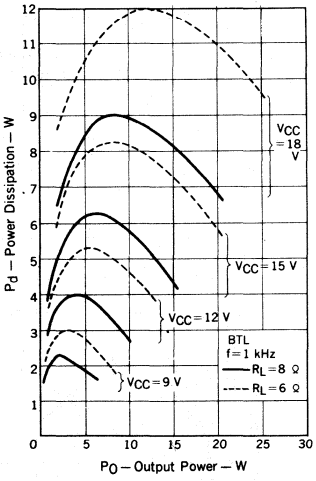
TOTAL HARMONIC DISTORTION, VOLTAGE GAIN vs. FREQUENCY



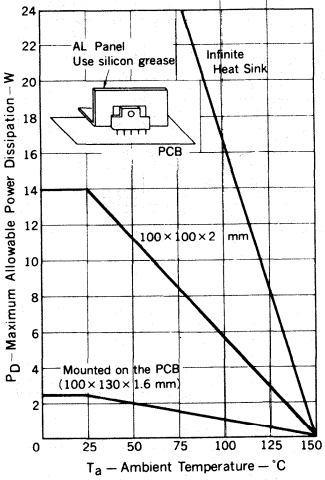
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



MAXIMUM ALLOWABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



NOTES FOR USE

(1) Adding a capacitor for phase compensation between Pin 1 (13) to Pin 3 (11), its value less than 47 pF is recommended, and the value of R_1 (R_2) and of C_6 (C_9) have to be chosen as follows.

R_1 (R_2) = 1 Ω

C_6 (C_9) = 0.15 μF

(2) At muting by shortage of Pin 7 to GND, ripple rejection is determinde by following equation.

$$SVR = \left| 20 \log \frac{R_L}{200+R_L} \right|$$

(3) Keep the μPC1335V's heat sink in shortage to GND or floating condition.

(4) Direct shortage between Pin 1 (13) to V_{CC} or GND will damage the μPC1335V.

(5) Keep some margin at design of external heat sink size.

(6) Use silicon grease and keep the torque of screw driver less than 10 kg·cm in attachment of a external heat sink.

Display-driver

LCD CONTROLLER/DRIVER ICs FOR 1/2-1/4 DUTY DRIVING

The μPD16430 is LCD driver IC with control circuit for 1/2, 1/3, 1/4 duty driving. The control block is able to transfer data serially from micro-computer system. And control cuircuit has the function of "Automatic Data Address Increment Mode" so that it isn't necessary to increase data address every data is transferred.

The Driver circuits have ability to switch middle voltage. (16 V MAX.) So it is able to get high contrast display with 1/3 or 1/4 duty driving.

And the μPD16430 has LCD driving voltage generator, it is able to reduce the number of outer parts.

FEATURES

- Middle Voltage Swing Capability
- Enable to Select Driving Duty (1/2, 1/3 or 1/4)
- Number of Display Segments
  - 1/2 duty: 120 seg.
  - 1/3 duty: 160 seg.
  - 1/4 duty: 240 seg.
- Enable to Select Bias (1/2 bias or 1/3 bias)
- Enable to Select Frame Frequency of 4 kinds
- Ability to Connect Multitude Chips
- Data Format is Serial 8 bit
- Power on Reset Circuit
- CMOS Structure
- Control Voltage is 3.5 to 6 V

ORDERING INFORMATION

PART NO.	PACKAGE	QUARITY GRADE
μPD16430GF-3B9	80 Pin Plastic QFP (14 x 20)	Standard

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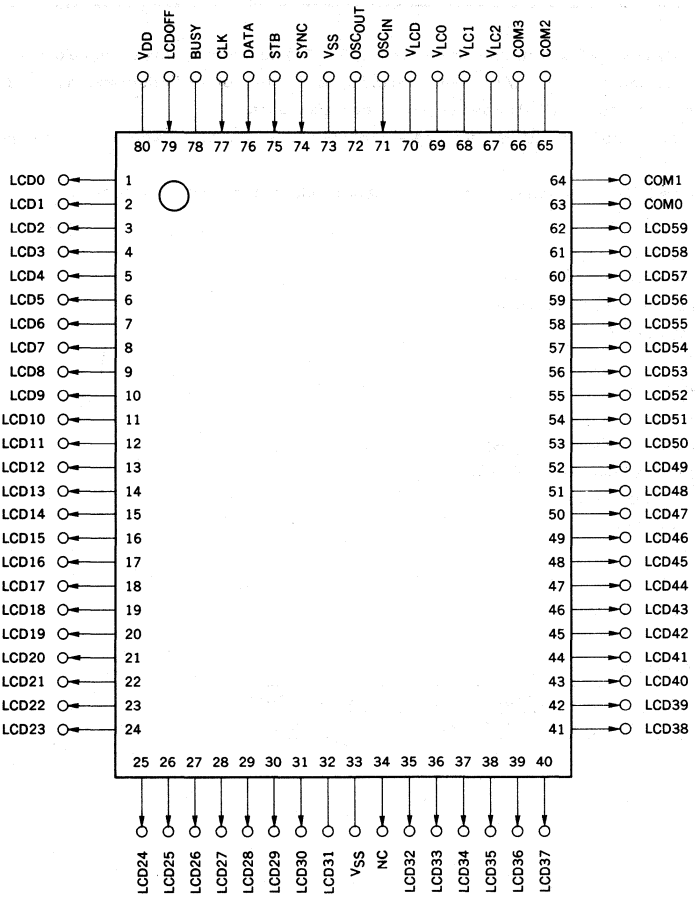
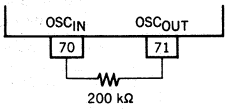
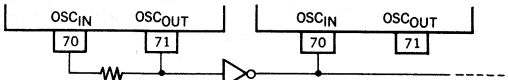
PIN CONNECTION DIAGRAM (TOP VIEW)



PIN CONFIGURATION

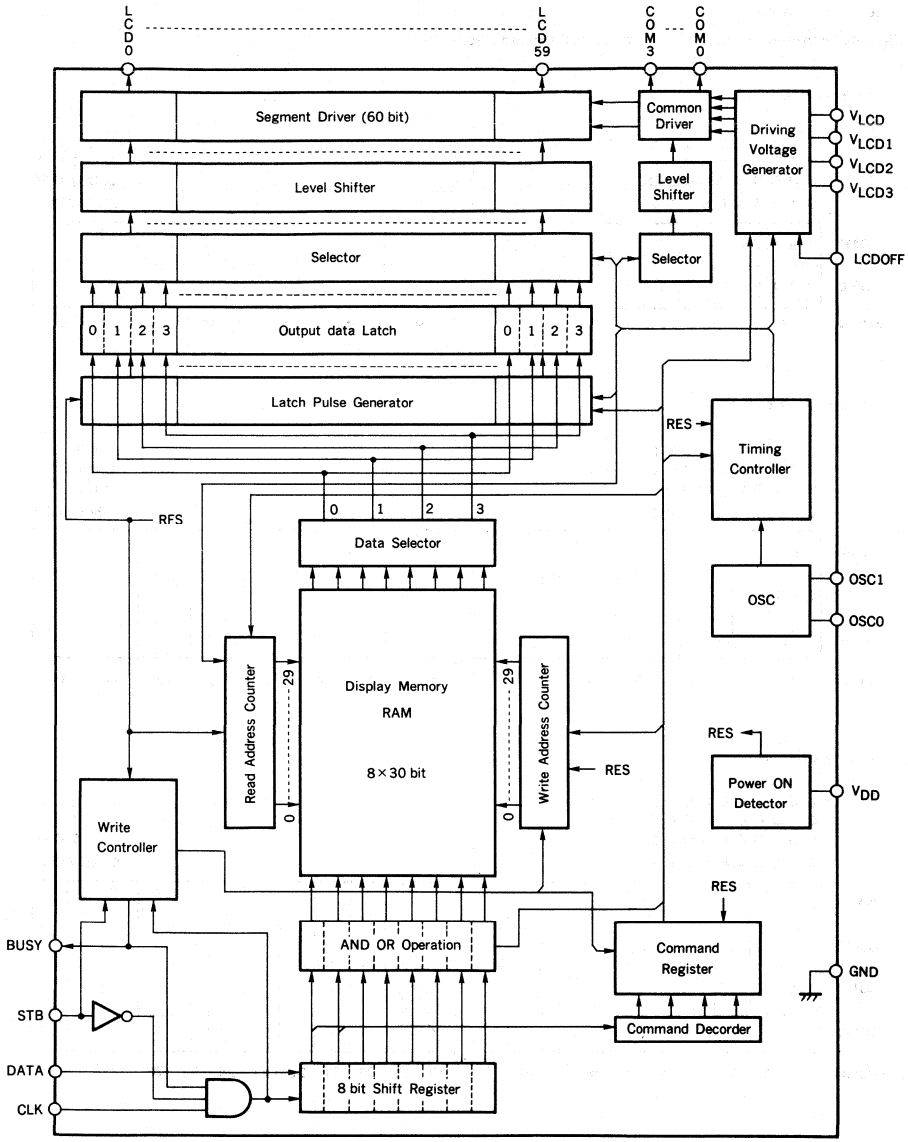
<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>I/O</th><th>OUTPUT</th><th>EXPLANATION</th></tr>
<tr><td>1-32
35-62</td><td>LCD0 –LCD31
LCD32–LCD59</td><td>O
O</td><td>CMOS
CMOS</td><td>Segment driver output
<table>
<tr><th>DUTY</th><th>BIAS</th><th>NO. OF SEG.</th><th>FRAME FREQUENCY (Hz)</th></tr>
<tr><td>1/2</td><td>1/2</td><td>120</td><td>$f_{osc}/256$, $f_{osc}/512$, $f_{osc}/1024$ or $f_{osc}/2048$</td></tr>
<tr><td>1/3</td><td>1/3</td><td>160</td><td>$f_{osc}/384$, $f_{osc}/768$, $f_{osc}/1536$ or $f_{osc}/3072$</td></tr>
<tr><td>1/4</td><td>1/3</td><td>240</td><td>$f_{osc}/512$, $f_{osc}/1024$, $f_{osc}/2048$ or $f_{osc}/4096$</td></tr>
</table>
It is possible to display 240 segments maximum using segment driver outputs and common driver outputs in 1/4 duty driving. Segment drivers' voltage are supplied from V_{LCD} terminal. V_{LCD} maximum voltage is 12 V. The bias resistor is able to select of internal or outer its.</td></tr>
<tr><td>63–66</td><td>COM0–COM3</td><td>O</td><td>CMOS</td><td>Common driver outputs
It is able to select of 3 display modes.
Common drivers' voltage are supplied from V_{LCD}.</td></tr>
<tr><td>67
68
69</td><td>V_{LC2}
V_{LC1}
V_{LC0}</td><td>I</td><td>–</td><td>These are LCD driving level supply terminals.
It is able to select of internal resistor or outer supply level using to set commands.</td></tr>
<tr><td>70</td><td>V_{LCD}</td><td>–</td><td>–</td><td>Driver part power supply terminal.
This terminal is supplied LCD driving voltage.
LCD driving voltage is typically 12 V.
Don't supply voltage until going 3.5 V in V_{DD}.</td></tr>
<tr><td>71
72</td><td>OSC_{IN}
OSC_{OUT}</td><td>I
O</td><td>CMOS</td><td>These terminals are for system clock oscillator.
Please connect a resistor following figure.
 

Using only one chip
 

Using some chips connected each other</td></tr>
<tr><td>34
73</td><td>V_{SS}</td><td>–</td><td>–</td><td>Ground terminals</td></tr>
<tr><td>74</td><td>SYNC</td><td>I/O</td><td>–</td><td>Synchronous input
This terminal is used that some chips connected each other. How to connect is wired OR.</td></tr>
</table>

PIN NO.	SYMBOL	I/O	OUTPUT	EXPLANATION
75	STB	I	–	This terminal is input of device selecting signal and strobe signal in serial communication. It is enable to latch display data in output latch circuits and to clear serial communication and mode of receiving commands. It is enable to communicate while STB is low level. The shift clock pulses inputed while STB is high level aren't recognized. (1) Latch display data to output buffers When BUSY is high level, display data is latched in output latch circuit at rising edge of STB. But if internal LATCHMD flag is reset, LATCHMD flag have to be set "1". Latch time needs $48/f_{osc}$. (2) Setting the receiving command data mode When BUSY is high level, the mode of receiving command data mode is set at falling edge of STB. First 1 byte data is regarded command data in receiving command data mode. And next data is regarded display data until next falling edge of STB. Command data function time is about 300 ns. And in this time, BUSY isn't changed any state. (3) Initialize serial communication When BUSY is low level, it clear serial communication at falling edge of STB. It becomes receiving command data mode after clearing serial communication. While μPD16430 is going to decode command data or write display data to display data to display memory, it is canceled to function at falling edge of STB and clear serial communication. And at this time all display disappear. (LCDON flag are going to reset.)
76	DATA	I		This terminal is the input of serial data. The data are read at rising edge of shift clock.
77	CLK	I		This terminal is the input of shift clock.
78	BUSY	O	3-State	Internal status is appeared in this terminal. It is able to communicate from/to micro-processor while BUSY is high level. While BUSY is high level, shift clock pulses are invalid. While STB is high level, BUSY is high impedance. After power on reset function, BUSY is low level until STB pulse is input.
79	LCDOFF	I		While this terminal is high level, display disappears and LCDON flag is reset. But this function dosen't influence serial communication. And to appear display again, LCDON flag has to be set "1".
80	V_{DD}			This terminal is power supply terminal. It is necessary to supply 3.5 V–5.5 V. If supply voltage is going 0 V to 3.5 V or decrease under 3.5 V, power on reset circuit become enable. Display disappear after power on reset function. CAUTION Please don't supply voltage over than V_{DD} voltage to V_{LCD} terminal while V_{DD} voltage is lower than 3.5 V. Following sequences are recommended. When power on, at first turn on V_{DD} and next turn on V_{LCD}. When power off, at first turn off V_{LCD} and next turn off V_{DD}.

BLOCK DIAGRAM



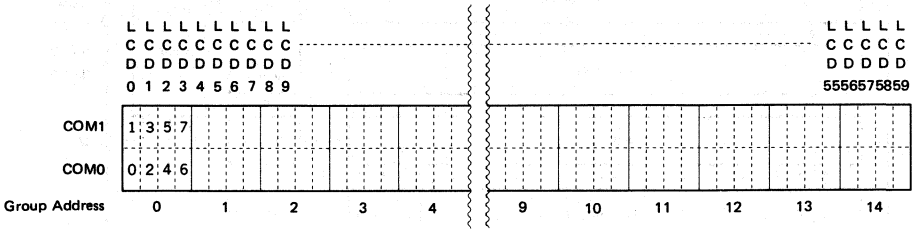
RELATION DISPLAY MEMORY ADDRESS AND DISPLAY DOT

Display memory is the place stored display data temporarily.

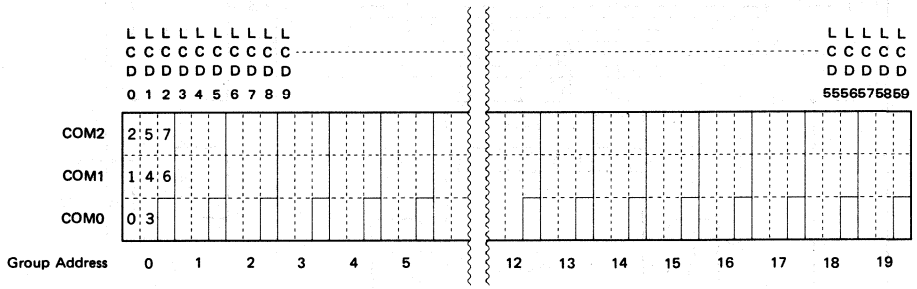
Display memory has address (group address) every 8 bit. And it is possible to write display data transferred at once to same group address's memory.

Following figures are shown relation group address and display dot.

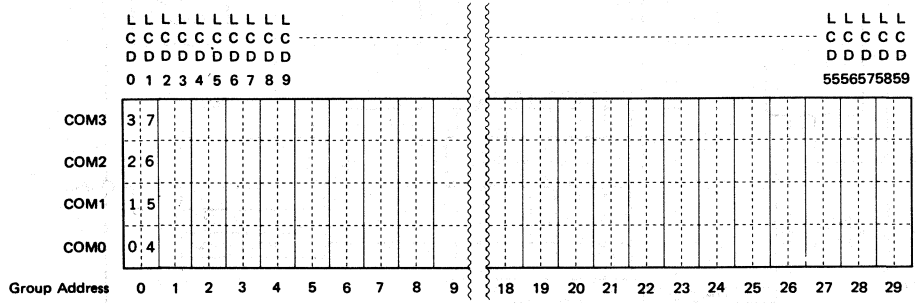
(1) 1/2 duty driving



(2) 1/3 duty driving



(3) 1/4 duty driving



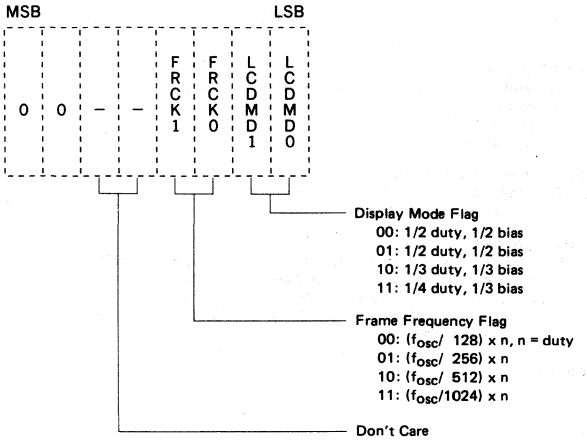
COMMAND REFERENCE

Command function to set display mode and internal status.

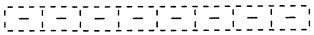
First 1 byte data after falling edge of STB is regarded command data.

It is shown command following sentence.

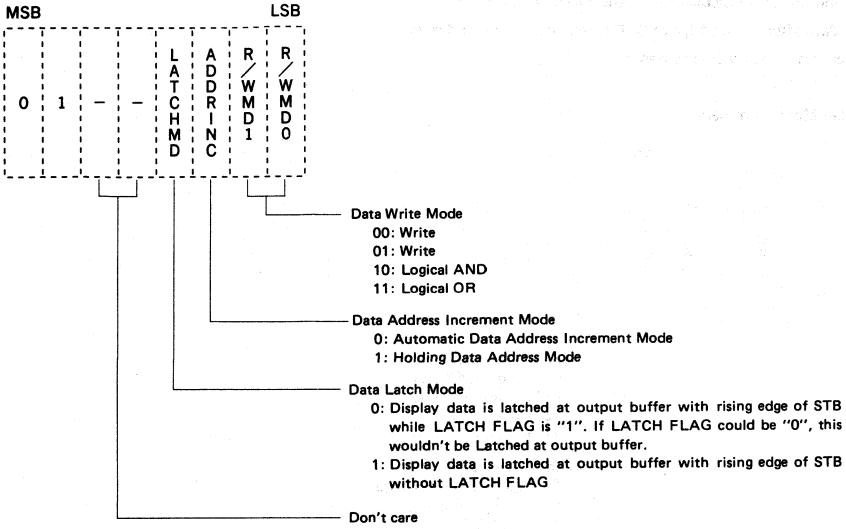
1. Set up Display Mode Command



After Power On Reset



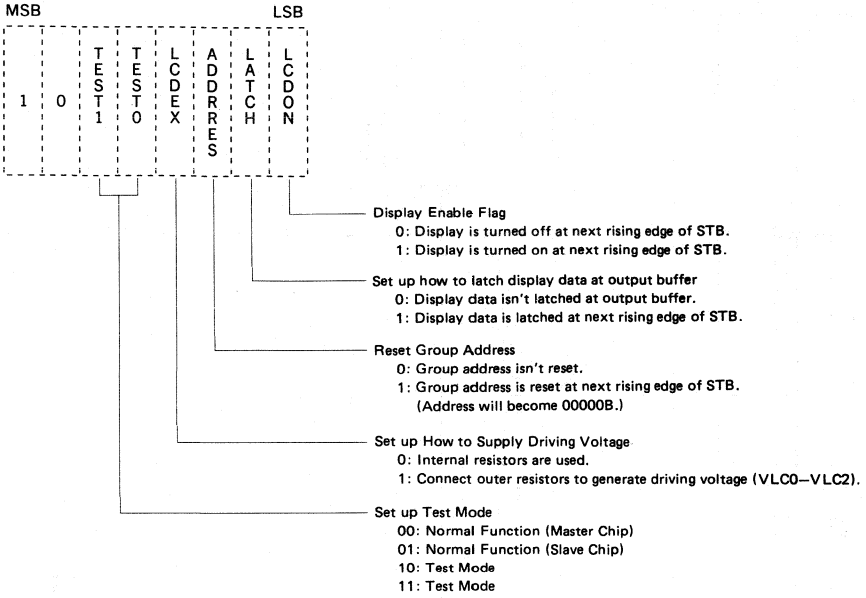
(2) Set up Data Mode Command



After Power On Reset

–	–	–	–	0	0	0	0

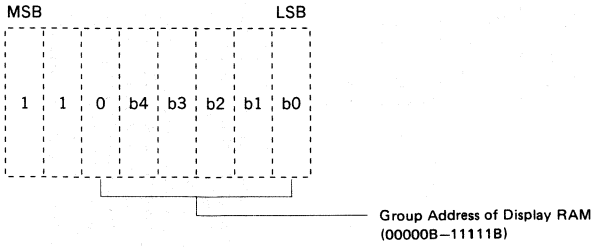
(3) Set up Status Command



After Power On Reset

–	–	0	0	0	0	0	0

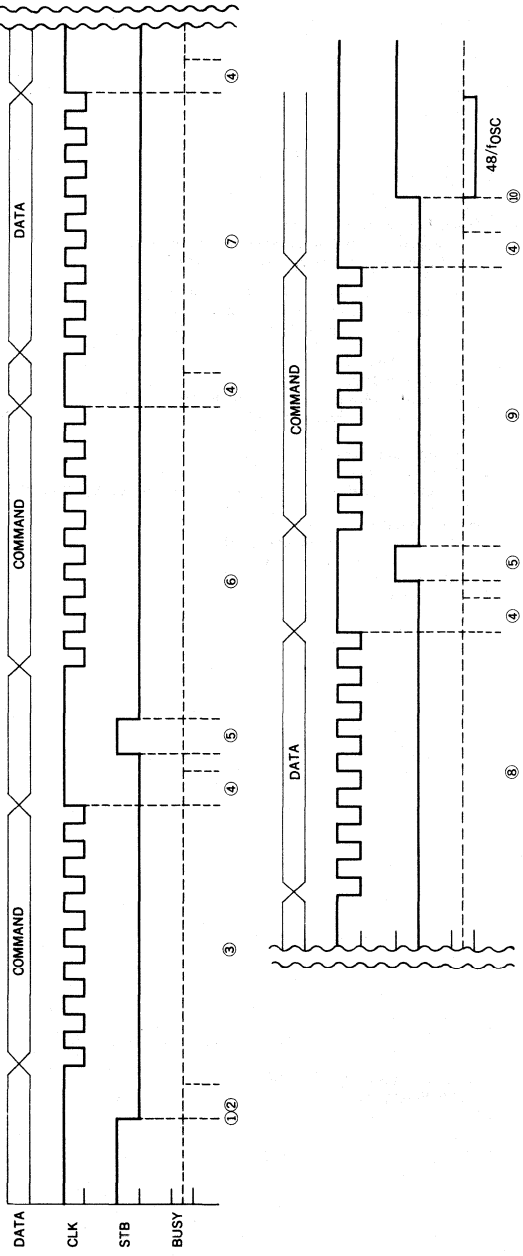
(4) Set up Address Command



After Power On Reset

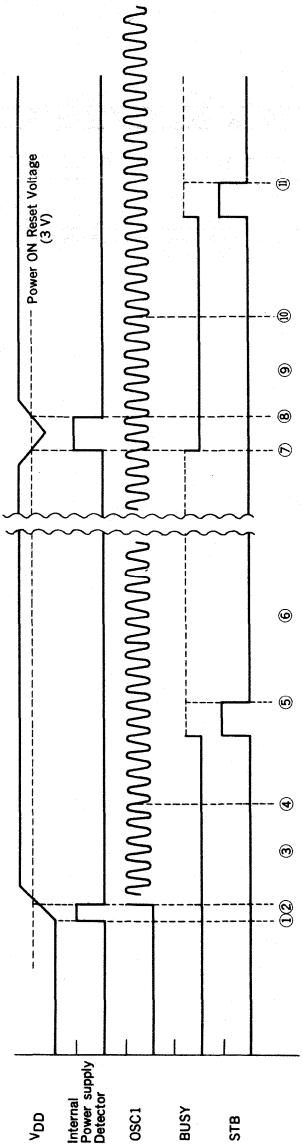
–	–	–	0	0	0	0	0

SEQUENCE OF DATA TRANSFER



① Initialize serial communication to fall STB.
② Wait 300 ns (Internal transaction time)
③ Transfer "Set up mode command" if it is initialized state.
④ Wait 300 ns
⑤ μPD16430 become to wait command data after falling edge of STB.
⑥ Input "Set up Address Command" or "Set up Data Mode Command".
⑦ Transfer RAM data pointed at address which has already set.
⑧ Transfer RAM data pointed at address which has already set.
⑨ Input "Set up Address Command" or "Set up Data Mode Command".
⑩ To rise STB signal, RAM data is latched at output buffer and display is turned on.
⑪ BUSY signal (Low Level) appears while data is latched. The pulse width is $48/f_{OSC}$.

POWER ON RESET SEQUENCE



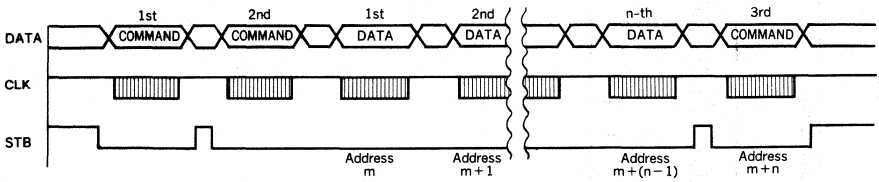
① Supplying V_{DD}
② When V_{DD} voltage is higher than the voltage of power on reset, function starts.
③ This period is oscillator's stabilization time. (less than 10 ms)
Don't input STB pulse while this period.
④ It is ready for STB pulse input.
⑤ If STB pulse is input, BUSY terminal appears high level and it is able to receive new command data.
⑥ Waiting new command data.
⑦ When V_{DD} voltage down than the voltage of power on reset, function stop.
⑧ When V_{DD} voltage up than the voltage of power on reset, function start again.
⑨ Oscillator's stabilization time. (less than 10 ms)
⑩ It is ready for STB pulse input.
⑪ If STB pulse is input, BUSY terminal appears high level and it is able to receive new command data.
⑫ Waiting new command data.

Power on reset function
(1) turning off all display
(2) initializing serial communication

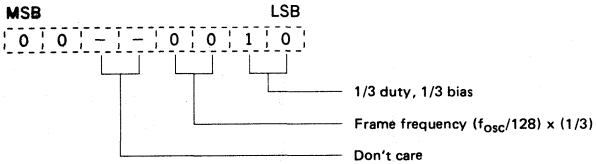
9

EXAMPLE HOW TO USE COMMAND

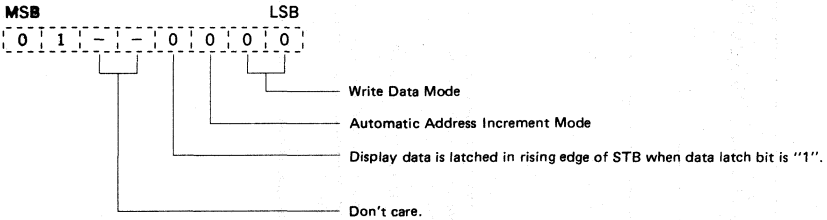
(1) Data Address Increment Mode



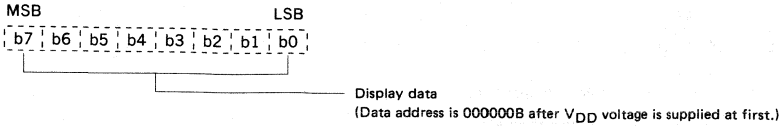
1st Command



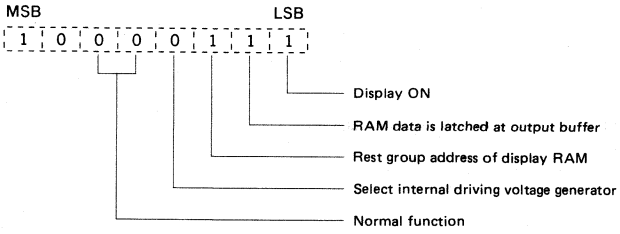
2nd Command



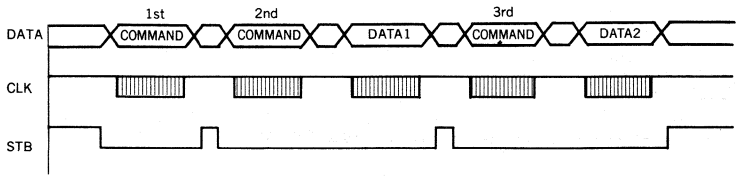
Data 1–n



3rd Command



Changing optional address data (bit manipulation with addressing)



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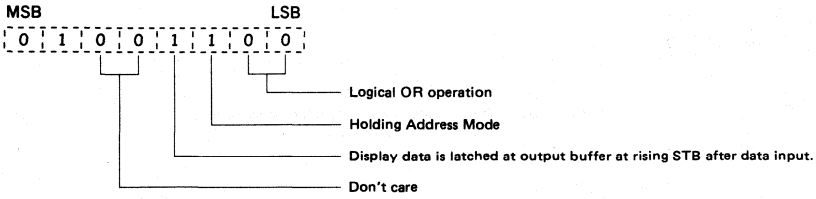
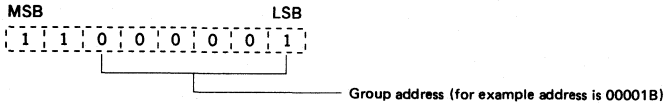
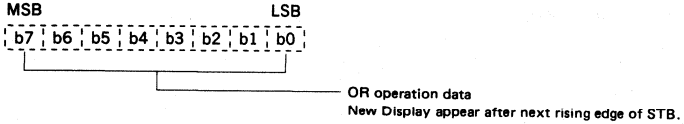
1st Command



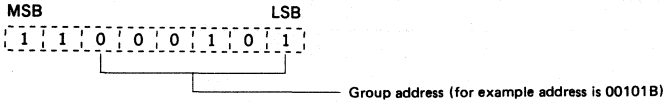
2nd Command



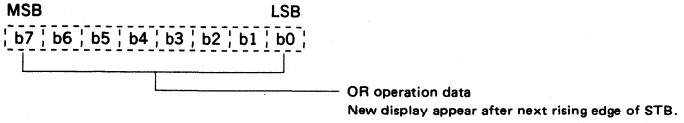
1st Data



3rd Command



2nd Data



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, GND = 0 V)

Logic Power Supply Voltage	V_{DD}	−0.3 to +7.0	V
Logic Input Voltage	V_I	−0.3 to V_{DD}+0.3	V
Logic Output Voltage	V_{O1}	−0.3 to V_{DD}+0.3	V
Driver Power Supply Voltage	V_{LCD}	−0.3 to +16	V
Driver Input Voltage	V_{LC0}–V_{LC2}	−0.3 to V_{LCD}+0.3	V
Driver Output Voltage	V_{O2}	−0.3 to V_{LCD}+0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −40 to +85 °C, GND = 0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Logic Power Supply Voltage	V_{DD}	3.5		6.0	V	
Driver Power Supply Voltage	V_{LCD}	V_{DD}		14	V	
Driver Input Voltage	V_{LC0}–V_{LC2}	0		V_{LCD}	V	

9

ELECTRICAL CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V, V_{LCD} = 9 to 12 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	
High Level Output Voltage	V_{OH}	0.9 V_{DD}			V	OSC_{OUT}, I_{OH} = −1 mA
Low Level Output Voltage	V_{OL}			0.1 V_{DD}	V	OSC_{OUT}, SYNC, BUSY I_{OL} = 1 mA
High Level Input Leak Current	I_{IH}			10	μA	V_{IN} = V_{DD}
Low Level Input Leak Current	I_{IL}	−10			μA	V_{IN} = V_{SS}
High Level Output Leak Current	I_{LOH}			10	μA	SYNC, BUSY V_O = V_{DD}
Low Level Output Leak Current	I_{LOL}	−10			μA	SYNC, BUSY V_O = V_{SS}
Common Output Impedance	R_{COM}		1.2	2.4	kΩ	COM0–COM3, V_{LCD} = 9 V $\|I_O\|$ = 100 μA
Segment Output Impedance	R_{SEG}		2	4	kΩ	LCD0–LCD59, V_{LCD} = 9 V $\|I_O\|$ = 100 μA
Logic Supply Current	I_{DD}		200	500	μA	f_{OSC} = 140 kHz
Driver Supply Current	I_{LCD}		350	700	μA	V_{LCD} = 12 V, No-load

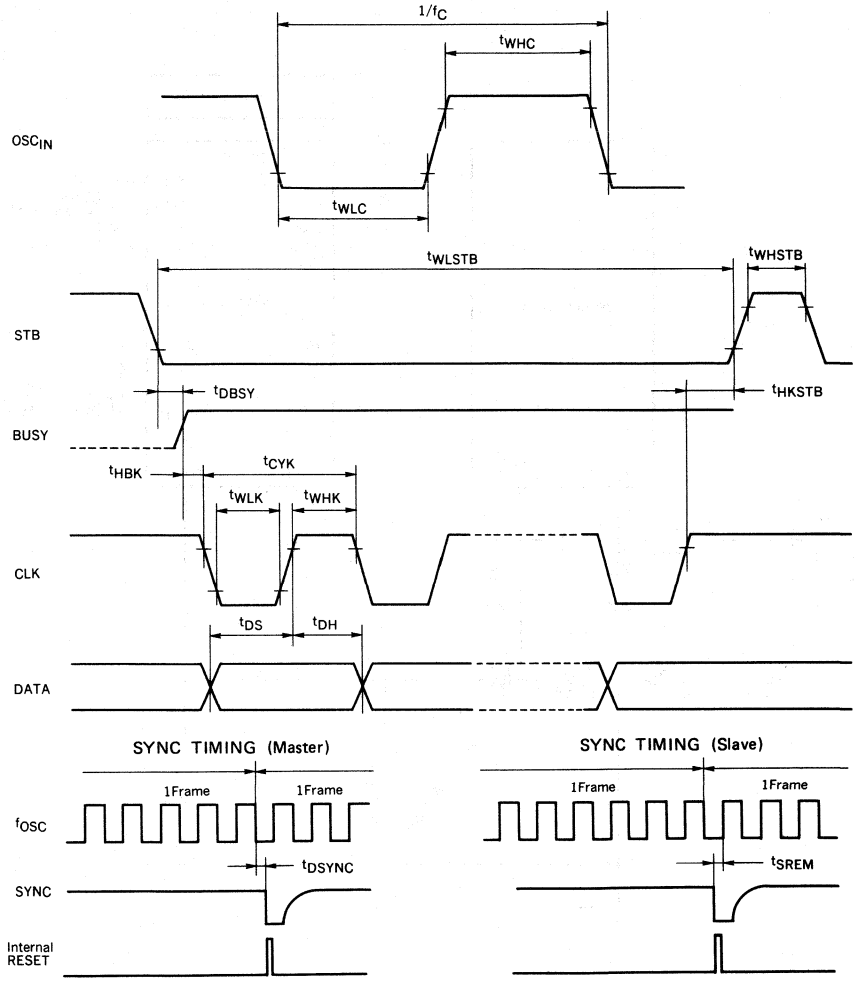
SWITCHING CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V, V_{LCD} = 9 to 12 V, R_L = 5 kΩ, C_L = 150 pF)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Oscillation Frequency	f_{OSC}	98	140	182	kHz	R = 200 kΩ
BUSY Delay Time	f_{DBSY}		0.02	1.5	μs	STB↑ to BUSY↓
SYNC Delay Time	f_{DSYNC}		250	500	ns	

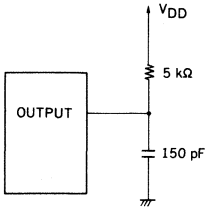
TIMING REQUIREMENT CONDITION (T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V, V_{LCD} = 9 to 12 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock Frequency	f_c	50		200	kHz	Outer Clock
High Level Clock Width	t_{WHC}	2		16	μs	OSC_{IN}, Outer Clock
Low Level Clock Width	t_{WLC}	2		16	μs	OSC_{IN}, Outer Clock
Shift Clock Cycle Time	t_{CYK}	900			ns	CLK
High Level Shift Clock Width	t_{WHK}	400			ns	CLK
Low Level Shift Clock Width	t_{WLK}	400			ns	CLK
Shift Clock Hold Time for BUSY signal	t_{HBK}	0			ns	BUSY↑ to CLK↓
Data Setup Time for CLK	t_{DS}	100			ns	
Data Hold Time for CLK	t_{DH}	200			ns	
STB Hold Time for 8th CLK	t_{HKSTB}	1			μs	
High Level STB Pulse Width	t_{WHSTB}	1			μs	
Low Level STB Pulse Width	t_{WLSTB}	8.2			μs	
Internal Reset Removal Time	t_{SREM}	250			ns	

SWITCHING CHARACTERISTICS WAVEFORM



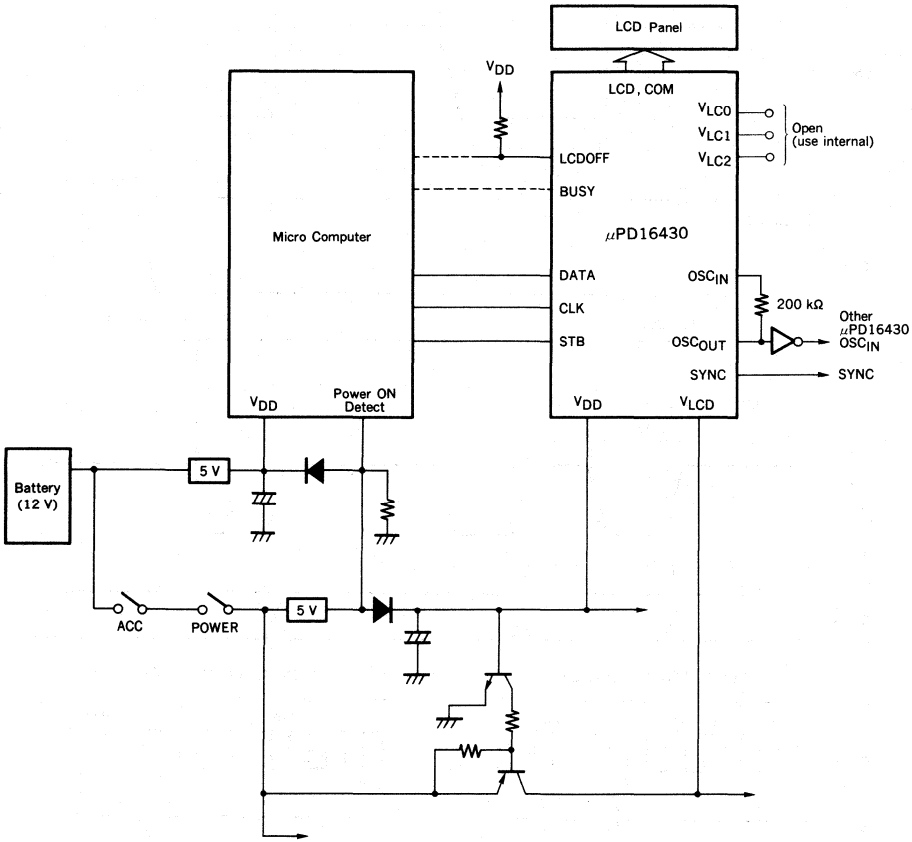
Test Circuit



Testing Point
INPUT ; 0.7 V_{DD}, 0.3 V_{DD}
OUTPUT; 0.8 V_{DD}, 0.2 V_{DD}

9

EXAMPLE APPLICATION CIRCUIT



Development tools

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Section 10 - Development tools

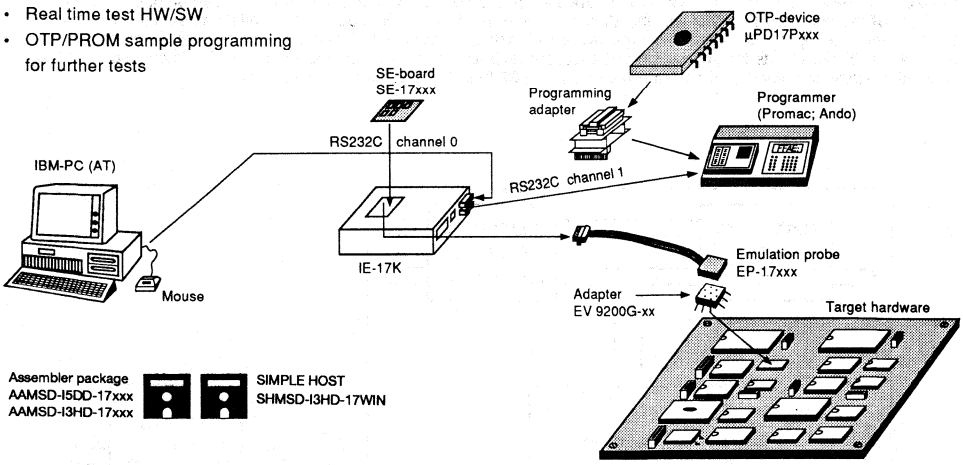
1. Development tools for the μPD17K-Family

This section gives a brief explanation of the development environment of the μPD17K-Family.

Hardware Tools: - IE-17K
- SE-17xxx
- EP-17xxx
- EV-9200G-xx

Software Tools: - AAMSD-I5DD-170xx (Assembler for μPD170xx)
- AAMSD-I3HD-170xx (Assembler for μPD170xx)
- AAMSD-I5DD-171xx (Assembler for μPD171xx)
- AAMSD-I3HD-171xx (Assembler for μPD171xx)
- AAMSD-I5DD-172xx (Assembler for μPD172xx)
- AAMSD-I3HD-172xx (Assembler for μPD172xx)
- SHMSD-I3HD-17WIN (Source level debugger SIMPLEHOST)

- SW development
- HW/SW debugging
- Real time test HW/SW
- OTP/PROM sample programming for further tests



Development Environment

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IE-17K

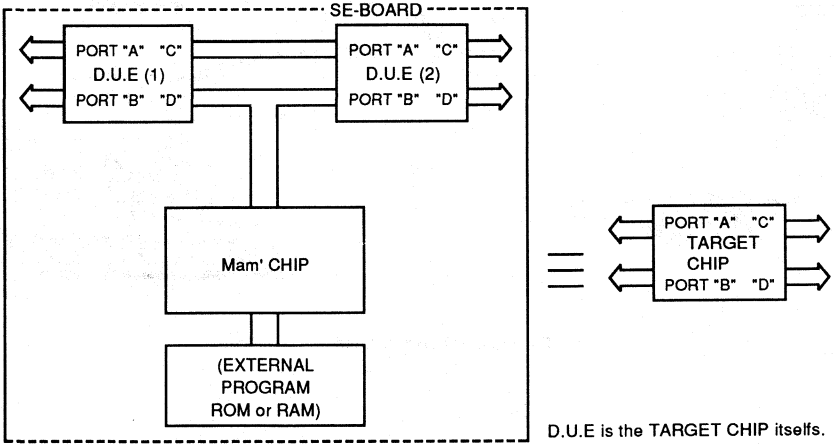
The IE-17K is a software development support tool applicable to every model of the μPD17K-Family. It consists of two boards:
a memory board and a supervisor board.

Features:

- Real-time emulation and one step emulation are available.
- Programmable break/trace function by which various break/trace conditions can be set hierarchically.
- Real-time trace function with a large-capacity trace memory (32K steps)
- Data memory coverage function which displays the state of writing in the data memory.
- Program memory coverage function which increments a counter every time an instruction which references to an address location is executed. The maximum count is 255.
- Incorporated programmable pattern generator (PPG) with 14 channels.

SE-17xxx

The SE-17xxx is the device-specific emulator board which completes the in-circuit-emulator. To ensure that the system evaluation (SE) board exhibits the same electrical behaviour as the original IC, a method known as „MAM chip" (implemented as an ASIC) device is applied. Two μPD17000 devices and a MAM chip are mounted on the SE board as shown in the diagram. Half the I/O-lines of each 17000 device are passed outside the board, so that they can be used to evaluate the I/O-lines of the real chip. Together with the MAM chip the other device form a bus system. All data sent out from the SE board or received by the SE board from outside are routed through the two μPD17000 devices. Therefore an observer outside the SE board gets the impression that a real chip is being used. The external memory which is connected to the MAM chip stores the developed software in the case the SE board is used as a standalone system.



Emulation Chip Set Configuration

EP-17xxx

To connect the SE board with the printed circuit board a special cable is required. This device-specific emulation probe is called EP-17xxx.

EV-9200G-xx

The EV-9200G-xx is a special adapter socket to connect the emulation probe EP-17xxx with the target hardware in the case that the target device is mounted in a QFP package. This conversion socket is soldered onto the PCB.

AAMSD-I5DD-170xx
AAMSD-I3HD-170xx
AAMSD-I5DD-171xx
AAMSD-I3HD-171xx
AAMSD-I5DD-172xx
AAMSD-I3HD-172xx

These are absolute macro assembler packages used for all devices of the 170xx, 171xx and the 172xx device group. They all comprise two parts. One part is the main unit used for all devices of the corresponding device group, the other is a device file for the particular μPD17000 device. The device file includes device-specific information, like ROM and RAM size, reserved words and addresses of the on-chip hardware functions. The assembler has a unique feature which supports software assembly of the code configured in modules. The assembler handles up to 99 modules. This feature, however, belongs to a relocatable assembler. The assembler is not able to assemble each module separately. Nevertheless, after the software is assembled for the first time, the assembler can be directed to assemble only those parts of the user program which were changed. Therefore the software development is speeded up.
The assembler also performs linkage operations to produce an executable code. In addition, this assembler supports powerful macro functions to end up in a versatile development tool for execution in a MS-DOS environment.

SIMPLEHOST

SIMPLEHOST is a full-screen debugger which improves the interface between the in-circuit-emulator and the operator. SIMPLEHOST runs under Microsoft Windows, which means that all emulator commands can be selected and activated with a mouse. The contents of the ROM and RAM size of the emulator are shown on the screen together with the source program.

Overview of the development enviroment for the μCOM 17K-Family

Device	SE board	Probe	Adapter	Assembler package
μPD17001GH	SE-17001	EP-17001GH	EV-9200GH-48	
μPD17003AGF	SE-17005	EP-17003GF	EV-9200G-80	
μPD17005GF	SE-17005	EP-17003GF	EV-9200G-80	
μPD17006GF	SE-17006	EP-17201GF	EV-9200G-80	AAMSD-I5DD-170XX
μPD17010GF	SE-17010	EP-17003GF	EV-9200G-80	
μPD17002CU	SE-17002	EP-17002CU		
μPD17002GF	SE-17002	No flat probe yet	EV-9200G-64	
μPD17008CW	SE-17008	EP-17008CW		
μPD17051CU	SE-17051	EP-17051CU		
μPD17052CW	SE-17052	EP-17052CW		
μPD17053CW	SE-17053	EP-17052CW		
μPD17102G	SE-17102	EP-17102G	EV-9200G-52	
μPD17106GC	SE-17106	EP-17106GC	EV-9200G-64	
μPD17103CX	SE-17103	EP-17103CX		AAMSD-I5DD-171XX
μPD17103GS	SE-17103	No SOP probe		
μPD17103LCX	SE-17103L	EP-17103CX		
μPD17103LGS	SE-17103L	No SOP probe		
μPD17104CS	SE-17104	EP-17104CS		
μPD17104GS	SE-17104	No SOP probe		
μPD17104LCS	SE-17104L	EP-17104CS		
μPD17104LGS	SE-17104L	No SOP probe		
μPD17107CX	SE-17107	EP-17103CX		
μPD17107GS	SE-17107	No SOP probe		
μPD17107LCX	SE-17107	EP-17103CX		
μPD17107LGS	SE-17107	No SOP probe		
μPD17108CS	SE-17108	EP-17104CS		AAMSD-I5DD-171XX
μPD17108GS	SE-17108	No SOP probe		
μPD17108LCS	SE-17108	EP-17104CS		
μPD17108LGS	SE-17108	No SOP probe		
μPD17134ACT	SE-17134	EP-17134CT		
μPD17134AGT	SE-17134	No SOP probe		
μPD17135ACT	SE-17134	EP-17134CT		
μPD17135AGT	SE-17134	No SOP probe		
μPD17136ACT	SE-17134	EP-17134CT		
μPD17136AGT	SE-17134	No SOP probe		
μPD17137ACT	SE-17134	EP-17134CT		
μPD17137AGT	SE-17134	No SOP probe		
μPD17201AGF	SE-17207	EP-17201GF	EV-9200G-80	
μPD17202AGF	SE-17202	EP-17202GF	EV-9200G-64	
μPD17203AGC	SE-17203	EP-17203GC	EV-9200G-52	AAMSD-I5DD-172XX
μPD17204GC	SE-17204	EP-17203GC	EV-9200G-52	
μPD17207GF	SE-17207	EP-17201GF	EV-9200G-80	

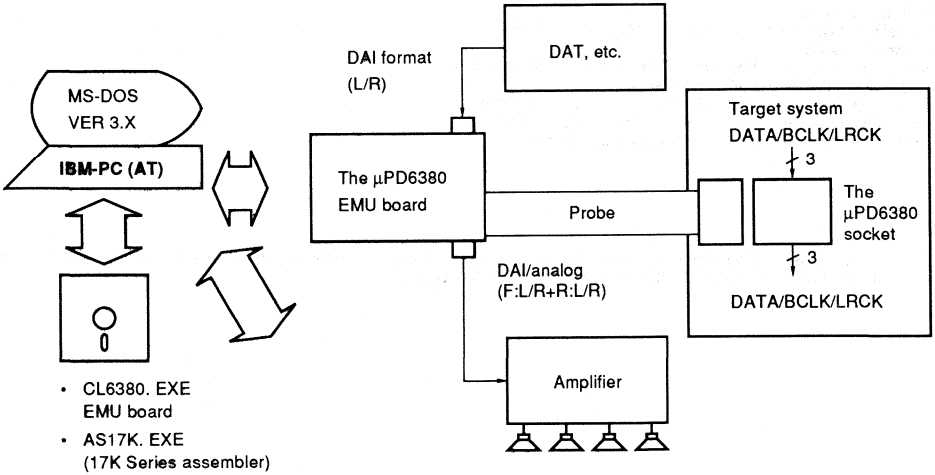
For further and more detailed information about the development tools of the µPD17K-Family please refer to the special user's manual „Development tools".

2. Development tools for the Audio Digital Signal Processors

This section gives a brief explanation of the development environment of the Audio Digital Signal Processors.

Hardware Tools: - EMULATORKIT-6380

Software Tools: - AAMSD-I5DD-6380



- CL6380. EXE
  EMU board
- AS17K. EXE
  (17K Series assembler)
- D6380. DEV
  (The µPD6380 device file)
- DBF 6380. EXE
  (HEX→DB conversion utility)

Development Environment

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EMULATORKIT-6380

The EMULATORKIT-6380 is an emulator designed for developing the audio digital signal processor μPD6380 system. This EMULATORKIT-6380 permits efficient development of a μPD6380 system capable of real-time digital processing of the audio signals and has the following features:

- the host system uses the popular personal computer IBM PC-AT and MS-DOS.
- with DAI (Digital Audio Interface) and a D/A-Converter incorporated, this single emulator permits both the input and output of digital audio signals.
- with the accessory target probe connected to the user's target system, this emulator operates as an in-circuit-emulator.
- abundant provision of the debugging commands and command language (CLICE) permits a series of debugging operation to be stored into the memory and executed automatically.

AAMSD-I5DD-6380

The μPD6380 assembler system is a software to generate a machine language for the μPD6380 providing the following features:

- runs under MS-DOS Ver. 3.1 or later for the IBM PC-AT series personal computer.
- it consists of two programs: assembler and „Define-Byte" conversion utility.
- uses the AS17K as the main unit of the assembler, which serves as the assembler for the μPD17000 series.
- allows split programming which is one of the features of the relocatable assembler while being an absolute assembler.
- creates an assemble report to give assemble information.

For further and more detailed information about the development tools of the Audio Digital Signal Processor please refer to the special user's manuals "UMAA6380..021*10" and "UMIE6380..031*10".

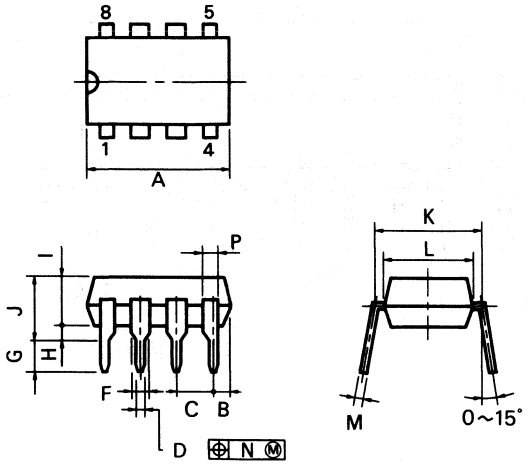
Packaging information

Section 11 - Packaging information

Package/device cross reference

8-Pin Plastic DIP (300 mil)

μPD6252C
μPD6253C
μPD6254C



P8C-100-300B,C

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

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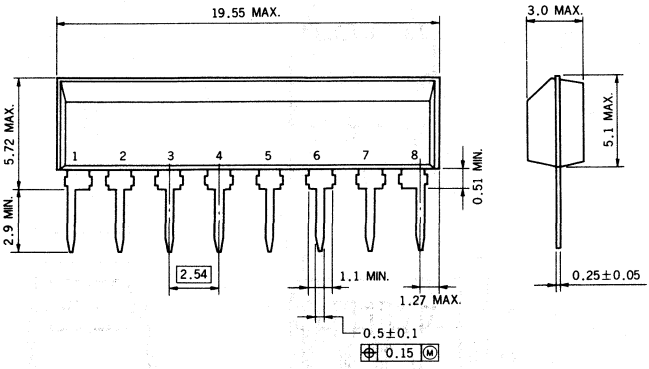
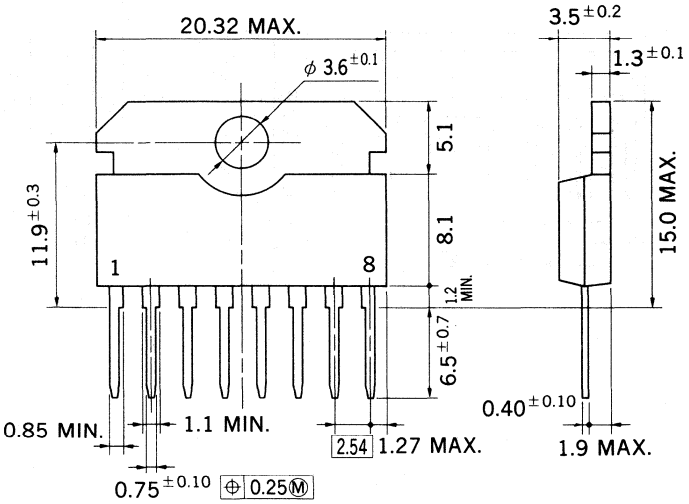
8-Pin Plastic SIP
μPC1228HA

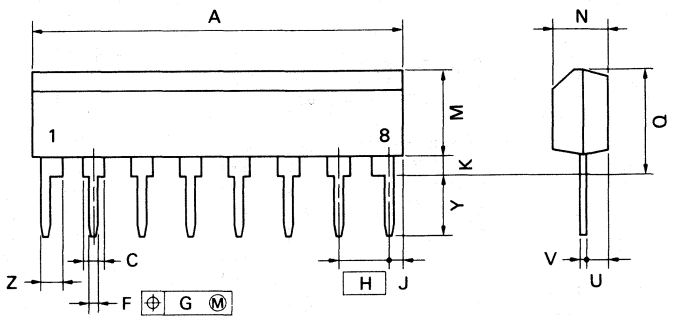


8-Pin Plastic Power SIP
μPC1498H



8-Pin Plastic Slim SIP

μPC2800HA
μPC2801HA
μPC1237HA



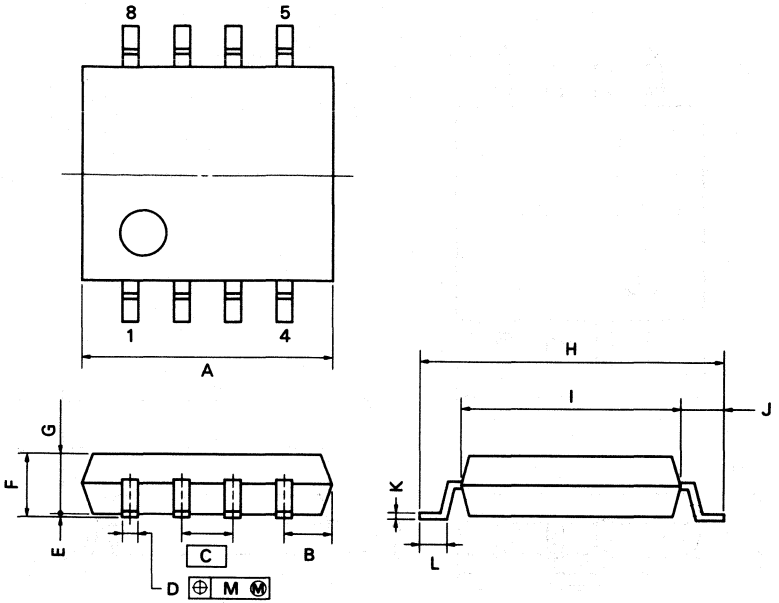
P8HA-254B

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.8 MAX.
C	1.1 MIN.	0.043 MIN.
F	$0.5^{\pm 0.1}$	$0.02^{+0.004}_{-0.005}$
G	0.25	0.01
H	2.54	0.1
J	1.27 MAX.	0.05 MAX.
K	0.51 MIN.	0.02 MIN.
M	5.08 MAX.	0.2 MAX.
N	$2.8^{\pm 0.2}$	$0.11^{+0.008}_{-0.009}$
Q	5.75 MAX.	0.227 MAX.
U	1.5 MAX.	0.059 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.003}$
Y	$3.2^{\pm 0.5}$	$0.126^{\pm 0.02}$
Z	1.1 MIN.	0.043 MIN.

NOTE

Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

8-Pin Plastic SOP (225 mil)
μPC2800GR
μPC2801GR



S8GM-50-225B-1

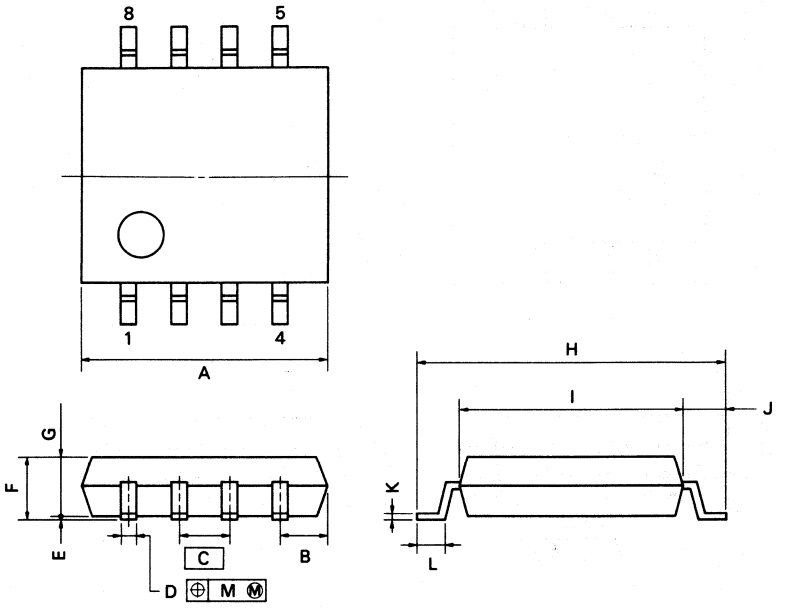
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	5.37 MAX.	0.212 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5 ± 0.3	0.256 ± 0.012
I	4.4	0.173
J	1.1	0.043
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

11

8-Pin Plastic SOP (300 mil)
μPD6253GS-BA1
μPD6254GS-BA1

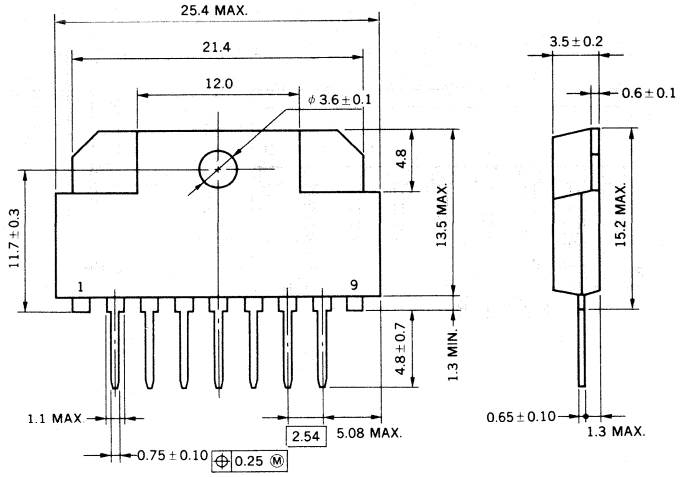


P8GM-50-300B

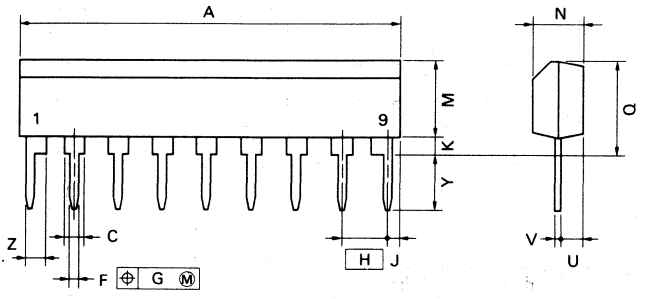
NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	6.65 MAX.	0.262 MAX.
B	1.42 MAX.	0.056 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.08}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.05	0.041
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

9-Pin Plastic Power SIP
μPC1488H



9-Pin Plastic Slim SIP
μPC1313HA
μPC1406HA

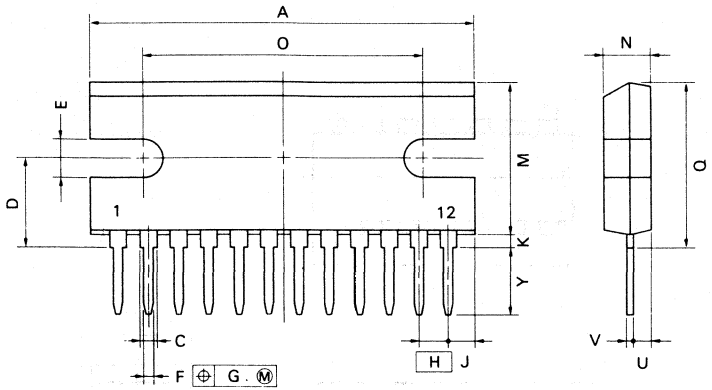


P9HA-254B

NOTE
Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.9 MAX.
C	1.1 MIN.	0.043 MIN.
F	$0.5^{\pm 0.1}$	$0.02^{+0.004}_{-0.005}$
G	0.25	0.01
H	2.54	0.1
J	1.27 MAX.	0.05 MAX.
K	0.51 MIN.	0.02 MIN.
M	5.08 MAX.	0.2 MAX.
N	$2.8^{\pm 0.2}$	$0.11^{+0.008}_{-0.009}$
Q	5.75 MAX.	0.227 MAX.
U	1.5 MAX.	0.059 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.003}$
Y	$3.2^{\pm 0.5}$	$0.126^{\pm 0.02}$
Z	1.1 MIN.	0.043 MIN.

12-Pin Plastic Power SIP
μPC2500H

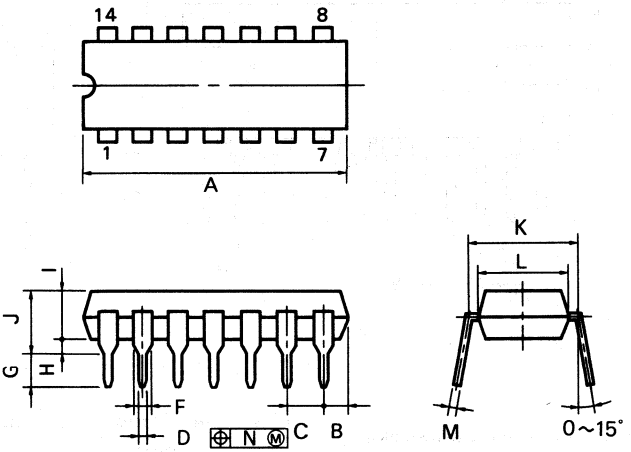


P12HP-254B2

NOTE
Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	33.02 MAX.	1.3 MAX.
C	1.2 MIN.	0.047 MIN.
D	$8.2^{\pm 0.3}$	$0.323^{\pm 0.012}$
E	$3.6^{\pm 0.1}$	$0.142^{\pm 0.004}$
F	$0.8^{\pm 0.1}$	$0.031^{\pm 0.004}$
G	0.25	0.01
H	2.54	0.1
J	2.54 MAX.	0.1 MAX.
K	1.0 MIN.	0.039 MIN.
M	13.8 MAX.	0.544 MAX.
N	$4.8^{\pm 0.2}$	$0.189^{\pm 0.008}$
O	$24.0^{\pm 0.1}$	$0.945^{\pm 0.004}$
Q	15.0 MAX.	0.591 MAX.
U	2.8 MAX.	0.111 MAX.
V	$0.35^{\pm 0.1}$	$0.014^{\pm 0.004}$
Y	$6.5^{+0.7}$	$0.256^{\pm 0.028}$

14-Pin Plastic DIP (300 mil)
μPD4990AC



P14C-100-300A,C

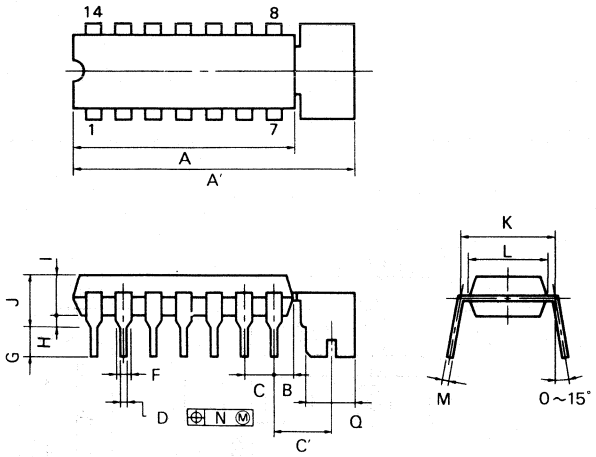
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.003}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

14-Pin Plastic DIP with Tab (300 mil)
μPC1316C



P14CT-100-300B

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

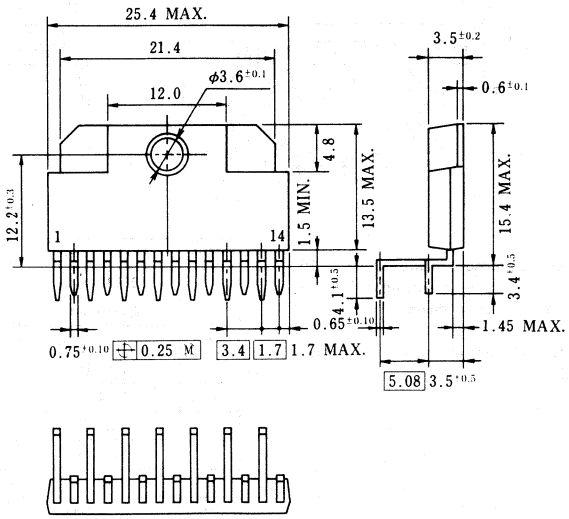
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
A'	24.60 MAX.	0.969 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
C'	4.74	0.187
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.4^{\pm 0.3}$	$0.134^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.30^{+0.10}_{-0.05}$	$0.012^{+0.004}_{-0.003}$
N	0.25	0.01
Q	$4.40^{\pm 0.50}$	$0.173^{\pm 0.020}$

11

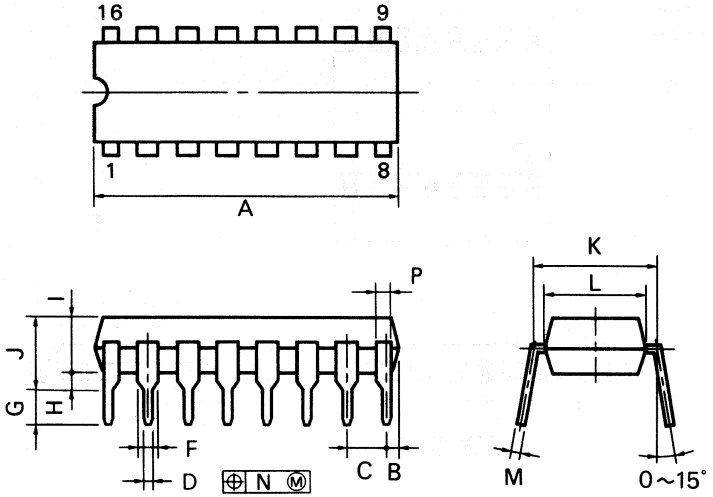
14-Pin Plastic Power VDIP

μPC1298V
μPC1342V
μPC1308V
μPC1310V
μPC1318AV
μPC1335V



16-Pin Plastic DIP (300 mil)

μPD17103CX
μPD17P103CX
μPD17107CX
μPD17P107CX
μPD6123C
μPD6140C-001
μPD6141C-001
μPD6142C-001
μPD6143C-001
μPD6144AC-001
μPD6325C
μPD6326C
μPD6335C
μPD6336C
μPD6901C
μPD6376CX
μPD6316CX



P16C-100-300B

NOTES

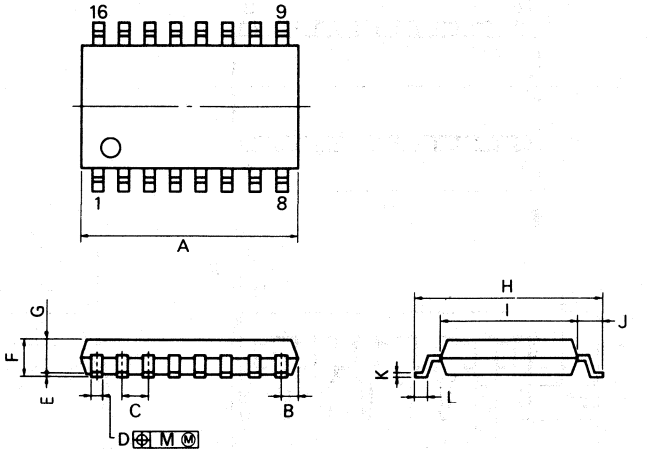
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16-Pin Plastic SOP (300 mil)

μPD17103GS
μPD17P103GS
μPD17107GS
μPD17P107GS
μPD6123G
μPD6252G
μPD6325G
μPD6335G
μPD6376GS
μPD6316GS
μPD4990AG



P16GM-50-300B

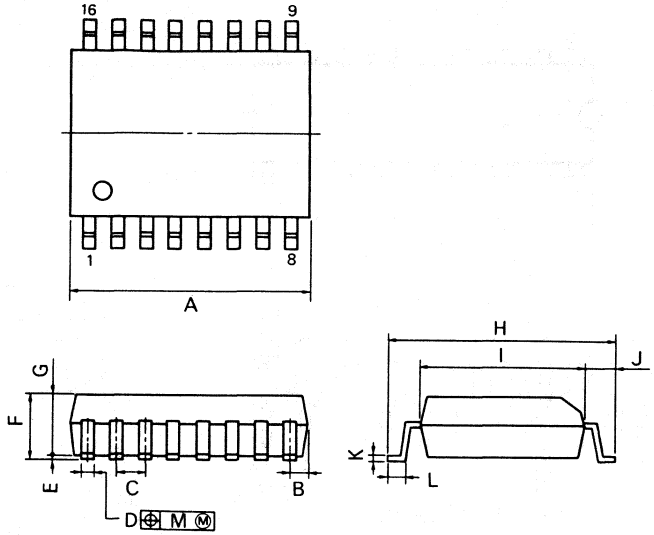
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.08}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.08}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

16-Pin Plastic SOP (375 mil)

μPD6140G-101
μPD6141G-101
μPD6142G-101
μPD6143G-101
μPD6144AG-101



P16GM-50-375B

NOTE

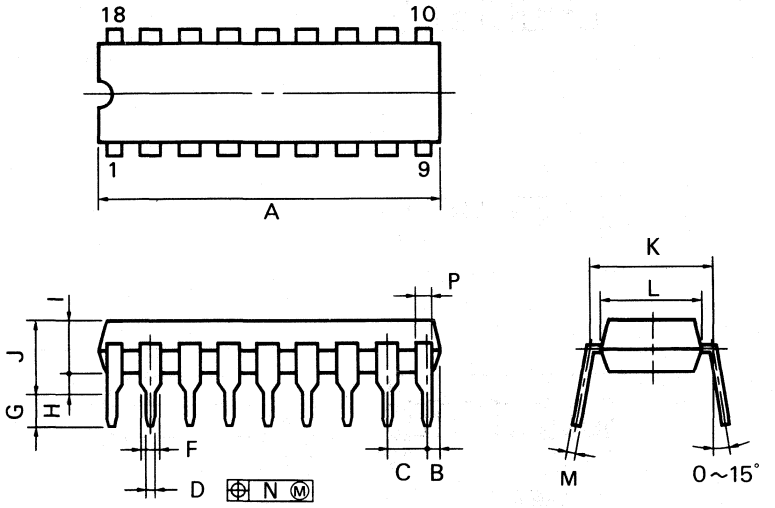
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	$0.1^{+0.2}_{-0.1}$	$0.004^{+0.008}_{-0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{\pm 0.3}$	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

11

18-Pin Plastic DIP (300 mil)

μPD6145C-001
μPD6450CX-002
μPD6451ACX-001
μPD7011C
μPD4991AC



P18C-100-300A,C

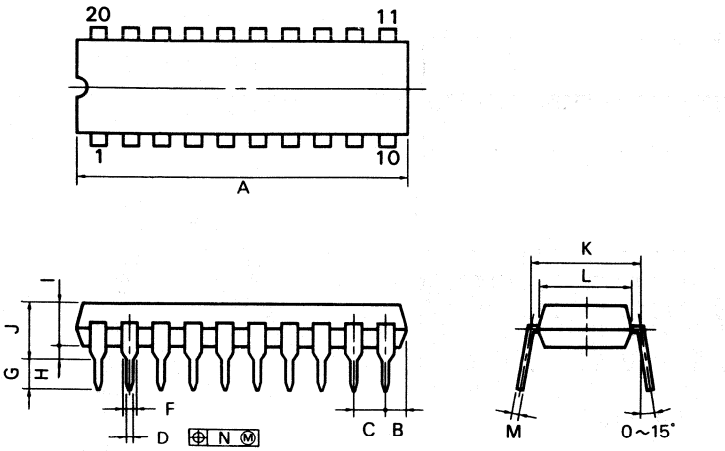
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.

20-Pin Plastic DIP (400 mil)
μPC1891ACY
μPD6453CY-001



P20C-100-400B

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

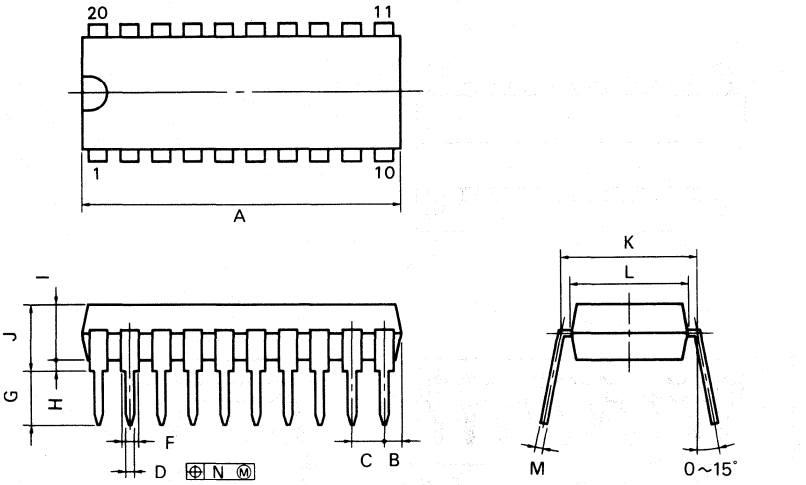
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	27.94 MAX.	1.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

11

20-Pin Plastic Shrink DIP (300 mil)

μPD6124CA
μPD6127CS



P20C-70-300B

NOTES

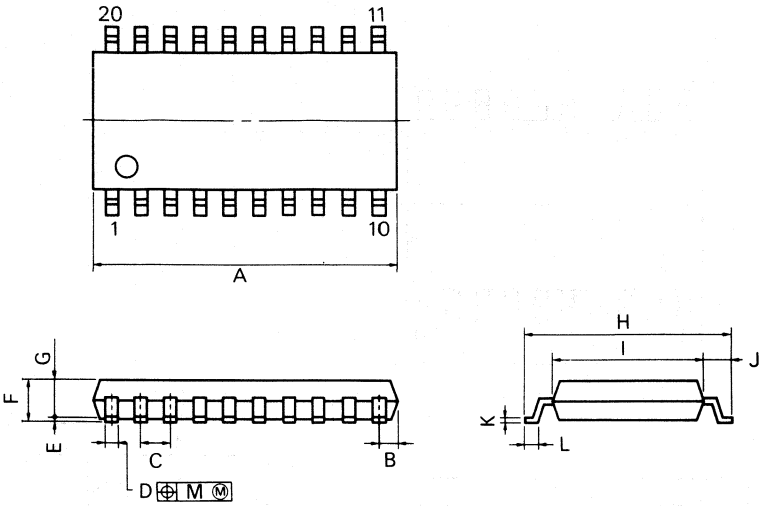
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	19.57 MAX.	0.771 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}$	$0.126^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

20-Pin Plastic SOP (300 mil)

μPD6124G
μPD6127GS
μPD4991AG



P20GM-50-300B,C-1

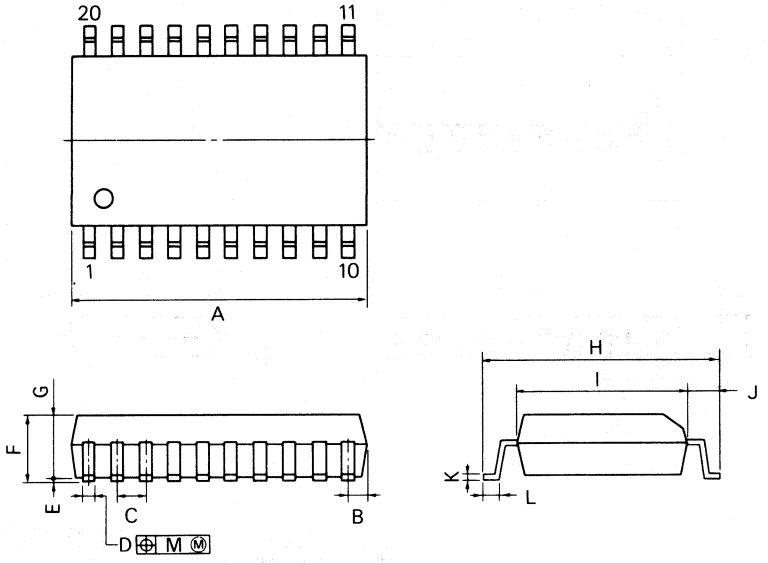
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

20-Pin Plastic SOP (375 mil)

μPD6145G-101
μPD6450GT-102
μPD6451AGT-101
μPD6453GT-101
μPD6460GT-101



P20GM-50-375B-1

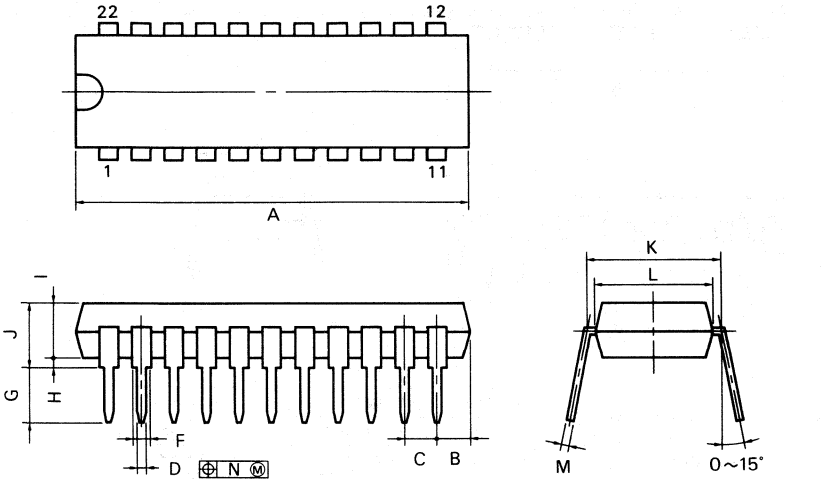
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	$0.004^{+0.008}_{-0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{\pm 0.3}$	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

22-Pin Plastic DIP (300 mil)

μPD17104CS
μPD17P104CS
μPD17108CS
μPD17P108CS



S22C-70-300B

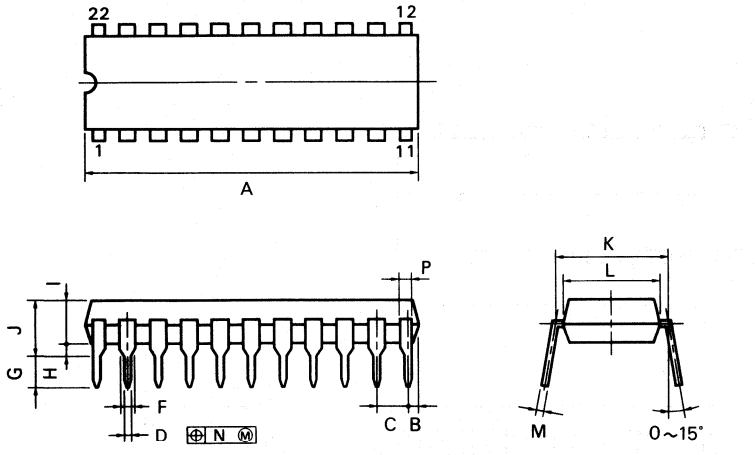
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

22-Pin Plastic DIP (400 mil)
μPD6900C
μPD6902C



P22C-100-400B

NOTES

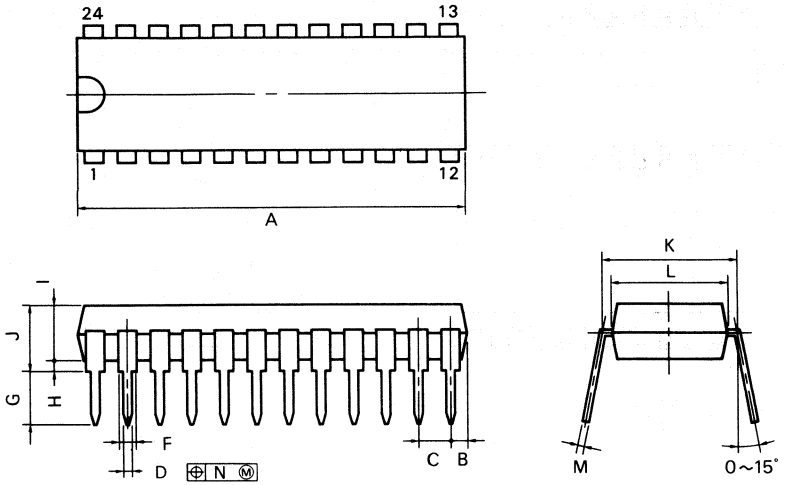
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	27.94 MAX.	1.100 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.8 MIN.	0.031 MIN.

24-Pin Plastic Shrink DIP (300 mil)

μPD6125ACA
μPD6129CS
μPD6452CS



S24C-70-300B

NOTES

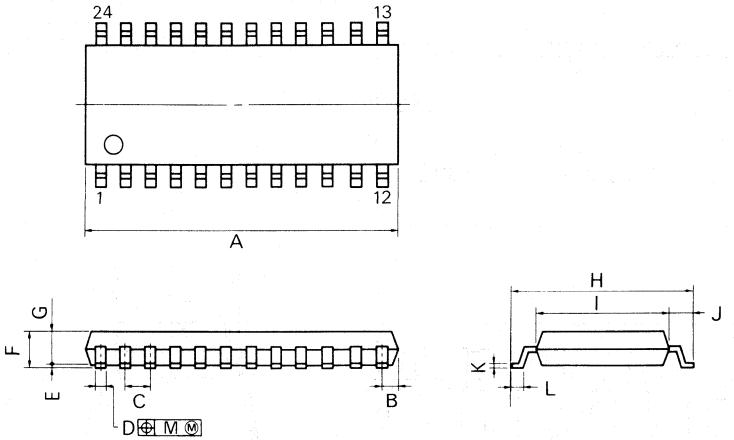
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24-Pin Plastic SOP (300 mil)

μPD17104GS
μPD17P104GS
μPD17108GS
μPD17P108GS
μPD6125AG
μPD6129GS
μPC659G



P24GM-50-300B-1

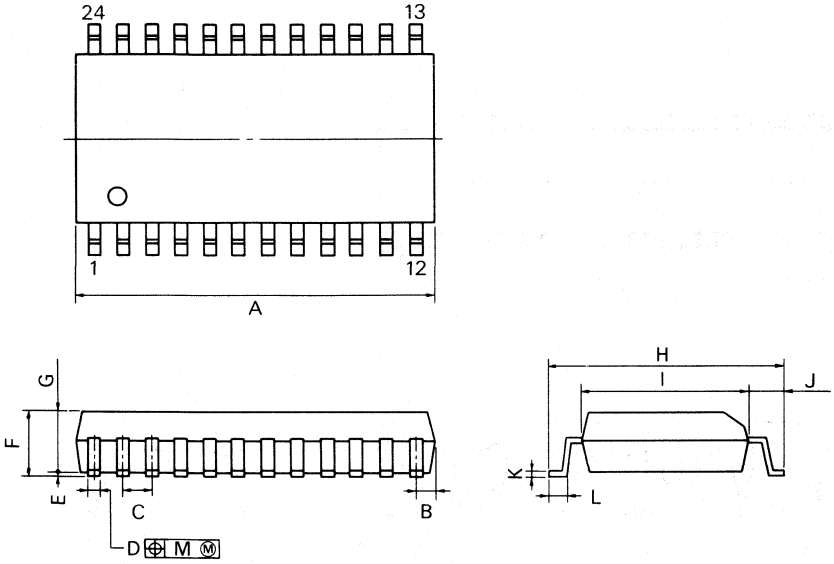
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

24-Pin Plastic SOP (375 mil)

μPD6452GT
μPC661G



P24GM-50-375B-1

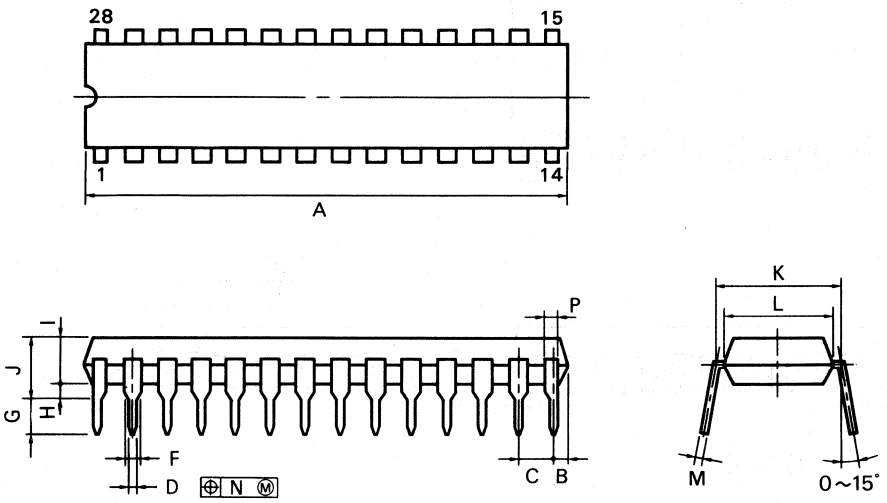
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

28-Pin Plastic Shrink DIP (400 mil)

μPD17134ACT
μPD17135ACT
μPD17136ACT
μPD17P136ACT
μPD17137ACT
μPD17P137ACT
μPD7004C



P28C-100-400

NOTES

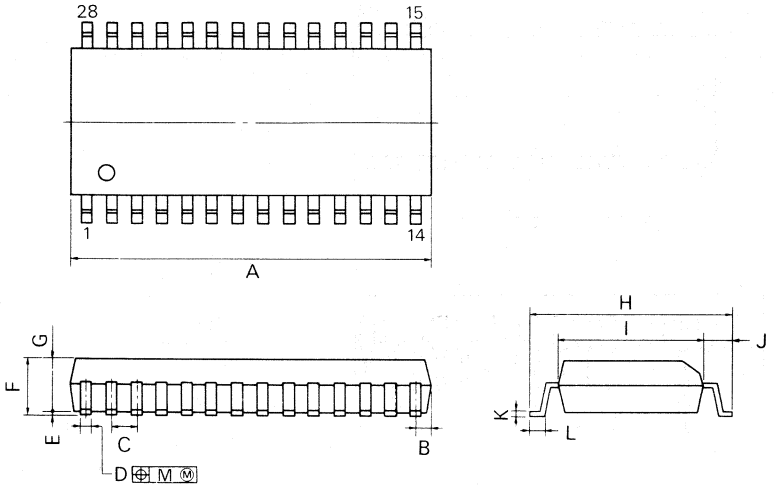
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm0.3}$	$0.138^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

28-Pin Plastic SOP (375 mil)

μPD17134AGT
μPD17135AGT
μPD17136AGT
μPD17P136AGT
μPD17137AGT
μPD17P137AGT
μPD6126AG



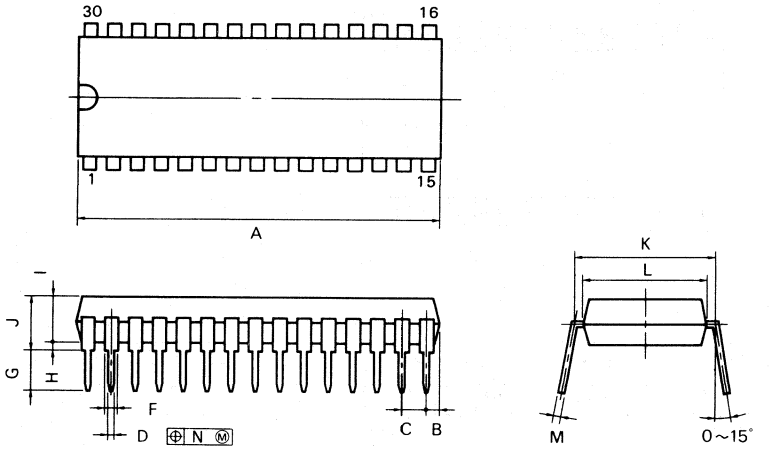
P28GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

30-Pin Plastic Shrink DIP (400 mil)
μPC1820CA



S30C-70-400B

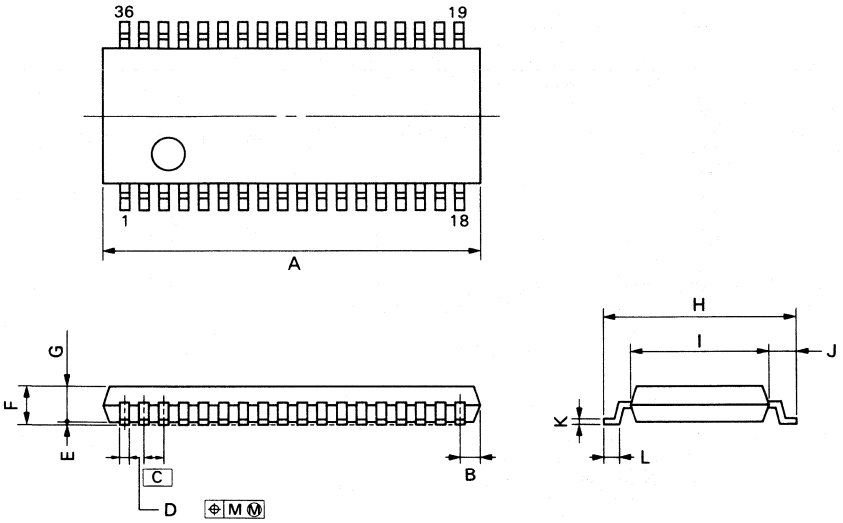
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2 ± 0.3	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

36-Pin Plastic SOP (300 mil)
μPC664GS



P36GM-80-300B-1

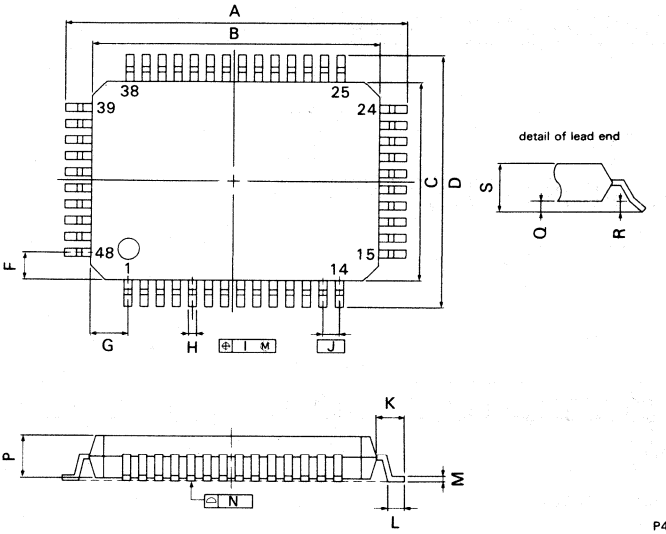
NOTE
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.97 MAX.	0.039 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.35^{+0.10}_{-0.05}$	$0.014^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.10	0.004

11

48-Pin Plastic QFP (10x14)

μPD17001GH-xxx-2A5
μPD17P001GH-2A5
μPC662GH
μPC1340GH-2A5
μPC1348GH-2A5



P48GH-80-2A5-1

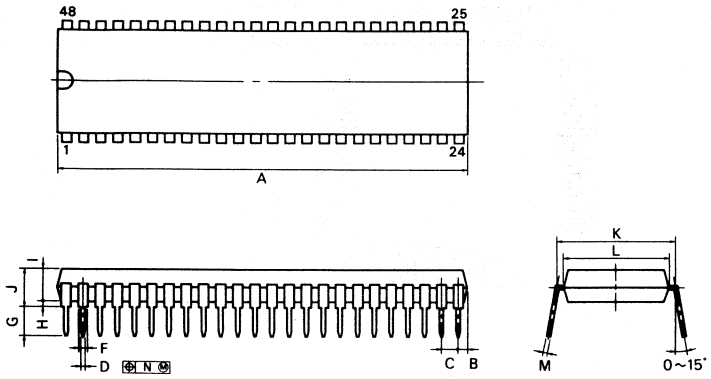
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$16.8^{\pm 0.4}$	$0.661^{+0.017}_{-0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{\pm 0.008}$
C	$10.0^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
D	$12.8^{\pm 0.4}$	$0.504^{\pm 0.016}$
F	1.4	0.055
G	1.8	0.071
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.4^{\pm 0.2}$	$0.055^{\pm 0.008}$
L	$0.6^{\pm 0.2}$	$0.024^{+0.008}_{-0.009}$
M	$0.20^{+0.10}_{-0.05}$	$0.079^{+0.008}_{-0.003}$
N	0.15	0.006
P	$2.2^{\pm 0.1}$	$0.087^{+0.004}_{-0.005}$
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	2.5 MAX.	0.099 MAX.

48-Pin Plastic Shrink DIP (600 mil)

μPD17002CU
μPD17051CU
μPC1880CA



P48C-70-600B

NOTES

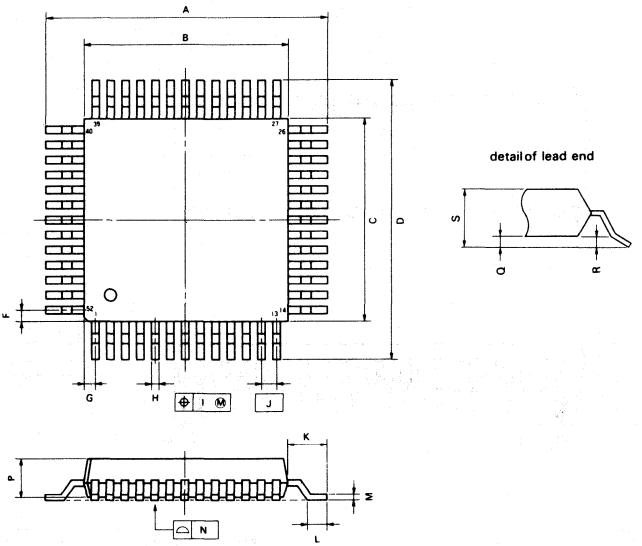
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	44.46 MAX.	1.751 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

52-Pin Plastic QFP (14x14)

μPD6380GC-3BH
μPD17203AGC-xxx-3BH
μPD17P203AGC-001-3BH
μPD17P203AGC-002-3BH
μPD17P203AGC-003-3BH
μPD17204GC-xxx-3BH



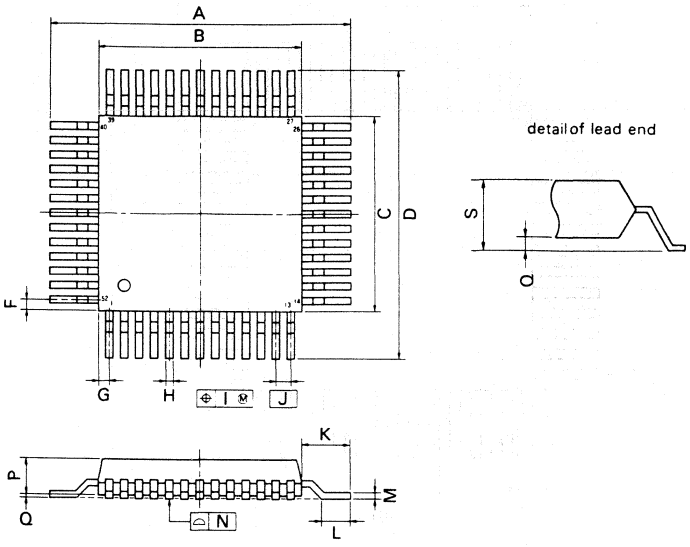
S52GC-100-3BH

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{+0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

52-Pin Plastic QFP (14x14)
bent lead
μPD17102G-xxx-00

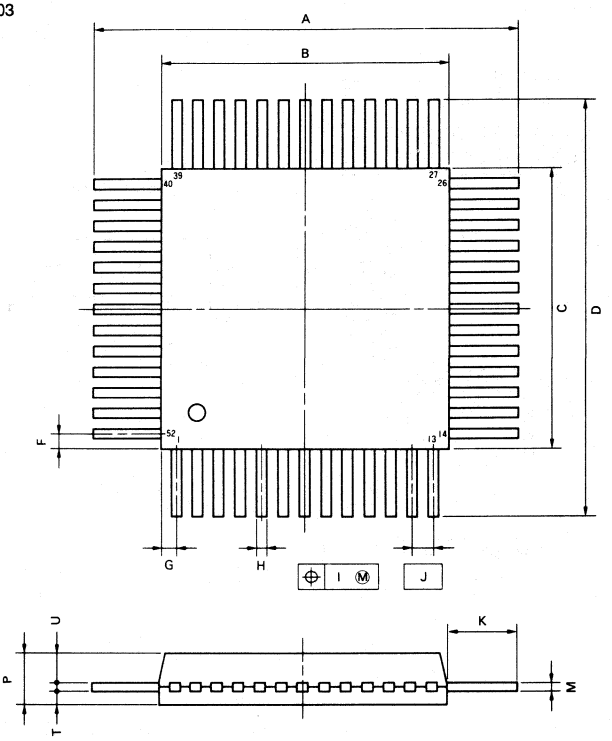


P52G-100-00-1

ITEM	MILLIMETERS	INCHES
A	$21.0^{\pm 0.4}$	$0.827^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$21.0^{\pm 0.4}$	$0.827^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$3.5^{\pm 0.2}$	$0.138^{+0.008}_{-0.009}$
L	$2.2^{\pm 0.2}$	$0.087^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	$2.6^{+0.2}_{-0.1}$	$0.102^{+0.008}_{-0.004}$
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

NOTE
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

52-Pin Plastic QFP (14x14)
straight lead
μPD17102G-xxx-03

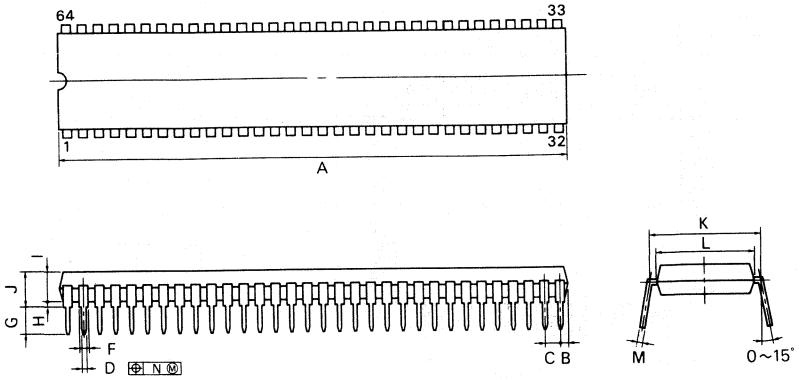


P52G-100-03-1

NOTE
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$19.8^{\pm 0.4}$	$0.780^{+0.016}_{-0.017}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$19.8^{\pm 0.4}$	$0.780^{+0.016}_{-0.017}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$2.9^{\pm 0.2}$	$0.114^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
P	$2.6^{\pm 0.2}$	$0.102^{+0.008}_{-0.009}$
T	1.0	0.039
U	1.45	0.057

64-Pin Plastic Shrink DIP (750 mil)
μPD17052CW
μPD17053CW



P64C-70-750A,C

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

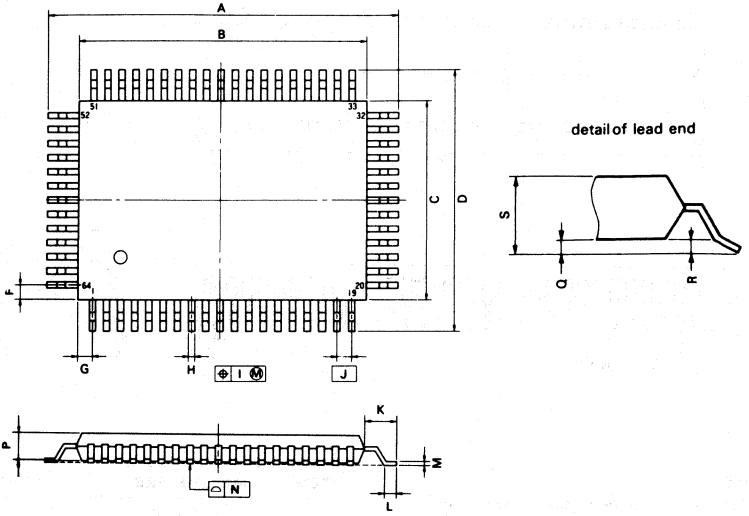
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

11

64-Pin Plastic QFP (14x20)

μPD17106GC
μPD17P106GC
μPD17202AGF-xxx-3BE
μPD17P202AGF-3BE
μPD17301GF-xxx-3BE
μPD42272AGF



P64GF-100-3B8,3BE-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.6^{\pm 0.4}$	$0.929^{\pm 0.016}$
B	$20.0^{\pm 0.2}$	$0.795^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.6^{\pm 0.4}$	$0.693^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

80-Pin Plastic QFP (14x20)

μPD17003AGF-xxx-3B9
μPD17005GF-xxx-3B9
μPD17P005GF-3B9
μPD17006GF-xxx-3B9
μPD17P006GF-3B9
μPD17010GF-xxx-3B9
μPD17P010GF-3B9
μPD17201AGF-xxx-3B9
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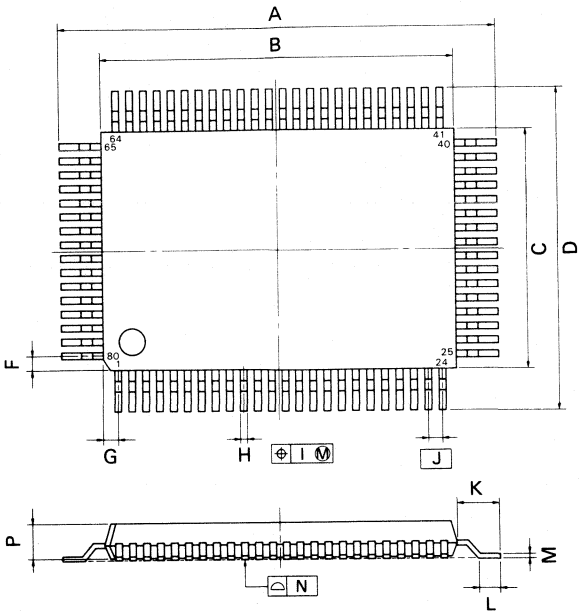
μPD6381GF-3B9
μPD16430GF-3B9



detail of lead end

S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

11

NEC Customer Services

NEC's Commitment to Information

Our offices throughout Europe are always at your service for comprehensive support. Here are some of the technical services we provide:

- INSECT
- Seminars
- Update service
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- University program

INSECT

INformation **S**ystem and **E**lectronic **C**a**T**alog.

This is an on-line information service. Via a telephone link you can call up the latest data on all VLSI devices available from NEC. This includes enhancements, news and the most recent application know-how.

The service is free to our customers and other interested parties. For a menu-driven guest session, you can dial in to INSECT via the international packet switching network – in Germany this is DATEX-P – using of these numbers
45 21 10 13 020/030
and responding to the request for USERNAME and PASSWORD simply with "customer".

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